NA2202/2203/2204

Analog Front End with High Precision 16/20/24-Bit A-D Converter

FEATURES

- Supply Voltage Analog +2.7 to +5.5V (unipolar)
  ±2.5V (bipolar)
  Digital +2.7 to +5.5V
- Ambient Operating Temperature -40°C to 125°C
- ADC Resolution 16/20/24-Bit (No missing codes)
- Data Rate 3.125 to 9.6ksps(1)
- Input mode Differential : 4 inputs
  Single-ended : 8inputs(2)
  Pseudo-differential
- PGA 1V/V to 128V/V
- System Calibration for offset & gain drift
- Built-in Regulator 2.048V±20mV
- Built-In Oscillator 1.2288MHz±3%
- 50Hz/60Hz Rejection Mode
- Current Consumption Analog 2.9mA (Normal
  Low Power Mode 0.9mA
  Digital 0.26mA
- Conversion mode Single / Continuous
- Excitation Current Source
  2 systems (0.1mA, 0.25mA, 0.5mA, 1.0mA)
- Interface SPI
- CS (Chip Select)
- Error detection CRC8, Check Sum
- Package QFN4040-24-NB

(1) Case of Continuous conversion. (Single conversion is 1/3 the data rate.)

(2) PGA2 can be used only. (PGA1 cannot be used.) Eight channels of VIN1P, VIN1N, VIN2P, VIN2N, VIN3P, VIN3N, VIN4P and VIN4N can be used.

APPLICATIONS

- Temperature Controller
- Pressure sensors
- Flowmeters
- PLC
- Digital Panel Mater

GENERAL DESCRIPTION

NA2202/2203/2204 are C-MOS based high precision AFE with up to 128 times internal PGA (Programmable Gain Amplifier).

Internal 16/20/24-bit ΔΣ type A / D converter can perform conversion rates from 3.125sps to 9.6ksps.

NA2202/2203/2204 have error detection. (CRC8 or Check Sum.)

It is useful for noise applications.

It is also possible to turn off the CRC.

NA2202/2203/2204 support bipolar operation of analog supply voltage, for example AVDD is set in +2.5V and AVSS is in -2.5V. A negative voltage input is possible such as thermocouple.

Two matched excitation current sources supply the bias of pressure sensor, resistance temperature detectors, and so on.

The matching error between two excitation current sources is less than 1% in 3-sigma.

By using low power consumption mode, power consumption can be reduced to about 1/3 of normal operation.

The conversion data rate in the low power consumption mode operates at 1/4 of the normal operation.

QFN4040-24-NB
4.0 × 4.0 × 0.75(mm)

Case of Continuous Conversion. (Single conversion is 1/3 the data rate.)

PGA2 can be used only. (PGA1 cannot be used.) Eight channels of VIN1P, VIN1N, VIN2P, VIN2N, VIN3P, VIN3N, VIN4P andVIN4N can be used.

PRODUCT NAME INFORMATION

NA2202 NB A E2 S
NA2203 NB A E2 S
NA2204 NB A E2 S

Description of configuration

Suffix	Item	Description
NB	Package code	Indicates the package. Refer to the order information.
A	Version	Product version A: Specified value
E2	Packing	Refer to the packing specifications.
S	Grade	Indicates the quality grade.

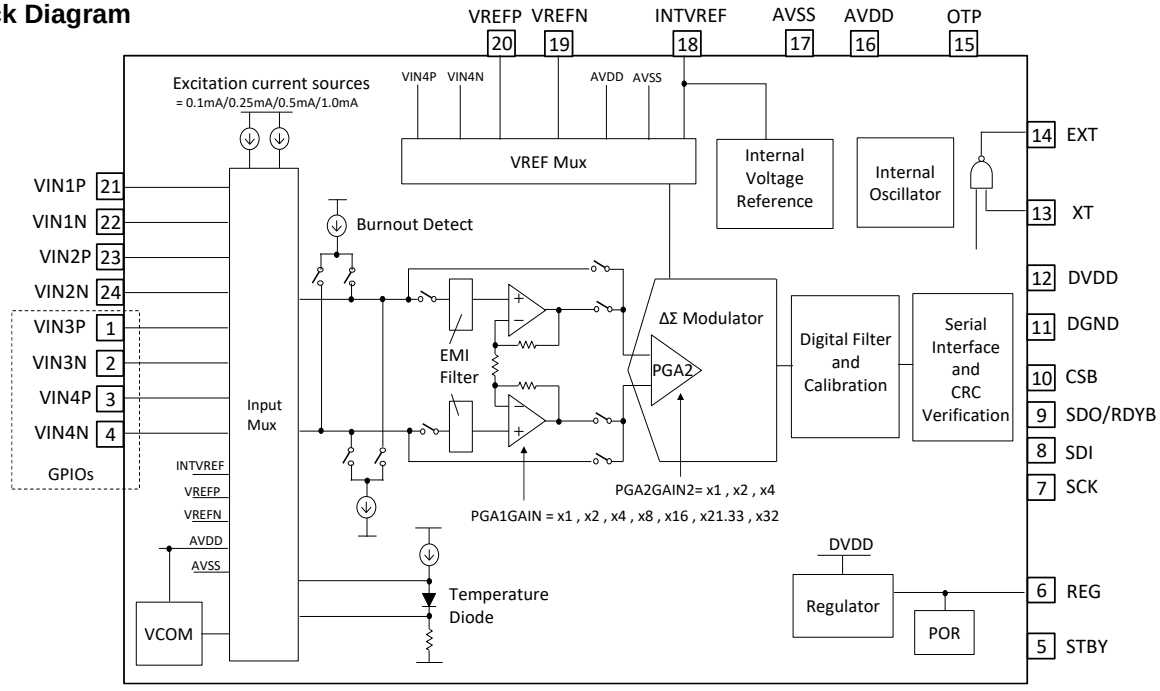
Grade

Grade	Usage	Operating Temperature Range	Test Temperature
S	General-purpose and Consumer application	−40°C to 125°C	25°C

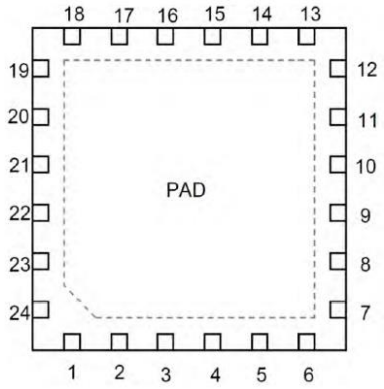
■ ORDER INFORMATION

Product Name	Package	RoHS	Halogen-Free	Plating Composition	Weight (mg)	Quantity (pcs/reel)
NA2202NBAE2S	QFN4040-24-NB	Yes	Yes	Sn-2Bi	31	1,000
NA2203NBAE2S	QFN4040-24-NB	Yes	Yes	Sn-2Bi	31	1,000
NA2204NBAE2S	QFN4040-24-NB	Yes	Yes	Sn-2Bi	31	1,000

■ Block Diagram



■ PIN DESCRIPTION



QFN4040-24-NB Pin Configuration

Pin No.	Pin Name	I/O	Description
1	VIN3P	Analog Input	Differential positive input 3 / Single-end input 5 / GPIO
2	VIN3N	Analog Input	Differential negative input 3 / Single-end input 6 / GPIO
3	VIN4P	Analog Input	Differential positive input 4 / Single-end input 7 / GPIO
4	VIN4N	Analog Input	Differential negative input 4 / Single-end input 8 / GPIO
5	STBY	Digital Input	Stand-by terminal (Normally connected to DGND)
6	REG	Power Supply	Internal Regulator Output. (Connected to 0.1µF capacitor between REG and DGND terminal. Prohibition of connection of IC to external circuit)
7	SCK	Digital Input	SPI SCK
8	SDI	Digital Input	SPI SDI
9	SDO/RDYB	Digital Input	SPI SDO/RDYB
10	CSB	Digital Input	SPI CSB
11	DGND	Digital GND	Digital GND
12	DVDD	Power Supply	Digital VDD
13	EXT	-	Pin for connecting Xtal (Recommended to connect a 4.9152MHz crystal unit)
14	XT	- / Digital Input	Pin for connecting Xtal / External CK input
15	OTP	GND	Connected AVSS
16	AVDD	Analog Power Supply	Analog positive power supply
17	AVSS	Analog GND	Analog negative power supply
18	INTVREF	Power Supply	VREF output voltage (Connected to 2.2µF capacitor between INTVREF and AVSS terminal.)
19	VREFN	REF Input	External negative reference voltage input (usually connected to AVSS)
20	VREFP	REF Input	External positive reference voltage input
21	VIN1P	Analog Input	Differential positive input 1 / Single-end input 1
22	VIN1N	Analog Input	Differential negative input 1 / Single-end input 2
23	VIN2P	Analog Input	Differential positive input 2 / Single-end input 3
24	VIN2N	Analog Input	Differential negative input 2 / Single-end input 4
-	EXT_PAD	-	Connected AVSS

Please refer to “TYPICAL APPLICATION CIRCUIT“ or “APPLICATION NOTES“ for details.

■ ABSOLUTE MAXIMUM RATINGS

	Symbol	Ratings	Unit
Analog Positive Supply Voltage	$(AVDD-AVSS)_{abso}$	7.0(3)	V
Analog Negative Supply Voltage	$AVSS_{abso}$	-5.0(3)	V
Digital Supply Voltage	$DVDD_{abso}$	7.0(4)	V
Power Dissipation (Ta=25℃)	P_D	830(5)/2100(6)	mW
Analog Input Voltage	V_{IA}	(AVSS-0.3) to (AVDD+0.3)(7)	V
Digital Input Voltage	V_{ID}	-0.3 to (DVDD+0.3)(7)	V
Operation Temperature Range	T_{opr}	-40 to +125	°C
Storage Temperature Range	T_{stg}	-40 to +150	°C

(3) The difference between the absolute maximum power supply voltage and the operating power supply voltage is small. Please be careful so that the operating power supply voltage does not exceed the absolute maximum supply voltage by spike voltage.
(4) Digital Power Supply Voltage is DGND reference.
(5) Mounted on glass epoxy board.
(114.3 x 76.2 x 1.57mm: based on EIA/JEDEC standard, 2Layers FR-4, with Exposed Pad)
(6) Mounted on glass epoxy board
(114.3 x 76.2 x 1.6mm: based on EIA/JEDEC standard, 4Layers FR-4, with Exposed Pad)
(7) Input pin is connected to the clamp diode to the power supply pin. When the input signal exceeds the supply rails 0.3V or more (below the DGND rail 0.3V or more), the input current must be limited to less than 10mA.

ABSOLUTE MAXIMUM RATINGS

Electronic and mechanical stress momentarily exceeded absolute maximum ratings may cause permanent damage and may degrade the lifetime and safety for both device and system using the device in the field. The functional operation at or over these absolute maximum ratings is not assured.

■ ELECTRICAL CHARACTERISTICS

ELECTRICAL CHRACTERISTICS(Analog Input)

NA2202NBAE1S_NA2203NBAE1S_NA2204NBAE1S

Unless otherwise specified, all limits ensured for T_a = +25°C, AVDD = 5.0V, VREFP = 0.5 x (AVDD-AVSS)+AVSS, DVDD=5V, AVSS=0V, VREFN = 0V, DGND=0V, DR=400sps

Parameter	Symbol	Condition	MIN	TYP	MAX	UNIT
Analog Input 1 (PGA1 = unused, PGA2 = used, PGAIN2 = 1 or 2 or 4)						
Differential Input Voltage Range 1	VDIN1		-	±VREF / (PGAIN2)	-	V
Common Mode Input Voltage Range 1	VCIN1	PGAIN2 = 1	VSS+0.4[8]	-	AVDD	V
Input Impedance 1	ZIN1	FMOD = 614.4kHz PGAIN2 = 1	-	900	-	kΩ
		FMOD = 614.4kHz PGAIN2 = 2 or 4	-	450	-	kΩ
Common Mode Rejection Ratio 1	CMRR1	PGAIN2 = 1	70	90	-	dB
Analog Input 2 (PGA1, 2 = used, PGAIN1 = 1 or 2 or 4 or 8 or 16 or 21.33 or 32 PGAIN2=1 or 2 or 4)						
Differential Input Voltage Range2	VDIN2	PGAIN1 ≥ 2	-	(±VREF) / (PGAIN1 x PGAIN2)	-	V
Common Mode Input Voltage Range 2	VCIN2		AVSS+0.4	-	AVDD-0.5	V
Input Impedance 2	ZIN2		-	100	-	MΩ
Common Mode Rejection Ratio 2	CMRR2	PGAIN1 = 2 PGAIN2 = 1 CHOP = ON	70	90	-	dB

[8] In case of VREFP=VDD, VREFN=AVSS condition, “Common Mode Input Voltage Range 1” is AVSS (Min.).

ELECTRICAL CHARACTERISTICS (Reference Voltage Input)

Unless otherwise specified, all limits ensured for T_a = +25°C, AVDD = 5.0V, VREFP=5.0V, DVDD=5.0V, AVSS=0V, VREFN=0V, DGND = 0V

Parameter	Symbol	Condition	MIN	TYP	MAX	UNIT
Positive Reference Voltage	VREFP		(AVDD+AVSS) x0.4+AVSS	-	AVDD	V
Negative Reference Voltage	VREFN		AVSS	-	AVSS+2.2	V
Reference Voltage	VREF	VREF = VREFP - VREFN	(AVDD-AVSS) x0.4	(AVDD-AVSS) x0.5	AVDD-AVSS	V
Input Impedance 3	ZIN3	FMOD = 614.4kHz PGAIN2 = 1 or 2	-	450	-	kΩ
		FMOD = 614.4kHz PGAIN2 = 4	-	900	-	kΩ
Internal VREF Output	INTVREF	2.2µF capacitor between INTVREF and AVSS.	2.028+AVSS	2.048+AVSS	2.068+AVSS	V
Internal VREF TEMP Drift	INTVREF_TC		-	±25	-	ppm

ELECTRICAL CHARACTERISTICS (Internal Regulator, Bias Voltage)

Unless otherwise specified, all limits ensured for T_a = +25°C, AVDD = 5.0V, DVDD=5.0V, AVSS=0V, DGND = 0V

Parameter	Symbol	Condition	MIN	TYP	MAX	UNIT
Output Voltage	REG	0.1µF capacitor between REG and DGND.	-	2.4	-	V
VCOM Voltage	VCOM		-	(AVDD-AVSS) x 0.5+AVSS	-	V

ELECTRICAL CHARACTERISTICS (Internal Oscillator)

Unless otherwise specified, all limits ensured for T_a = +25°C, AVDD = 5.0V, DVDD=5.0V, AVSS=0V, DGND = 0V

Parameter	Symbol	Condition	MIN	TYP	MAX	UNIT
OSC Frequency	FOSC		1191.9	1228.8	1265.7	kHz

ELECTRICAL CHARACTERISTICS (Internal Temperature Sensor)

Unless otherwise specified, all limits ensured for T_a = +25°C, AVDD = 5.0V, DVDD=5.0V, AVSS=0V, DGND = 0V

Parameter	Symbol	Condition	MIN	TYP	MAX	UNIT
Sensor Voltage	VTEMP	TEMPP-TEMPN Ta=25°C	-	0.74	-	V
Sensitivity	TSLOPE		-	-1.7	-	mV/°C

ELECTRICAL CHARACTERISTICS (Excitation Current Source)

Unless otherwise specified, all limits ensured for T_a = +25°C, DVDD = 5.0V, DGND = 0V

Parameter	Symbol	Condition	MIN	TYP	MAX	UNIT
Output Current 1	IEX1[9]		-	0.10, 0.25, 0.50, 1.00	-	mA
Output Current 2	IEX2[9]		-	0.10, 0.25, 0.50, 1.00	-	mA
Absolute Value Deviation 1	IEX1_E	(Measured Value – IEX1) / IEX1 x 100	-	-	±10	%
Absolute Value Deviation 2	IEX2_E	(Measured Value – IEX2) / IEX2 x 100	-	-	±10	%
Matching Error	IEX_ME	IEX1 = IEX2 = 1mA, (IEX2 - IEX1) / IEX1 x 100	-	-	±1	%
Temperature Drift 1	IEX1_TD	Ta = 25 to 125℃ (IEX125 - IEX25) / IEX25 x 10 ^ 6 / (125 - 25) [10]	-	±100	-	ppm /°C
Temperature Drift 2	IEX2_TD	Ta = 25 to 125℃ (IEX125 - IEX25) / IEX25 x 10 ^ 6 / (125 - 25) [10]	-	±100	-	ppm /°C
Temperature Drift Matching Error	IEX_TD_ME	IEX2_TD - IEX1_TD [11]	-	±10	-	ppm /°C
Compliance Voltage	VCOMP		-	AVDD-0.8	-	V

[9] IEX1 -> Measured value of Excitation current source 1.
IEX2 -> Measured value of Excitation current source 2.
[10] IEX25 -> Measured value at 25℃.
IEX125 -> Measured value at 125℃.
[11] IEX1_TD -> Temperature Drift of Excitation current source 1.
IEX2_TD -> Temperature Drift of Excitation current source 2.

ELECTRICAL CHARACTERISTICS (Burn Out Current Source)

Unless otherwise specified, all limits ensured for T_a = +25°C, AVDD=5C, DVDD = 5.0V, AVSS=0V, DGND = 0V

Parameter	Symbol	Condition	MIN	TYP	MAX	UNIT
Burn Out Current Sink	IBURNP		-	10.0	-	µA
Burn Out Current Source	IBURNN		-	10.0	-	µA

ELECTRICAL CHARACTERISTICS (Programmable Gain Amplifier)

Unless otherwise specified, all limits ensured for T_a = +25°C, AVDD=5.0V, DVDD=5V, AVSS=0V, DGND=0V

Parameter	Symbol	Condition	MIN	TYP	MAX	UNIT
PGA1 Gain	PGAIN1		-	1, 2, 4, 8, 16, 21.33, 32	-	V/V
PGA2 Gain	PGAIN2		-	1, 2, 4	-	V/V

ELECTRICAL CHARACTERISTICS (Analog to Digital Convertor)

Unless otherwise specified, all limits ensured for T_a = 25°C, DVDD = 5V, VREFP = 0.5 x (AVDD-AVSS)+AVSS, DVDD=5V, AVSS=0V, VREFN = 0V, DGND=0V, PGAIN1 = PGAIN2 = 1, VCIN2 = 0.5 x (AVDD-AVSS)+AVSS

Parameter	Symbol	Condition	MIN	TYP	MAX	UNIT
Resolution	N	NA2202 No missing codes(12)	16	-	-	Bit
		NA2203 No missing codes(12)	20	-	-	Bit
		NA2204 No missing codes(12)	24	-	-	Bit
Data Rate	DR		Refer to Table			sps
Clock Frequency	FMOD (MDCK)	FMOD = FOSC / 2	596.0	614.4	632.8	kHz
Integral Non Linearity	INL	best-fit-line method(13) VREFP = 5.0V PGAIN1 = 2	-	±10	±40	ppm
Offset Error	OE	PGAIN1 = 32 PGAIN2 = 4 DR = 400sps CHOP = ON	-	±1	±2	µV
Gain Error	GE	PGAIN = 1 to 32 PGAIN = 1	-	±0.5	±2.0	%
		PGAIN1 = 32 PGAIN2 = 2 to 4	-	±0.5	±3.0	%
Noise Free Bit(12)(14)	NFB		Refer to Table			Bit

(12) This parameter is not production tested.
(13) Guaranteed by design evaluation and several points test
(14) NFB represents the ADC output code variations 6.6σ with the differential input shorted.
The specifications for noise-free bits are defined by the conversion data rate and the PGA gain setting.
(See Table for NA2202/2203/2204 Effective Resolution and NFB)

ELECTRICAL CHARACTERISTICS (Power Supply / Supply Current)

Unless otherwise specified, all limits ensured for Ta = 25°C, AVDD = 5.0V, VREFP = 0.5 x (AVDD-AVSS)+AVSS, DVDD=5V, AVSS=0V, VREFN = 0V, DGND = 0V

Parameter	Symbol	Condition	MIN	TYP	MAX	UNIT
Analog Power Supply Voltage	AVDD-AVSS	AVDD ≥ 1.35V	2.7	5.0	5.5	V
Analog Negative Power Supply Voltage	AVSS		-2.75	-	0	V
Digital Power Supply Voltage	DVDD		2.7	5.0	5.5	V
Analog Supply Current Normal Mode	IDD_{ana}	PGA1 OFF	-	1.9	2.4	mA
		PGA1 ON	-	2.9	3.6	mA
Digital Supply Current Normal Mode	IDD_{dig}	PGA1 OFF	-	0.26	0.35	mA
		PGA1 ON	-	0.26	0.35	mA
Analog Supply Current Low Power Mode	IDD LOW_{ana}	PGA1 OFF	-	0.6	0.9	mA
		PGA1 ON	-	0.9	1.2	mA
Digital Supply Current Low Power Mode	IDD LOW_{dig}	PGA1 OFF	-	0.26	0.35	mA
		PGA1 ON	-	0.26	0.35	mA
Analog Supply Current Sleep Mode	$IDDSLP_{ana}$		-	0.14	0.26	mA
Digital Supply Current Sleep Mode	$IDDSLP_{dig}$		-	0.14	0.27	mA
Supply Current Standby Mode	IDD_{STBY}	STBY = DVDD	-	-	1.0	µA

ELECTRICAL CHARACTERISTICS (GPIO)

Unless otherwise specified, all limits ensured for Ta = 25°C, AVDD = 5V, DVDD = 5V, AVSS = 0V, DGND = 0V

Parameter	Symbol	Condition	MIN	TYP	MAX	UNIT
High-Level Input Voltage	$V_{gpio-ih}$		0.7 x (AVDD-AVSS)+AVSS	-	AVDD	V
Low-level input voltage	$V_{gpio-il}$		AVSS	-	0.3x(AVDD-AVSS)+AVSS	V
High-Level Output Voltage	$V_{gpio-oh}$	AVDD-AVSS=4.5 to 5.5V $I_{gpio-oh}$ max=24mA	0.8x(AVDD-AVSS)+AVSS	-	AVDD	V
		AVDD-AVSS=2.7 to 4.5V $I_{gpio-oh}$ max=10mA	0.8x(AVDD-AVSS)+AVSS	-	AVDD	V
Low-Level Output Voltage	$V_{gpio-ol}$	AVDD-AVSS=4.5 to 5.5V $I_{gpio-ol}$ max=24mA	AVSS	-	0.2x(AVDD-AVSS)+AVSS	V
		AVDD-AVSS=2.7 to 4.5V $I_{gpio-ol}$ max=10mA	AVSS	-	0.2x(AVDD-AVSS)+AVSS	V

ELECTRICAL CHARACTERISTICS (XT/EXT)

Unless otherwise specified, all limits ensured for Ta = 25°C, AVDD = 5V, DVDD = 5V, AVSS = 0V, DGND = 0V

Parameter	Symbol	Condition	MIN	TYP	MAX	UNIT
High-Level Input Voltage	$V_{xt\text{-}ih}$		0.7 x DVDD	-	DVDD	V
Low-level input voltage	$V_{xt\text{-}il}$		DGND	-	0.3xDVDD	V
High-Level Output Voltage	$V_{ext\text{-}oh}$	AVDD-AVSS=4.5 to 5.5V $I_{gpio\text{-}oh}$_max=1.5mA	0.8xDVDD	-	DVDD	V
		AVDD-AVSS=2.7 to 4.5V $I_{gpio\text{-}oh}$_max=0.3mA	0.8xDVDD	-	DVDD	V
Low-Level Output Voltage	$V_{ext\text{-}ol}$	AVDD-AVSS=4.5 to 5.5V $I_{gpio\text{-}ol}$_max=3mA	DGND	-	0.2xDVDD	V
		AVDD-AVSS=2.7 to 4.5V $I_{gpio\text{-}ol}$_max=1mA	DGND	-	0.2xDVDD	V

ELECTRICAL CHARACTERISTICS (with Out GPIO)

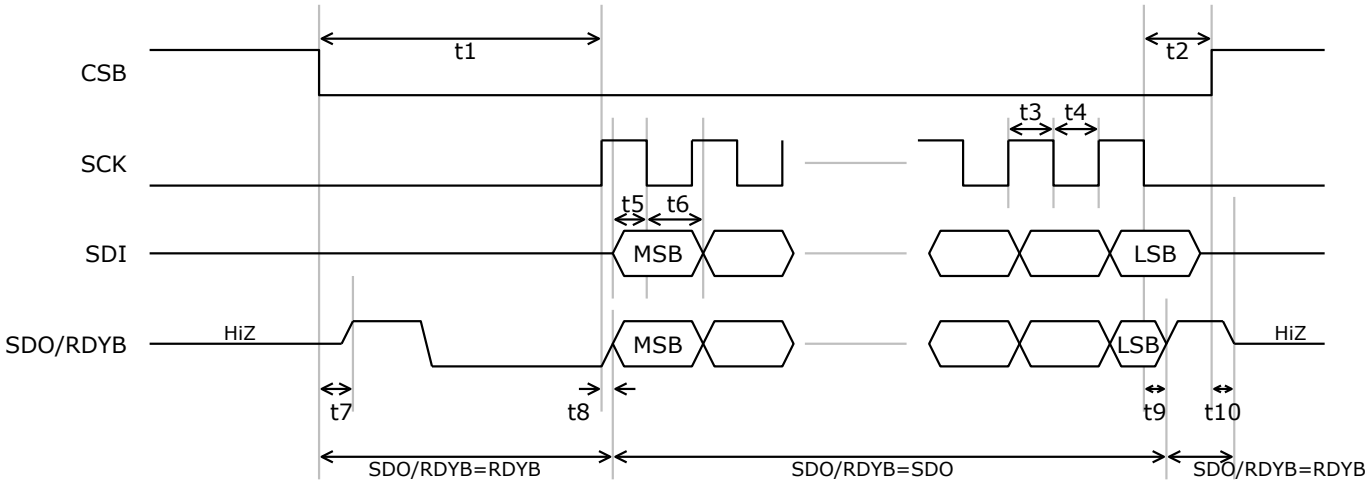
Unless otherwise specified, all limits ensured for Ta = 25°C, DVDD = 5V, DGND = 0V

Parameter	Symbol	Condition	MIN	TYP	MAX	UNIT
High-Level Input Voltage	V_{ih}	DVDD=2.7 to 5.5V	0.8xDVDD	-	DVDD	V
Low-level input voltage	$V_{xt\text{-}il}$	DVDD=2.7 to 5.5V	DGND	-	0.2xDVDD	V
High-Level Output Voltage	$V_{ext\text{-}oh}$	DVDD=2.7 to 5.5V $I_{gpio\text{-}oh}$_max=8mA	0.8xDVDD	-	DVDD	V
Low-Level Output Voltage	$V_{ext\text{-}ol}$	DVDD=2.7 to 5.5V $I_{gpio\text{-}ol}$_max=8mA	DGND	-	0.2xDVDD	V

ELECTRICAL CHARACTERISTICS (Serial Peripheral Interface)

Parameter	Symbol	MIN	TYP	MAX	UNIT
SPI clock frequency	f_{sck}	-	-	5	MHz
Setup time, CSB falling edge to first SCK rising edge	t1	15	-	-	nsec
Hold time, final SCK falling edge to CSB rising edge	t2	15	-	-	nsec
Pulse duration, SCK high	t3	80	-	-	nsec
Pulse duration, SCK low	t4	80	-	-	nsec
Setup time, SDI input data valid before SCK falling edge	t5	15	-	-	nsec
Hold time, SDI input data valid after SCK falling edge	t6	15	-	-	nsec
Setup time, CSB falling edge to SDO / RDYB output data	t7	0	-	30	nsec
Setup time, SCK rising edge to SDO / RDYB output data	t8	0	-	40	nsec
Hold time, SCK falling edge of LSB to SDO / RDYB output data	t9	10	-	50	nsec
Setup time, CSB rising edge to SDO / RDYB changing to HiZ	t10	0	-	30	nsec
Reset time	t_{rstw}	-	-	400	nsec

- The SPI AC timing is shown in the figure below. It is the communication of 5Mbps at the highest speed.
- Capacitance Load of SDO / RDYB terminal is assumed to 40pF



SPI AC timing

■ REGISTER DESCRIPTION

NA2202/2203/2204 has register (list shown below) which can access it through SPI bus.
Registers with different data lengths (2 to 3 bytes) are assigned to 4-Bit register address (0x0 to 0xF).

REGISTER ADDRESS	REGISTER NAME	Data Length [byte]	
		NA2203/2204	NA2202
0x0	CTRL	2-Byte (16-Bit)	
0x1	ADCDATA	3-Byte (24-Bit)	2-Byte (16-Bit)
0x2	IEXCONF	2-Byte (16-Bit)	
0x3	AFECONF	2-Byte (16-Bit)	
0x4	CLKCONF	2-Byte (16-Bit)	
0x5	GPIOCTRL0	2-Byte (16-Bit)	
0x6	GPIOCTRL1	2-Byte (16-Bit)	
0x7	OPTION	2-Byte (16-Bit)	
0x8	GAIN1	3-Byte (24-Bit)	2-Byte (16-Bit)
0x9	GAIN2	3-Byte (24-Bit)	2-Byte (16-bit)
0xA	-	3-Byte (24-Bit)	2-Byte (16-Bit)
0xB	-	3-Byte (24-Bit)	2-Byte (16-Bit)
0xC	OFFSET1	3-Byte (24-Bit)	2-Byte (16-bit)
0xD	OFFSET2	3-Byte (24-Bit)	2-Byte (16-Bit)
0xE	-	3-Byte (24-Bit)	2-Byte (16-Bit)
0xF	-	3-Byte (24-Bit)	2-Byte (16-Bit)

< View of the register table>

REGISTER NAME								
BIT	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
BIT NAME								
R / W								
RESET								

R / W: Bit of attribute (Write or Read)
- R (Read Only) : Read only
- W (Write Only) : Write only (At the time of read, return "0".)
- RW (Read Write) : Read & Write
- RC (Read / Write 1 to Clear bit) : Read returns the register value.
  Writing 1 clears the bit to 0. Writing 0 does not affect the operation.

Reset: Reset value in register
Set to the reset value by SPI reset command and power-on reset.

■ REGISTER DESCRIPTION

CTRL Register

Register Address: 0x0

CTRL								
BIT	[15]	[14]	[13]	[12]	[11]	[10]	[9]	[8]
BIT NAME	CHSELN				CHSELP			
R / W	RW				RW			
RESET	0x4				0x0			
BIT	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
BIT NAME	RDYCNT		RDYB	OV	MODE			
R / W	R		R	R	RW			
RESET	0x0		1	0	0x0			

BIT	BIT NAME	FUNCTION
[15:12]	CHSELN	Analog input channel setting of negative side. Refer the below table: CHSELP / CHSELN Register.
[11:8]	CHSELP	Analog input channel setting of positive side. Refer the below table: CHSELP / CHSELN Register.
[7:6]	RDYCNT	Modulo operation counter. 2-Bit modulo operation counter that adds 1 each time the ADCDATA resister is updated.
[5]	RDYB	Data ready flag. When conversion data is updated, this bit is set to “0”. When ADCDATA read, this bit set to “1”. 0: Conversion completion 1: Conversion non-completion
[4]	OV	Overflow flag. When conversion data is overflow, this bit is set to “1”. When ADCDATA read, this bit is set to “0”. 0: Valid 1: Overflow (Invalid)
[3:0]	MODE	Operation mode setting. When this bit is “write”, sets the operation mode of ADC. When this bit is “read”, returns the current configuration state. Refer the below table : MODE Register

Table 1 CHSELP Bit

CHSELP	Positive
0x0	VIN1P
0x1	VIN1N
0x2	VIN2P
0x3	VIN2N
0x4	VIN3P
0x5	VIN3N
0x6	VIN4P
0x7	VIN4N
0x8	INTVREF
0x9	AVSS
0xA	VREFP
0xB	VREFN
0xC	TEMPP
0xD	TEMPN
0xE	AVDD
0xF	VCOM

CHSELN Bit

CHSELN	Negative
0x0	VIN1P
0x1	VIN1N
0x2	VIN2P
0x3	VIN2N
0x4	VIN3P
0x5	VIN3N
0x6	VIN4P
0x7	VIN4N
0x8	INTVREF
0x9	AVSS
0xA	VREFP
0xB	VREFN
0xC	TEMPP
0xD	TEMPN
0xE	AVDD
0xF	VCOM

Table 2 MODE Bit

MODE	Operation	Processing
0x0	Idle	Waiting state of conversion operation or calibration
0x1	Sleep	Setting the state of low power consumption which conversion operation or calibration is available. Start-up time is inserted automatically before conversion operation.
0x2	Single conversion	Convert once the input channel that is selected in the CHSELP / N. After the conversion, the operation is “Idle (0x0)” state. Using the value of the “OFFSET1, 2” register.
0x3	Continuous conversion	Convert continuous the input channel that is selected in the CHSELP / N. Until the operation is set to "Idle (0x0)", conversion will continue. Using the value of the “OFFSET1, 2” register.
0x4	Single conversion + CHOP	This is the same as “Single conversion (0x2)”, but the data rate is 1/2. Not using the value of the “OFFSET1, 2” register.
0x5	Continuous conversion + CHOP	This is the same as “Continuous conversion (0x3)”, but the data rate is 1/3. Not using the value of the “OFFSET1, 2” register.
0x6	Single conversion + CHOP + IEX CHOP	This is the same as “Single conversion (0x2)”, but the data rate is 1/2. Not using the value of the “OFFSET1, 2” register. CHOP operation is valid. The connection channel of IEX1 and IEX2 is switched in conjunction with the CHOP operation.
0x7	Continuous conversion + CHOP + IEX CHOP	This is the same as “Continuous conversion (0x3)”, but the data rate is 1/3. Not using the value of the “OFFSET1, 2” register. CHOP operation is valid. The connection channel of IEX1 and IEX2 is switched in conjunction with the CHOP operation.
0x8	Not used(15)	-
0x9	Not used(15)	-
0xA	Not used(15)	-
0xB	Not used(15)	-
0xC	Calibration system offset	Input is selected by CHSELP / N, system offset is calibrated.
0xD	Calibration system gain	Input is selected by CHSELP / N, system gain is calibrated.
0xE	Not used(15)	-
0xF	Boot	Read only. It shows the state from the reset to change to “Idle (0x0)”. After the initial setting, automatically shifts to the "Idle (0x0)".

(15) Please do not absolutely use the “Not used” code. It will be the cause of failure.

ADCDATA Register <NA2202>

Register Address 0x1

ADCDATA								
BIT	[15]	[14]	[13]	[12]	[11]	[10]	[9]	[8]
BIT NAME	ADCDATA							
R / W	R							
RESET	-							
BIT	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
BIT NAME	ADCDATA							
R / W	R							
RESET	-							

BIT	BIT NAME	FUNCTION
[15:0]	ADCDATA	Store the converted data of the ADC.(16) Conversion data is expressed as a signed 16-bit. - When the input voltage is negative full-scale, the output is 0x8000 - When the input voltage is zero, the output is 0x0000 - When the input voltage is positive full-scale, the output is 0x7FFF. (in decimal -32768 to +32767)

(16) Relationship of conversion data ADCDATA and the analog input voltage V_{in} is as the following equation.
(It assumed that the offset error and gain error are zero.)

$$ADCDATA = \frac{V_{in}}{2 \times VREF} \times PGAIN1 \times PGAIN2 \times 2^{16} = \frac{V_{in}}{VREF} \times PGAIN1 \times PGAIN2 \times 2^{15}$$

ADCDATA Register <NA2203>

Register Address 0x1

ADCDATA								
BIT	[23]	[22]	[21]	[20]	[19]	[18]	[17]	[16]
BIT NAME	ADCDATA							
R / W	R							
RESET ⊦	-							
BIT	[15]	[14]	[13]	[12]	[11]	[10]	[9]	[8]
BIT NAME	ADCDATA							
R / W	R							
RESET	-							
BIT	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
BIT NAME	ADCDATA				-			
R / W	R				R			
RESET	-				0x0			

BIT	BIT NAME	FUNCTION
[23:4]	ADCDATA	Store the converted data of the ADC.(16) Conversion data is expressed as a signed 20-bit. - When the input voltage is negative full-scale, the output is 0x80000 - When the input voltage is zero, the output is 0x00000 - When the input voltage is positive full-scale, the output is 0x7FFFF. (in decimal -524288 to +524287)

(16) Relationship of conversion data ADCDATA and the analog input voltage Vin is as the following equation.
(It assumed that the offset error and gain error are zero.)

$$ADCDATA = \frac{V_{in}}{2 \times VREF} \times PGAIN1 \times PGAIN2 \times 2^{20} = \frac{V_{in}}{VREF} \times PGAIN1 \times PGAIN2 \times 2^{19}$$

ADCDATA Register <NA2204>

Register Address 0x1

ADCDATA								
BIT	[23]	[22]	[21]	[20]	[19]	[18]	[17]	[16]
BIT NAME	ADCDATA							
R / W	R							
RESET	-							
BIT	[15]	[14]	[13]	[12]	[11]	[10]	[9]	[8]
BIT NAME	ADCDATA							
R / W	R							
RESET	-							
BIT	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
BIT NAME	ADCDATA							
R / W	R							
RESET	-							

BIT	BIT NAME	機能
[23:0]	ADCDATA	Store the converted data of the ADC.(16) Conversion data is expressed as a signed 24-bit. - When the input voltage is negative full-scale, the output is 0x800000 - When the input voltage is zero, the output is 0x000000 - When the input voltage is positive full-scale, the output is 0x7FFFFF. (in decimal -8388608 to +8388607)

(16)Relationship of conversion data ADCDATA and the analog input voltage Vin is as the following equation.
(It assumed that the offset error and gain error are zero.)

$$ADCDATA = \frac{V_{in}}{2 \times VREF} \times PGAIN1 \times PGAIN2 \times 2^{24} = \frac{V_{in}}{VREF} \times PGAIN1 \times PGAIN2 \times 2^{23}$$

IEXCONF Register

Register Address: 0x2

IEXCONF								
BIT	[15]	[14]	[13]	[12]	[11]	[10]	[9]	[8]
BIT NAME	IEX2SLP	-	IEX2C		IEX2_EN	IEX2SW		
R / W	RW	-	RW		RW	RW		
RESET	0	-	0x0		0	0x0		
BIT	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
BIT NAME	IEX1SLP	-	IEX1C		IEX1_EN	IEX1SW		
R / W	RW	-	RW		RW	RW		
RESET	0	-	0		0	0x0		

BIT	BIT NAME	FUNCTION
[15]	IEX2SLP	Condition setting of IEX2 at sleep mode by AUTOSLP bit = “1” of OPTION register. 0: IEX2 current depends on IEX2C 1: IEX2 OFF
[14]	-	-
[13:12]	IEX2C	Current setting of IEX2. 0x0: 100μA 0x1: 250μA 0x2: 500μA 0x3: 1mA 0x4 to 0x7: Not used(16).
[11]	IEX2_EN	Setting ON / OFF of IEX2. 0: IEX2 OFF (Open) 1: IEX2 ON
[10:8]	IEX2SW	Connection setting of IEX2. 0x0: VIN1P 0x4: VIN3P 0x1: VIN1N 0x5: VIN3N 0x2: VIN2P 0x6: VIN4P 0x3: VIN2N 0x7: VIN4N
[7]	IEX1SLP	Condition setting of IEX1 at sleep mode by AUTOSLP bit = “1” of OPTION register. 0: IEX1 current depends on IEX1C 1: IEX1 OFF
[6]	-	-
[5:4]	IEX1C	Current setting of IEX1. 0x0: 100μA 0x1: 250μA 0x2: 500μA 0x3: 1mA 0x4 to 0x7: Not used(15).
[3]	IEX1_EN	Setting ON / OFF of IEX1. 0: IEX1 OFF (Open) 1: IEX1 ON
[2:0]	IEX1SEL	Connection setting of IEX1. 0x0: VIN1P 0x4: VIN3P 0x1: VIN1N 0x5: VIN3N 0x2: VIN2P 0x6: VIN4P 0x3: VIN2N 0x7: VIN4N

(15) Please do not absolutely use the “Not used” code. It will be the cause of failure.

AFECONF Register

Register Address: 0x3

AFECONF								
BIT	[15]	[14]	[13]	[12]	[11]	[10]	[9]	[8]
BIT NAME	LPWEN	-	-	-	BCDIR	BCEN	TEMPEN	INTVREFEN
R / W	RW	-	-	-	RW	RW	RC	RW
RESET	0	-	-	-	0	0	0	0
BIT	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
BIT NAME	VREFSEL[1:0]		PGA2GAIN[1:0]		PGA1EN	PGA1GAIN[2:0]		
R / W	RW		RW		RW	RW		
RESET	0x0		0x0		0	0x0		

BIT	BIT NAME	FUNCTION
[15]	LPWEN	Low power setting. ADC operating clock frequency (FMOD) becomes FMOD = FOSC / 4 regardless of CLKDIV setting. 0: Normal mode 1: Low power mode
[14:12]	-	-
[11]	PCDIR	Burn out current direction setting Burn out current setting BCEN / BCDIR / INPUTP / INPUTN 0 / X / Off / Off 1 / 0 / Source / Sink 1 / 1 / Sink / Source
[10]	BCEN	Burn out current operation setting Please refer Table. Xx (Burn out current)
[9]	TEMPEN	Internal TEMP setting 0: Internal TEMP OFF 1: Internal TEMP ON, TEMPP and TEMPN input are valid.
[8]	INTVREFEN	Internal reference voltage INTVREF setting. It is necessary the operation stabilization time after operating the internal reference voltage circuit. The operation stabilization time depends on the external capacitance connected to INTVREF terminal. 0: External reference voltage VREFP / VREFN 1: Internal reference voltage INTVREF / AVSS
[7:6]	VREFSEL	ADC reference voltage setting. VREFSEL Register VREFSEL[1:0] / REFP / REFN 0x0 / VREFP / VREFN 0x1 / INTVREF / AVSS 0x2 / VIN4P / VIN4N 0x3 / AVDD / AVSS
[5:4]	PGA2GAIN	Gain setting of PGA2 setting 0x0: PGAIN2=1 0x1: PGAIN2=2 0x2: PGAIN2=4 0x3: Use prohibition(15)
[3]	PGA1EN	Gain setting of PGA1 0: PGA1 OFF (PGA1 is power down mode. Input signal to ADC.) 1: PGA1 ON
[2:0]	PGA1GAIN	Gain of PGA1 setting 0x0: PGAIN1=1 0x1: PGAIN1=2 0x2: PGAIN1=4 0x3: PGAIN1=8 0x4: PGAIN1=16 0x5: PGAIN1=21.33 0x6: PGAIN1=32 0x7: Use prohibition(15)

(15) Please do not absolutely use the “Not used” code. It will be the cause of failure.

CLKCONF Register

Register Address: 0x4

CLKCONF								
BIT	[15]	[14]	[13]	[12]	[11]	[10]	[9]	[8]
BIT NAME	-	CLKSEL	CLKDIV		REJ		OSR	
R / W	-	RW	RW		RW		RW	
RESET	-	0	0x0		0x0		0x3	
BIT	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
BIT NAME	OSR							
R / W	RW							
RESET	0xFF							

BIT	BIT NAME	FUNCTION
[15]	-	-
[14]	CLKSEL	Setting of the ADC clock source. The clock selection mode must wait for a given clock start-up time. The clock start-up time differs between internal and external clock selection. 0: Internal oscillator (FOSC=1.2288MHz at typical) FOSC is system clock it is necessary to interval over 100µsec after switching the internal clock. 1: External clock (XT/EXT terminals) System clock frequency fsys is 1/4 of a crystal resonator frequency fext (fsys = fext/4) It is necessary to interval over stabilization time of external clock circuit + 1msec after switching the external clock.
[13:12]	CLKDIV	Setting of the ADC clock frequency (FMOD). Normal setting is CLKDIV=0 Normal Mode: FMOD= fsys/2, Low Power Mode: FMOD=fsys/8

LPWEN	CLKDIV[1:0]	FMOD
0	0	fsys/2
	1	fsys/4
	2	fsys/8
	3	fsys/16
1	0	Fsys/8
	1	Fsys/16
	2	Use prohibition
	3	Use prohibition

(fsys: system clock frequency)

[11:10]	REJ	Setting of the 50/60Hz rejection mode. This bit can be used when OSR[9:0] is set to 0xBF or 0x17F or 0x2FF. 0: Normal operation 1: 50Hz/60Hz rejection mode 2: Use prohibition(15) 3: Use prohibition(15)
[9:0]	OSR	Oversampling ratio setting

(15) Please do not absolutely use the “Not used” code. It will be the cause of failure.
Data rate is derived by the following equation. It will be the data rate of a single conversion.

$$\mathrm{DR} = F_{OSC} \times \frac{1}{64 \times (OSR[9:0]+1)} \times \frac{1}{2^{(CLKDIV[1:0]+1)}} \times \frac{1}{3} = F_{OSC} \times \frac{1}{OSR} \times \frac{1}{2^{(CLKDIV[1:0]+1)}} \times \frac{1}{3}$$

If FOSC is 1.288MHz of (TYP.) conversion data rate will be set in the table below.

OSR	Data Rate [sps]			
	CLKDIV=0(Recommend)	CLKDIV=1(*)	CLKDIV=2(*)	CLKDIV=3(*)
65536	0.003125k	0.0015625k	0.00078125k	0.000390625k
8192	0.025k	0.0125k	0.00625k	0.003125k
1024	0.2k	0.1k	0.05k	0.025k
128	1.6k	0.8k	0.4k	0.2k

(*) Design guarantee.

GPIOCTRL0 Register

Register Address: 0x5

GPIOCTRL0								
BIT	[15]	[14]	[13]	[12]	[11]	[10]	[9]	[8]
BIT NAME	DR							
R / W	RW							
RESET	0X00							
BIT	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
BIT NAME	PORTOUT							
R / W	RW							
RESET	0x00							

BIT	BIT NAME	FUNCTION
[15:8]	DR	Set to output mode of GPIO terminal when the customer uses analog input terminal as a GPIO output. 0: Set the output driver to Hi-Z 1: Output the PORTOUT register level from output driver. GPIO control and PORT configuration Port / PORTOUT / DR / PORTIE / PORTIN - / PORTOUT[0] / DR[0] / PORTIE[0] / PORTIN[0] - / PORTOUT[1] / DR[1] / PORTIE[1] / PORTIN[1] - / PORTOUT[2] / DR[2] / PORTIE[2] / PORTIN[2] - / PORTOUT[3] / DR[3] / PORTIE[3] / PORTIN[3] VIN3P / PORTOUT[4] / DR[4] / PORTIE[4] / PORTIN[4] VIN3N / PORTOUT[5] / DR[5] / PORTIE[5] / PORTIN[5] VIN4P / PORTOUT[6] / DR[6] / PORTIE[6] / PORTIN[6] VIN4N / PORTOUT[7] / DR[7] / PORTIE[7] / PORTIN[7] *These for terminals can use for GPIO: VIN3P, VIN3N, VIN4P, VIN4N
[7:0]	PORTOUT	Set to logic output level of GPIO internal when the customer uses analog input terminal as a GPIO output. 0: Low level output 1: High level output

GPIOCTRL 1 Register

Register Address: 0x6

GPIOCTRL1								
BIT	[15]	[14]	[13]	[12]	[11]	[10]	[9]	[8]
BIT NAME	PORTIE							
R / W	RW							
RESET	0x00							
BIT	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
BIT NAME	PORTIN							
R / W	R							
RESET	0x00							

BIT	BIT NAME	FUNCTION
[15:8]	PORTIE	Set to input of GPIO terminal when the customer uses analog input terminal as a GPIO input 0: Analog Input 1: Logic Input
[7:0]	PORTIN	Return the logic level of GPIO terminal.

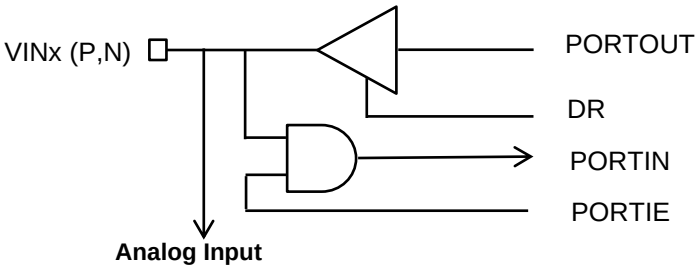


Fig GPIO terminal structure

OPTION Register

Register Address：0x7

OPTION								
BIT	[15]	[14]	[13]	[12]	[11]	[10]	[9]	[8]
BIT NAME	CHIPID							
R / W	R							
RESET	0xA1/ 0xA2/ 0xA3							
BIT	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
BIT NAME	CHIPREV				CEMODE		CE	AUTOSLP
R / W	R				RW		RC	RW
RESET	0x1				0x0		0	1

BIT	BIT NAME	FUNCTION
[15:8]	CHIPID	Used to identify the chip NA2202: 0xA1 NA2203: 0xA2 NA2204: 0xA3
[7:4]	CHIPREV	Used to revision the chip
[3:2]	CEMODE	SPI communication error mode setting 0： No use 1： Use prohibition 2： CRC8 3： Check Sum
[1]	CE	The communication error can be detected if CE MODE[1:0] is set to 2 (CRC8) or 3 (Check Sum) 0: No communication error 1: Communication error (Sticky bit)
[0]	AUTOSLP	When MODE[3:0] is idle (0x0), set to ON / OFF of analog block 0: ON(Wait) 1: OFF(Power down) When the customer changes AUTOSLP from 1 to 0, conversion start is necessary to start-up time of the analog block.

GAIN1 / GAIN2 Register <NA2202>

Register Address: 0x8, 0x9

	GAIN1 / GAIN2															
BIT	[15]	[14]	[13]	[12]	[11]	[10]	[9]	[8]	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
BIT NAME	GAIN															
R / W	RW															
RESET	0x00															

BIT	BIT NAME	FUNCTION
[15:0]	GAIN	Gain coefficient derived in gain calibration. Gain coefficient is 16-bit unsigned coefficient. The customer can do external writing gain coefficient, when operation mode setting is idle status of MODE=0x0 only. Please set to “0” AUTOSLP bit of OPTION0 register. It is necessary to interval over 10 µsec when the customer writes the gain coefficient on this register via SPI.

GAIN1 / GAIN2 Register <NA2203>

Register Address：0x8, 0x9

	GAIN1 / GAIN2																							
BIT	[23]	[22]	[21]	[20]	[19]	[18]	[17]	[16]	[15]	[14]	[13]	[12]	[11]	[10]	[9]	[8]	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
BIT NAME	GAIN																				-			
R / W	RW																				R			
RESET	0x80								0x00								0x0							

BIT	BIT NAME	FUNCTION
[23:4]	GAIN	Gain coefficient derived in gain calibration. Gain coefficient is 20-bit unsigned coefficient. The customer can do external writing gain coefficient, when operation mode setting is idle status of MODE=0x0 only. Please set to “0” AUTOSLP bit of OPTION0 register. It is necessary to interval over 10 µsec when the customer writes the gain coefficient on this register via SPI. Lower 4-bit have not register. (20-bit MSB first)

GAIN1 / GAIN2 Register <NA2204>

Register Address：0x8, 0x9

	GAIN1 / GAIN2																							
BIT	[23]	[22]	[21]	[20]	[19]	[18]	[17]	[16]	[15]	[14]	[13]	[12]	[11]	[10]	[9]	[8]	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
BIT NAME	GAIN																							
R / W	RW																							
RESET	0x80								0x00								0x0							

BIT	BIT NAME	FUNCTION
[23:0]	GAIN	Gain coefficient derived in gain calibration. Gain coefficient is 24-bit unsigned coefficient. The customer can do external writing gain coefficient, when operation mode setting is idle status of MODE=0x0 only. Please set to “0” AUTOSLP bit of OPTION0 register. It is necessary to interval over 10 µsec when the customer writes the gain coefficient on this register via SPI.

OFFSET1 / OFFSET2 Register <NA2202>

Register Address: 0xC, 0xD

	OFFSET1 / OFFSET2															
BIT	[15]	[14]	[13]	[12]	[11]	[10]	[9]	[8]	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
BIT NAME	OFFSET															
R / W	RW															
RESET	0x00															

BIT	BIT NAME	FUNCTION
[15:0]	OFFSET	Offset coefficient derived in offset calibration or the external writing offset coefficient. 16-bit signed coefficient. (17) The customer can do the external writing offset coefficient, when internal clock is active only. In case of writing offset coefficient, please set to "0" AUTOSLP bit of OPTION0 register. After writing to this register, allow at least 10µsec intervals between SPI communications.

(17) Sign - extended: If the sign is (-) fill the 1 in the free space. If the sign is (+) fill the "0" in the free space
- In the case of -4 in decimal 8- bit is “11111100”.
  16-bit sign extension is “11111111 11111100”.
- In the case of +4 in decimal 8-bit is “00000100”
  16-bit sign extension is “00000000 00000100”

OFFSET1 / OFFSET2 Register <NA2203>

Register Address: 0xC, 0xD

	OFFSET1 / OFFSET2																							
BIT	[23]	[22]	[21]	[20]	[19]	[18]	[17]	[16]	[15]	[14]	[13]	[12]	[11]	[10]	[9]	[8]	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
BIT NAME	OFFSET																				-			
R / W	RW																				R			
RESET	0x00								0x00								0x0							

BIT	BIT NAME	FUNCTION
[23:4]	OFFSET	Offset coefficient derived in offset calibration or the external writing offset coefficient. 20-bit signed coefficient. (17) The customer can do the external writing offset coefficient, when internal clock is active only. In case of writing offset coefficient, please set to "0" AUTOSLP bit of OPTION0 register. After writing to this register, allow at least 10µsec intervals between SPI communications. Lower 4-bit have not register. (20-bit MSB first)

(17) Sign - extended: If the sign is (-) fill the 1 in the free space. If the sign is (+) fill the "0" in the free space
- In the case of -4 in decimal 8- bit is “11111100”.
  20-bit sign extension is “1111 111111111 11111100”.
- In the case of +4 in decimal 8-bit is “00000100”
  20-bit sign extension is “0000 00000000 00000100”

OFFSET1 / OFFSET2 Register <NA2204>

Register Address: 0xC, 0xD

	OFFSET1 / OFFSET2																							
BIT	[23]	[22]	[21]	[20]	[19]	[18]	[17]	[16]	[15]	[14]	[13]	[12]	[11]	[10]	[9]	[8]	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
BIT NAME	OFFSET																							
R / W	RW																							
RESET	0x00								0x00								0x00							

BIT	BIT NAME	FUNCTION
[23:0]	OFFSET	Offset coefficient derived in offset calibration or the external writing offset coefficient. 24-bit signed coefficient.(17) The customer can do the external writing offset coefficient, when internal clock is active only. In case of writing offset coefficient, please set to "0" AUTOSLP bit of OPTION0 register. After writing to this register, allow at least 10µsec intervals between SPI communications.

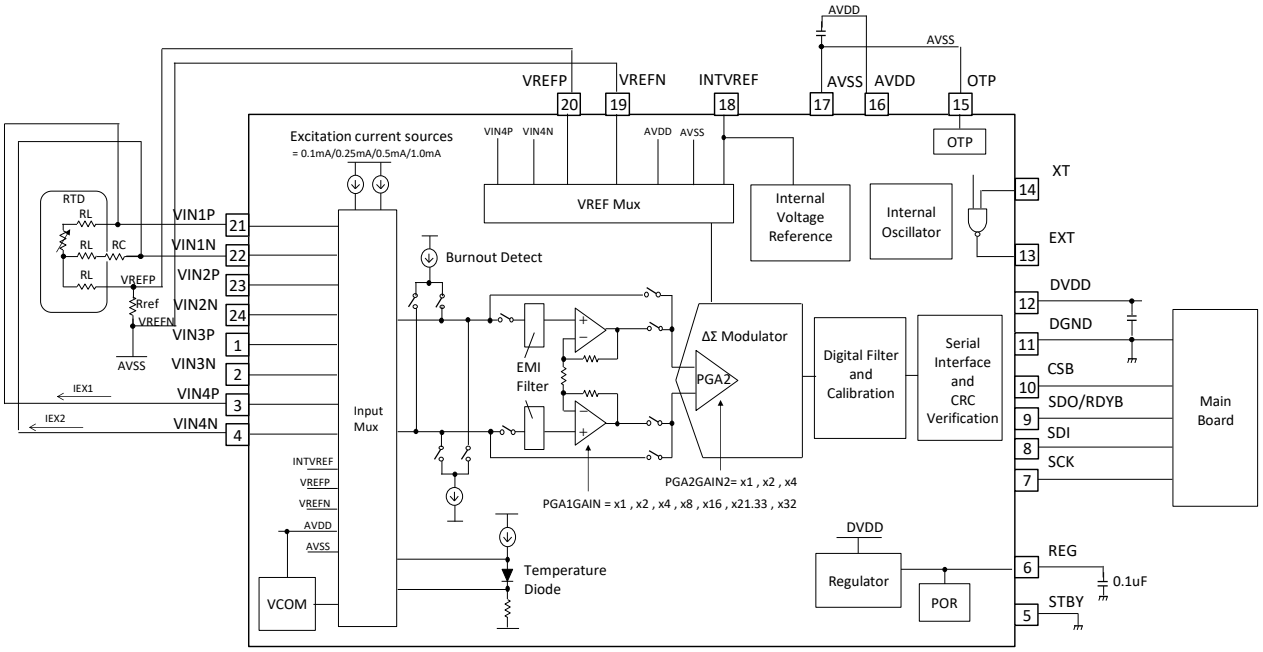
(17) Sign - extended: If the sign is (-) fill the 1 in the free space. If the sign is (+) fill the "0" in the free space
- In the case of -4 in decimal 8- bit is “11111100”.
  24-bit sign extension is “11111111 11111111 11111100”.
- In the case of +4 in decimal 8-bit is “00000100”
  24-bit sign extension is “00000000 00000000 00000100

The GAINn and OFFSETn registers are used for the coefficients used in gain and offset calibration.
“n” is determined by the setting value on the positive input side, CTRL Register 0x0 CHSELP.
Refer the below table: Data Calibration Coefficient Correspondence Table 3.

Table 3 Data Calibration Coefficient Correspondence Table

CHSELP Set Value	Positive	Gain n Register	OFFSET n Register
0x0	VIN1P	GAIN1	OFFSET1
0x1	VIN1N	GAIN1	OFFSET1
0x2	VIN2P	GAIN1	OFFSET1
0x3	VIN2N	GAIN1	OFFSET1
0x4	VIN3P	GAIN2	OFFSET2
0x5	VIN3N	GAIN2	OFFSET2
0x6	VIN4P	GAIN2	OFFSET2
0x7	VIN4N	GAIN2	OFFSET2
0x8	INTVREF	GAIN1	OFFSET1
0x9	AVSS	GAIN1	OFFSET1
0xA	VREFP	GAIN1	OFFSET1
0xB	VREFN	GAIN1	OFFSET1
0xC	TEMPP	GAIN1	OFFSET1
0xD	TEMPN	GAIN1	OFFSET1
0xE	AVDD	GAIN1	OFFSET1
0xF	VCOM	GAIN1	OFFSET1

■ TYPICAL APPLICATION CIRCUIT



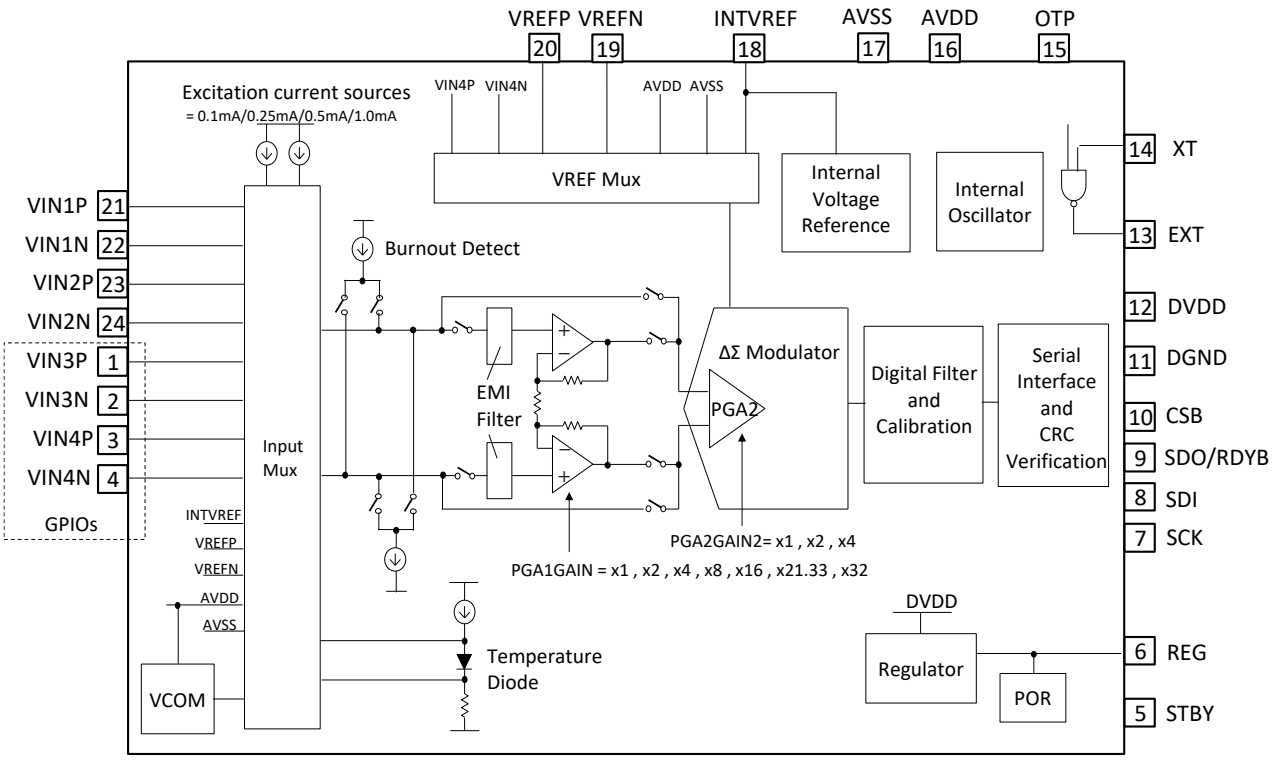
NA2202/03/04 Typical Application Circuit

Notes on External Parts

It is recommended that 5pin (STBY) is connected to ground.
Please Connect a decoupling capacitor (0.1μF) between pin 6 (REG) and DGND terminal. A decoupling capacitor should be connected to ground for stability.
The regulator is optimized for NA2202/2203/2204 operation, so do not connect any components other than the decoupling capacitor.
Please Connect a decoupling capacitor (0.1μF) between pin 12 (DVDD) and pin11 (DGND) terminal.
It is recommended connected the crystal unit (4.9152MHz) between 13pin (EXT) and 14pin (XT) terminals.
Please Connect a decoupling capacitor (0.1μF) between pin 16 (AVDD) and pin 17 (AVSS) terminal.
Connect the 15pin (OTP) to the AVSS terminal.
Connect a 2.2μF decoupling capacitor between the 18pin (INTVREF) and AVSS.
It is recommended to connect a 19PIN (VREFN) to AVSS.

EXT_PAD Connect to AVSS externally.

■ BLOCK DIAGRAMS



NA2202/2203/2204 Block Diagram

■ OPERATING DESCRIPTION

The NA2202/2203/2204 uses a PGA (Programmable Gain Amplifier) to amplify analog signals obtained from sensors and other devices connected to the VIN1P / VIN1N / VIN2P / VIN2N / VIN3P / VIN3N / VIN4P / VIN4N input terminals. Combination of PGA1 / PGA2 can amplify signals up to 128 times. The amplified signal is converted to digital data by a 16/20/24-Bit ΔΣ ADC, and after signal processing such as offset calibration and gain calibration, the digital signal is output to the MCU via SPI communication. A built-in level shifter outputs digital signals at the DVDD level, so it can be connected to a 5V MCU.

In addition, since it can be used with a negative voltage power supply, signals around 0V can be input without being affected by GND noise.

It supports up to 4 inputs in differential mode and up to 8 inputs in single-ended mode.

It has two excitation current sources and can be used for temperature controller applications using resistance temperature detectors.

The reference voltage source for the ADC can be set to either an external reference voltage VREFP / VREFN input externally or an internal reference voltage INT VREF using an internal regulator.

In addition to normal operation mode, low power consumption mode (conversion speed 1/4 and current consumption 1/3 compared to normal operation), sleep mode (OFF except bias and REG circuit), and standby mode (all circuit OFF, current consumption 1μA or less) can be selected.

■ APPLICATION NOTES

TERMINAL DESCRIPTION

- **1pin to 4pin (VIN3P, VIN3N, VIN4P, VIN4N), 21pin to 24pin(VIN1P, VIN1N, VIN2P, VIN2N) Analog Input terminals, GPIO terminals, Current Source Output terminals**

  Analog input terminals for inputting signals from external sources such as sensors.
  It supports up to 4 inputs in differential mode and up to 8 inputs in single-ended mode.
  CHSELP and CHSELN in CTRL register 0x5 select the analog input channel for data conversion (built-in multiplexer function).NA2202/2203/2204 has two excitation current sources to provide a constant current to the sensors. IEXCONF register 0x2 selects the analog input channel to which the excitation current source is connected and the current value can be set.

- **5pin (STBY), Standby terminal**

  Standby terminal. NA2202 /2203 /2204 is in standby mode when STBY = DVDD.

- **6pin (REG), Built-in regulator output terminal for digital power supply**

  NA2202 /2203 /2204 has a built-in regulator for digital power supply. 6pin (REG) is the output terminal.
  A decoupling capacitor should be connected to ground for stability. Place a decoupling capacitor close to 6pin (REG).
  The regulator is optimized for NA2202/2203/2204 operation, so do not connect any components other than the decoupling capacitor.

- **7pin (SCK), Clock terminal**

  Serial Interface, Clock terminal. Digital Input terminal.

- **8pin (SDO/RDYB), Data output / RDYB terminal**

  Serial Interface, Data output /RDYB terminal. Digital output terminal.

- **9pin (SDI), Data input terminal**

  Serial Interface, Digital Input terminal.
  When writing, data to the SDI terminal is communicated MSB first.
  SDI is captured on the falling edge of SCK.

- **10pin (CSB), SPI chip select terminal**

  NA2202/2203/2204 serial interface chip select terminals. Digital input terminal.
  When the CSB terminal is high level, SCK and SDI are disabled and communication is not possible.
  When the CSB terminal is low level, SCK and SDI are enable and communication is possible.
  After the CSB terminal changes from high to low level, the state of the SPI slave interface is reset and command byte must be resent.

- **11pin (DGND), Digital Ground terminal**

  Digital Ground terminal of NA2202/2203/2204.

- **12pin (DVDD), Digital Power Supply terminal**

  Digital Power Supply terminal of NA2202/2203/2204.

- **13pin (EXT), 14pin (XT) Crystal connect terminals**

  Crystal connect terminal (It Recommended connect to Crystal unit: 4.1952MHz)
  When using external clock, Input signal is into 14pin (XT) terminal. 13pin (EXT) is open.

- **15pin (OTP) Writing for OTP power supply terminal**

  User not used. Normally connect to AVSS terminal.

● **16pin (AVDD), Analog Power Supply terminal**

Analog power supply terminal of NA2202/2203/2204.

● **17pin (AVSS), Analog Ground terminal**

Analog ground terminal of NA2202/2203/2204.

● **18pin (INTVREF), Built-in regulator output terminal.**

NA2202/2203/2204 has a built-in regulator for digital power supply. 18pin (INTVREF) is the output terminal.

● **19pin (VREFN), 20pin (VREFP), INTVREF Voltage Input terminals**

Reference voltage input terminals. Negative input / positive input is supported.
Normally, VREFN is connected to AVSS.

■ Power up sequence

When the power supply pin VDD reaches a voltage at which the circuit can operate, the internal reset is released by the built-in power-on reset circuit and initialization begins.
After the reset is released, the startup sequence of the NA2202/2203/2204 are completed after a waiting period of about 600µsec .(The waiting time of about 600µsec does not include the power-on time.)
After the startup sequence is completed, the device transitions to the idle state and is ready for AD conversion operation.

■ Effective resolution, Noise Free Bit (NFB)

Data Rate (DR) is speed at the time of continuous conversion.
Output code variation σ is the effective resolution in the VIN1P connected to (AVDD-AVSS)/2+AVSS, 6.6σ is the NFB.

< Condition >
- FMOD=614.4 kHz
- AVDD=5.0V, AVSS=0V, DVDD=5V, DGND=0V
- VREFP=5.0V, VREFN=0V
- Differential input
- T_a=+25°C

Input referred noise RMS voltage (Vrms) and peak to peak voltage(Vpp) are defined as in Equation below.

・Input referred noise voltage (Vrms) = {2 × (VREFP-VREFN) / PGA Gain} / {2^Effective resolution(bit)}
・Input referred noise voltage(Vpp) = {2 × (VREFP-VREFN) / PGA Gain} / {2^NFB(bit)}

(1) CHOP ON

NA2202 DR vs. Effective resolution (Unit: bit)

OSR	DR [sps]	PGA OFF	PGAON								
			x1	x2	x4	x8	x16	x21.33	x32	x64	x128
65536	3.125	16	16	16	16	16	16	16	16	16	16
32768	6.25	16	16	16	16	16	16	16	16	16	16
16384	12.5	16	16	16	16	16	16	16	16	16	16
8192	25	16	16	16	16	16	16	16	16	16	16
4096	50	16	16	16	16	16	16	16	16	16	16
2048	100	16	16	16	16	16	16	16	16	16	16
1024	200	16	16	16	16	16	16	16	16	16	16
512	400	16	16	16	16	16	16	16	16	16	16
256	800	16	16	16	16	16	16	16	16	16	15.5
128	1600	16	16	16	16	16	16	16	16	16	14.2
64	3200	14.6	14.6	14.6	14.7	14.6	14.6	14.7	14.6	14.7	13

NA2202 DR vs. NFB (Unit: bit)

OSR	DR [sps]	PGA OFF	PGAON								
			x1	x2	x4	x8	x16	x21.33	x32	x64	x128
65536	3.125	16	16	16	16	16	16	16	16	16	16
32768	6.25	16	16	16	16	16	16	16	16	16	16
16384	12.5	16	16	16	16	16	16	16	16	16	16
8192	25	16	16	16	16	16	16	16	16	16	16
4096	50	16	16	16	16	16	16	16	16	16	16
2048	100	16	16	16	16	16	16	16	16	16	15.5
1024	200	16	16	16	16	16	16	16	16	16	15.1
512	400	16	16	16	16	16	16	16	16	15.4	14.5
256	800	16	16	16	16	15.9	15.8	15.8	15.6	15	12.8
128	1600	14.4	14.3	14.3	14.3	14.3	14.2	14,3	14.2	13.9	11.5
64	3200	11.9	11.8	12.0	11.9	11.9	11.9	12	11.9	12	10.3

(2) CHOP OFF

NA2202 DR vs. Effective resolution (Unit: bit)

OSR	DR [sps]	PGA OFF	PGAON								
			x1	x2	x4	x8	x16	x21.33	x32	x64	x128
65536	9.375	16	16	16	16	16	16	16	16	16	16
32768	18.75	16	16	16	16	16	16	16	16	16	16
16384	37.5	16	16	16	16	16	16	16	16	16	16
8192	75	16	16	16	16	16	16	16	16	16	16
4096	150	16	16	16	16	16	16	16	16	16	16
2048	300	16	16	16	16	16	16	16	16	16	16
1024	600	16	16	16	16	16	16	16	16	16	16
512	1200	16	16	16	16	16	16	16	16	16	16
256	2400	16	16	16	16	16	16	16	16	16	15.4
128	4800	16	16	16	16	16	16	16	16	16	13.9
64	9600	14.0	14.2	14.2	14.1	14.3	14.1	14.1	14.2	14.1	12.4

NA2202 DR vs. NFB (Unit: bit)

OSR	DR [sps]	PGA OFF	PGAON								
			x1	x2	x4	x8	x16	x21.33	x32	x64	x128
65536	9.375	16	16	16	16	16	16	16	16	16	16
32768	18.75	16	16	16	16	16	16	16	16	16	16
16384	37.5	16	16	16	16	16	16	16	16	16	16
8192	75	16	16	16	16	16	16	16	16	16	15.9
4096	150	16	16	16	16	16	16	16	16	16	15.4
2048	300	16	16	16	16	16	16	16	16	16	14.9
1024	600	16	16	16	16	16	16	16	16	16	14.4
512	1200	16	16	16	16	16	16	16	15.7	14.9	14
256	2400	15.7	15.6	15.6	15.6	15.5	15.4	15.3	15	14.3	12.6
128	4800	13.8	13.9	13.7	13.7	13.8	13.8	13.8	13.6	13.5	11.2
64	9600	11.3	11.4	11.5	11.4	11.6	11.4	11.4	11.4	11.4	9.7

(3) CHOP ON

NA2203 DR vs. Effective resolution (Unit: bit)

OSR	DR [sps]	PGA OFF	PGAON								
			x1	x2	x4	x8	x16	x21.33	x32	x64	x128
65536	3.125	20	20	20	20	20	20	20	20	20	20
32768	6.25	20	20	20	20	20	20	20	20	20	20
16384	12.5	20	20	20	20	20	20	20	20	20	19.7
8192	25	20	20	20	20	20	20	20	20	20	19.2
4096	50	20	20	20	20	20	20	20	20	19.7	18.7
2048	100	20	20	20	20	20	20	20	20	19.1	18.2
1024	200	20	20	20	20	20	20	19.8	19.5	18.7	17.8
512	400	19.9	19.7	19.7	19.7	19.5	19.5	19.3	19	18.2	17.3
256	800	18.7	18.8	18.8	18.7	18.6	18.5	18.5	18.3	17.7	15.5
128	1600	17.1	17	17	17	17	16.9	17	16.9	16.7	14.2
64	3200	14.6	14.6	14.7	14.6	14.6	14.7	14.7	14.6	14.7	13

NA2203 DR vs. NFB (Unit: bit)

OSR	DR [sps]	PGA OFF	PGAON								
			x1	x2	x4	x8	x16	x21.33	x32	x64	x128
65536	3.125	19.3	19.4	19.3	19.2	19.4	19.3	19.3	19.1	18.5	17.8
32768	6.25	19.2	19.3	19.3	19.2	19.2	19.2	19.1	18.9	18.2	17.3
16384	12.5	19.1	19.2	19.1	19	19	18.9	18.8	18.6	17.8	16.9
8192	25	19	18.8	18.8	18.8	18.7	18.6	18.5	18.2	17.4	16.5
4096	50	18.7	18.6	18.5	18.4	18.5	18.3	18.1	17.7	16.9	16
2048	100	18.4	18.3	18.2	18.1	18.1	17.9	17.7	17.3	16.4	15.5
1024	200	17.7	17.8	17.7	17.7	17.6	17.3	17.1	16.8	16	15.1
512	400	17.1	17	17	16.9	16.8	16.7	16.6	16.3	15.4	14.5
256	800	16	16	16	16	15.9	15.8	15.8	15.6	15	12.8
128	1600	14.4	14.3	14.3	14.3	14.3	14.2	14.3	14.2	13.9	11.5
64	3200	11.9	11.8	12	11.9	11.9	11.9	12	11.9	12	10.3

(4) CHOP OFF

NA2203 DR vs. Effective resolution (Unit: bit)

OSR	DR [sps]	PGA OFF	PGAON								
			x1	x2	x4	x8	x16	x21.33	x32	x64	x128
65536	9.375	20	20	20	20	20	20	20	20	20	19.4
32768	18.75	20	20	20	20	20	20	20	20	20	19.3
16384	37.5	20	20	20	20	20	20	20	20	19.8	18.9
8192	75	20	20	20	20	20	20	20	20	19.3	18.6
4096	150	20	20	20	20	20	20	20	19.8	19.1	18.1
2048	300	20	20	20	20	19.9	19.9	19.8	19.5	18.7	17.6
1024	600	19.9	19.9	19.8	19.8	19.6	19.5	19.4	19.1	18.2	17.2
512	1200	19.3	19.3	19.3	19.1	19.1	18.9	18.8	18.5	17.6	16.8
256	2400	18.4	18.3	18.3	18.3	18.3	18.1	18	17.8	17	15.4
128	4800	16.5	16.6	16.4	16.5	16.6	16.6	16.5	16.4	16.2	13.9
64	9600	14	14.2	14.2	14.1	14.3	14.1	14.1	14.2	14.1	12.4

NA2203 DR vs. NFB (Unit: bit)

OSR	DR [sps]	PGA OFF	PGAON								
			x1	x2	x4	x8	x16	x21.33	x32	x64	x128
65536	9.375	17.9	17.8	18.1	18	17.7	18.1	17.6	18	17.3	16.7
32768	18.75	17.8	17.8	17.6	18	17.9	18	17.7	17.9	17.4	16.6
16384	37.5	17.9	17.8	17.8	17.9	18	17.7	17.6	17.5	17.1	16.2
8192	75	17.9	17.8	17.9	17.8	17.8	17.6	17.3	17.4	16.6	15.9
4096	150	17.9	17.5	17.5	17.7	17.6	17.5	17.3	17.1	16.3	15.4
2048	300	17.5	17.6	17.5	17.4	17.2	17.2	17.1	16.8	16	14.9
1024	600	17.1	17.1	17.1	17	16.8	16.8	16.6	16.4	15.5	14.4
512	1200	16.6	16.6	16.6	16.4	16.4	16.2	16.1	15.7	14.9	14
256	2400	15.7	15.6	15.6	15.6	15.5	15.4	15.3	15	14.3	12.6
128	4800	13.8	13.9	13.7	13.7	13.8	13.8	13.8	13.6	13.5	11.2
64	9600	11.3	11.4	11.5	11.4	11.6	11.4	11.4	11.4	11.4	9.7

(5) CHOP ON

NA2204 DR vs. Effective resolution (Unit: bit)

OSR	DR [sps]	PGA OFF	PGAON								
			x1	x2	x4	x8	x16	x21.33	x32	x64	x128
65536	3.125	22	22.1	22	22	22.1	22	22	21.9	21.2	20.5
32768	6.25	22	22	22	21.9	21.9	21.9	21.8	21.6	20.9	20
16384	12.5	21.8	22	21.9	21.8	21.7	21.7	21.5	21.4	20.5	19.7
8192	25	21.7	21.5	21.6	21.5	21.4	21.3	21.2	20.9	20.1	19.2
4096	50	21.4	21.3	21.2	21.1	21.2	21	20.9	20.4	19.7	18.7
2048	100	21.1	21	20.9	20.8	20.8	20.6	20.4	20	19.1	18.2
1024	200	20.5	20.5	20.5	20.4	20.3	20	19.8	19.5	18.7	17.8
512	400	19.9	19.7	19.7	19.7	19.5	19.5	19.3	19	18.2	17.3
256	800	18.7	18.8	18.8	18.7	18.6	18.5	18.5	18.3	17.7	15.5
128	1600	17.1	17	17	17	17	16.9	17	16.9	16.7	14.2
64	3200	14.6	14.6	14.7	14.6	14.6	14.7	14.7	14.6	14.7	13

NA2204 DR vs. NFB (Unit: bit)

OSR	DR [sps]	PGA OFF	PGAON								
			x1	x2	x4	x8	x16	x21.33	x32	x64	x128
65536	3.125	19.3	19.4	19.3	19.2	19.4	19.3	19.3	19.1	18.5	17.8
32768	6.25	19.2	19.3	19.3	19.2	19.2	19.2	19.1	18.9	18.2	17.3
16384	12.5	19.1	19.2	19.1	19	19	18.9	18.8	18.6	17.8	16.9
8192	25	19	18.8	18.8	18.8	18.7	18.6	18.5	18.2	17.4	16.5
4096	50	18.7	18.6	18.5	18.4	18.5	18.3	18.1	17.7	16.9	16
2048	100	18.4	18.3	18.2	18.1	18.1	17.9	17.7	17.3	16.4	15.5
1024	200	17.7	17.8	17.7	17.7	17.6	17.3	17.1	16.8	16	15.1
512	400	17.1	17	17	16.9	16.8	16.7	16.6	16.3	15.4	14.5
256	800	16	16	16	16	15.9	15.8	15.8	15.6	15	12.8
128	1600	14.4	14.3	14.3	14.3	14.3	14.2	14.3	14.2	13.9	11.5
64	3200	11.9	11.8	12	11.9	11.9	11.9	12	11.9	12	10.3

(6) CHOP OFF

NA2204 DR vs. Effective resolution (Unit: bit)

OSR	DR [sps]	PGA OFF	PGAON								
			x1	x2	x4	x8	x16	x21.33	x32	x64	x128
65536	9.375	20.6	20.5	20.8	20.7	20.4	20.8	20.3	20.7	20	19.4
32768	18.75	20.6	20.6	20.4	20.7	20.6	20.7	20.4	20.6	20.1	19.3
16384	37.5	20.6	20.6	20.5	20.6	20.7	20.4	20.4	20.2	19.8	18.9
8192	75	20.6	20.5	20.6	20.5	20.5	20.4	20.1	20.2	19.3	18.6
4096	150	20.6	20.3	20.3	20.4	20.3	20.2	20	19.8	19.1	18.1
2048	300	20.2	20.3	20.2	20.1	19.9	19.9	19.8	19.5	18.7	17.6
1024	600	19.9	19.9	19.8	19.8	19.6	19.5	19.4	19.1	18.2	17.2
512	1200	19.3	19.3	19.3	19.1	19.1	18.9	18.8	18.5	17.6	16.8
256	2400	18.4	18.3	18.3	18.3	18.3	18.1	18	17.8	17	15.4
128	4800	16.5	16.6	16.4	16.5	16.6	16.6	16.5	16.4	16.2	13.9
64	9600	14	14.2	14.2	14.1	14.3	14.1	14.1	14.2	14.1	12.4

NA2204 DR vs. NFB (Unit: bit)

OSR	DR [sps]	PGA OFF	PGAON								
			x1	x2	x4	x8	x16	x21.33	x32	x64	x128
65536	9.375	17.9	17.8	18.1	18	17.7	18.1	17.6	18	17.3	16.7
32768	18.75	17.8	17.8	17.6	18	17.9	18	17.7	17.9	17.4	16.6
16384	37.5	17.9	17.8	17.8	17.9	18	17.7	17.6	17.5	17.1	16.2
8192	75	17.9	17.8	17.9	17.8	17.8	17.6	17.3	17.4	16.6	15.9
4096	150	17.9	17.5	17.5	17.7	17.6	17.5	17.3	17.1	16.3	15.4
2048	300	17.5	17.6	17.5	17.4	17.2	17.2	17.1	16.8	16	14.9
1024	600	17.1	17.1	17.1	17	16.8	16.8	16.6	16.4	15.5	14.4
512	1200	16.6	16.6	16.6	16.4	16.4	16.2	16.1	15.7	14.9	14
256	2400	15.7	15.6	15.6	15.6	15.5	15.4	15.3	15	14.3	12.6
128	4800	13.8	13.9	13.7	13.7	13.8	13.8	13.8	13.6	13.5	11.2
64	9600	11.3	11.4	11.5	11.4	11.6	11.4	11.4	11.4	11.4	9.7

Data Rate

In NA2202/ 2203/ 2204, the data rate is specified by the following formula. (Continuous conversion)

$$\mathrm{DR} = F_{OSC} \times \frac{1}{64 \times (OSR[9:0]+1)} \times \frac{1}{2^{(CLKDIV[1:0]+1)}} \times \frac{1}{3} = F_{OSC} \times \frac{1}{OSR} \times \frac{1}{2^{(CLKDIV[1:0]+1)}} \times \frac{1}{3}$$

The conversion data rate (DR) (In the table below, FOSC=1228.8kHz, CLKDIV [1:0]=0)

OSR	DR [sps]			
	CLKDIV=0(Recommend)	CLKDIV=1(*)	CLKDIV=2(*)	CLKDIV=3(*)
65536	0.003125k	0.0015625k	0.00078125k	0.000390625k
8192	0.025k	0.0125k	0.00625k	0.003125k
1024	0.2k	0.1k	0.05k	0.025k
128	1.6k	0.8k	0.4k	0.2k

(*) Guaranteed by design evaluation and several points test.

When LPWEN is set to 1, power consumption operation is achieved. The sampling clock frequency of the ΔΣ modulator FMOD at this time is 1/4 of the frequency of normal operation, so the conversion data rate during low-power operation is 1/4 of the conversion data rate during normal operation.

Digital Filter

The digital filter is a third-order Sinc filter with a variable oversampling rate from 64 to 65536. By setting the OSR bit, the oversampling rate can be switched in 64 steps.

The digital filter output is output by filter gain compensation circuitry as a 26-bit signed fixed decimal (Q1.25) at any oversampling rate setting. The ADC input full scale (differential input = -VREF+VREF) is then scaled to the digital filter output value of -0.5+0.5.

When REJ=0, the transfer function of the filter can be expressed by the following equation.

$$\mathrm{H}(z) = \frac{\left(1 - z^{-((OSR+1)\cdot 64)}\right)^3}{(1 - z^{-1})^3} \cdot \frac{1}{\left((OSR+1)\cdot 64\right)^3}$$

50Hz/60Hz rejection mode

When the REJ bit is set to 1, the digital filter valid 50Hz/60Hz rejection mode. However, the 50Hz/60Hz rejection mode can only be set when the value of the OSR bit is 0x0BF, 0x17F, or 0x2FF.

The ADC data rate and notch filter frequency are set as follows:

- When OSR=0x0BF, 1/Tadc = 50[Hz], notch frequency is 50*n[Hz],60*n[Hz] (n=1,2,3,...)
- When OSR = 0x17F, 1/Tadc = 25.5 [Hz], notch frequency is 25.5*n[Hz], 30*n[Hz] (n=1,2,3,...)
- When OSR=0x2FF, 1/Tadc=12.25[Hz], notch frequency is 12.25*n[Hz],15*n[Hz] (n=1,2,3,...)

This setting can reduce the attenuation of commercial frequencies of 50 Hz and 60 Hz more than that of a normal Sinc3 filter.

When REJ=0, the transfer function of the filter can be expressed by the following equation.

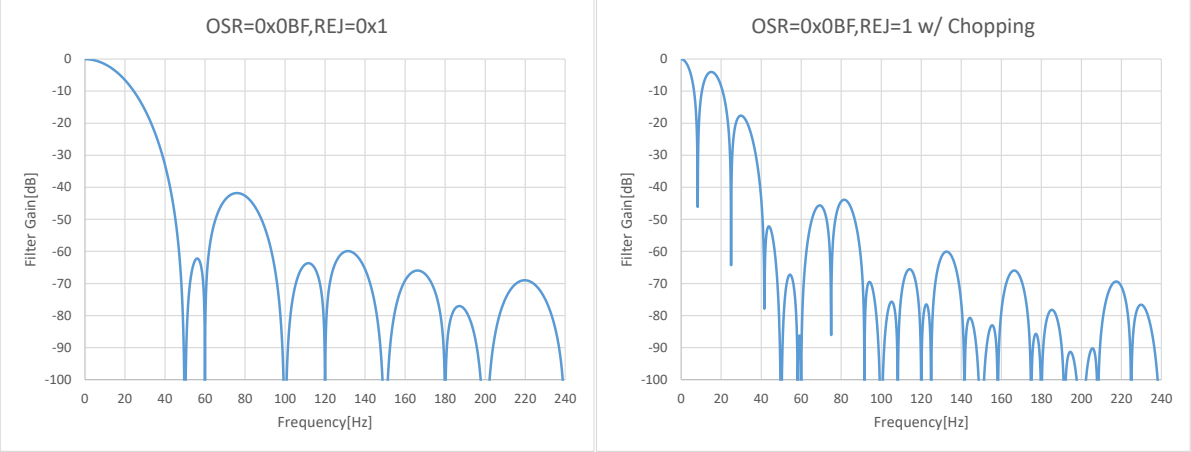
$$\mathrm{H}(z) = \frac{\left(1 - z^{-((OSR+1)\cdot 64)}\right)^2 \cdot \left(1 - z^{-\left((OSR+1)\cdot 64\cdot \frac{5}{6}\right)}\right)}{(1 - z^{-1})^3} \cdot \frac{1}{\left((OSR+1)\cdot 64\right)^2 \cdot \left((OSR+1)\cdot 64 \cdot \frac{5}{6}\right)}$$

If External clock is 4.9152MHz, 50Hz/60Hz rejection in the table below.

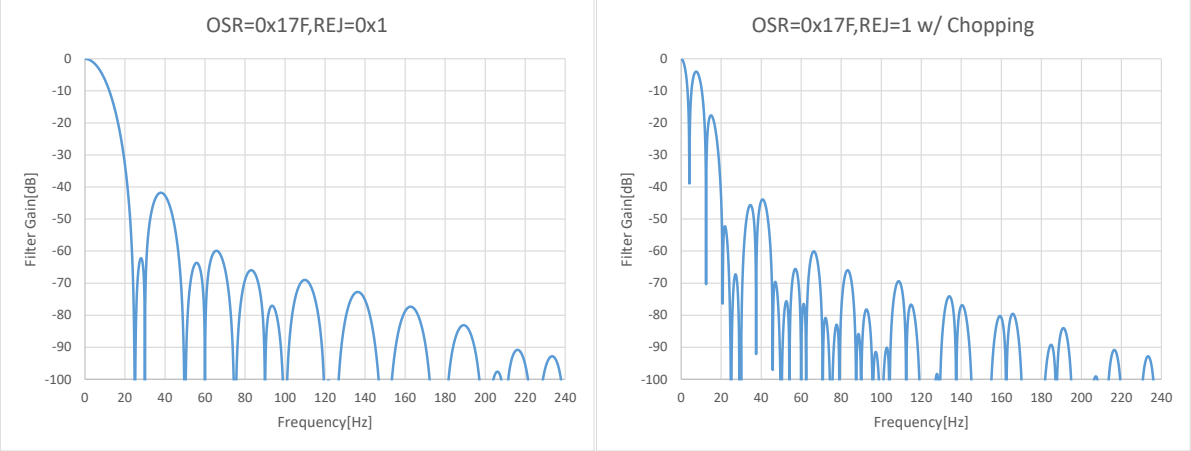
Digital filter setting and 50Hz/60Hz Attenuation.

OSR[9:0]	0x9F	0xBF	0xBF	0x17F	0x2FF	0x3BF
REJ[1:0]	0x0	0x0	0x1	0x1	0x1	0x0
OSR Ratio	10240	12288	12288	24576	49152	61440
Continuous DR 1/Tadc[sps]	60.0	50.0	50.0	25.0	12.5	10.0
50Hz+1Hz Attenuation [dB]	-40.0	-101.4	-81.1	-82.6	-89.5	-101.8
50Hz+2Hz Attenuation[dB]	-37.9	-82.9	-67.6	-69.9	-78.1	-84.6
60Hz+1Hz Attenuation[dB]	-106.3	-46.7	-66.9	-71.4	-86.9	-106.7
60Hz+2Hz Attenuation[dB]	-87.8	-45.3	-60.0	-65.6	-77.8	-89.5

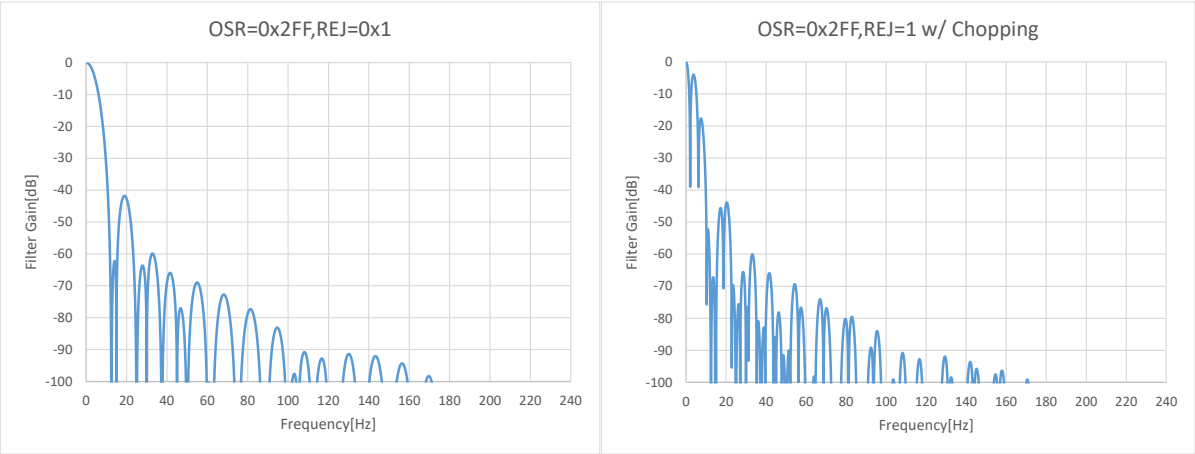
■ Digital filter frequency characteristics



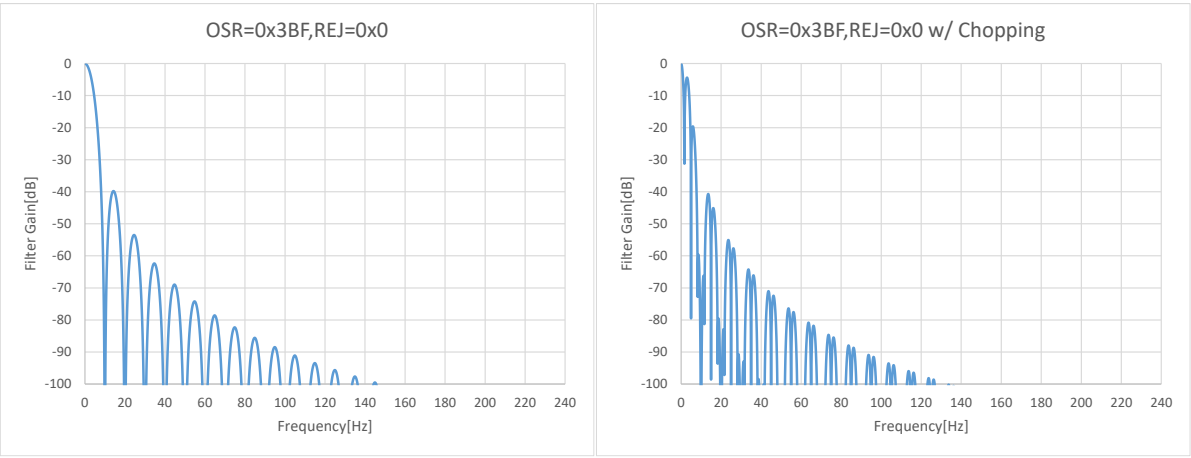
Digital filter frequency example_1(OSR=0x0BF, REJ=1)



Digital filter frequency example_2(OSR=0x17F, REJ=1)



Digital filter frequency example_3(OSR=0x2FF, REJ=1)



Digital filter frequency example_4(OSR=0x3BF, REJ=1)

If Internal OSC(FOSC=1.228MHz±3%) is used, 50Hz/60Hz rejection in the table below.

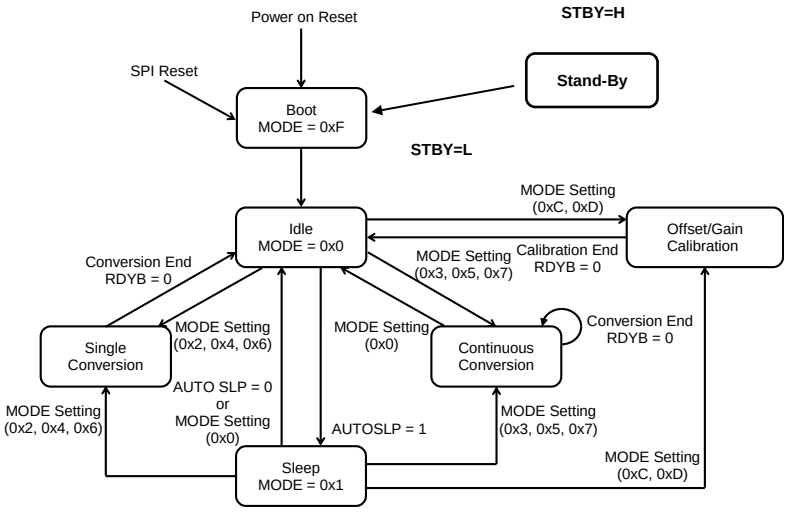
Digital filter setting and 50Hz/60Hz Attenuation. (FOCS=1.2288MHz±3%)

OSR[9:0]	0x9F	0xBF	0xBF	0x17F	0x2FF	0x3BF
REJ[1:0]	0x0	0x0	0x1	0x1	0x1	0x0
OSR Ratio	10240	12288	12288	24576	49152	61440
Continuous DR 1/Tadc[sps]	60.0	50.0	50.0	25.0	12.5	10.0
50Hz+1Hz Attenuation [dB]	-36.8	-77.6	-64.0	-66.2	-74.5	-80.1
50Hz+2Hz Attenuation[dB]	-34.7	-68.4	-57.2	-59.9	-70.6	-73.4
60Hz+1Hz Attenuation[dB]	-79.5	-44.2	-56.3	-62.8	-73.9	-82.7
60Hz+2Hz Attenuation[dB]	-71.2	-43.1	-53.1	-61.0	-70.6	-77.1

■ Conversion Control

Set the conversion operation by MODE bit of CTRL register.

MODE	OPERATION
0x0	Idle
0x1	Sleep
0x2	Single conversion
0x3	Continuous conversion
0x4	Single conversion + CHOP
0x5	Continuous conversion + CHOP
0x6	Single conversion + CHOP + IEX CHOP
0x7	Continuous conversion + CHOP + IEX CHOP
0x8, 0x9 0xA, 0xB	Not used
0xC	Calibration system offset
0xD	Calibration system gain
0xE	Not used
0xF	Boot



< Definition of time >

(1) ADC conversion time of basic : T_{adc} (sec)

Tadc = {(OSR[9:0]+1)*64}/FMOD [s]

OSR : Over Sampling Rate
FMOD: Clock Frequency of ADC

(2) Calculation time for data correction (after ADC conversion) : T_{cal} (sec)

Tcal = 92/Fsys [S] = 75[µs]

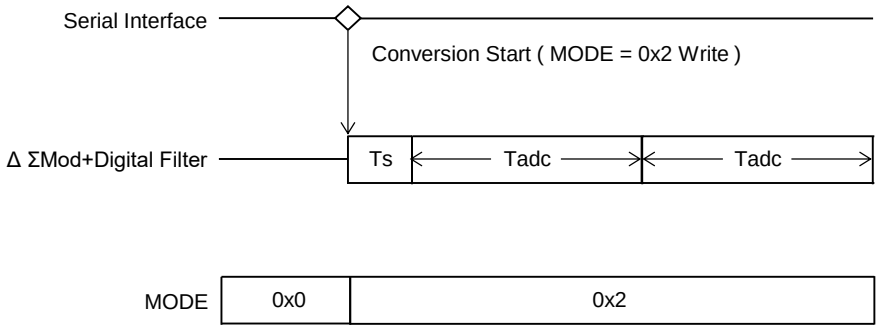
Fsys : Clock Frequency of Internal Oscillator

(3) Calculation time for gain coefficient (after gain calibration) : T_{div} (sec)

Tdiv = 88/Fsys[S] = 72[µS]

(4) Setup time : T_s

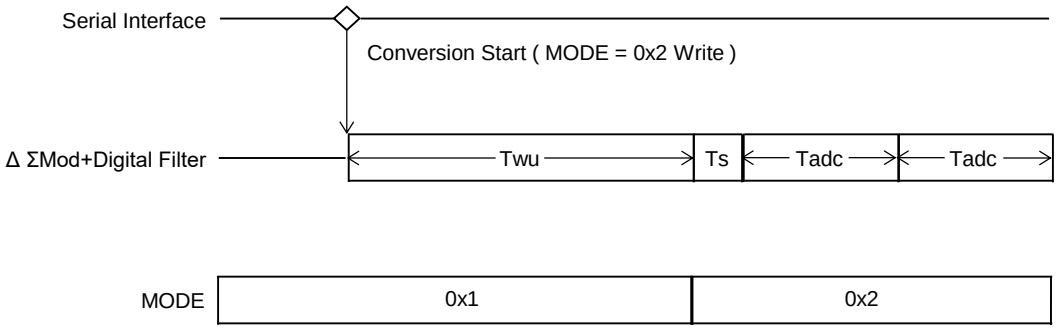
When the analog block is ON (AUTOSLP bit of OPTION 0 register = "0"), setting the MODE bit in CTRL register to operation mode starts operation after T_s (about 10µsec). The case where the MODE bit is switched from "Idle (0x0)" to "single conversion (0x2)" is shown below.



Setup time AUTOSLP=0

(5) Startup wait time : T_{wu}

Waiting time of T_{wu} (about 70µsec) is required when changing the analog block from OFF to ON (AUTOSLP bit from "1" to "0"). The figure below shows the case where the MODE bit is switched from "sleep (0x1)" to "single conversion (0x2)".

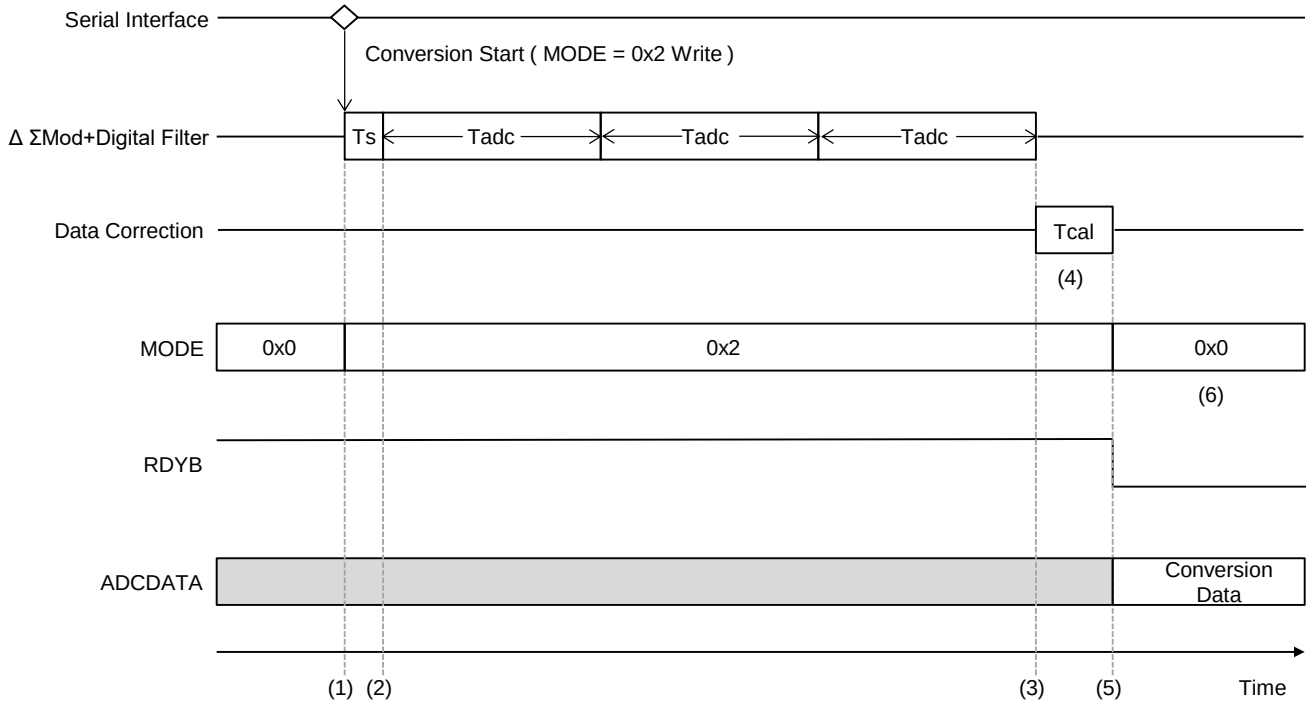


Startup wait time AUTOSLP=1

Single Conversion operation (MODE = 0x2)

It is the basic conversion of NA2202/ 2203/ 2204.
Even if the input signal is switched by the multiplexer (external), waiting time for converted data is unnecessary.
(1 settling, zero latency)

When the conversion cycle is long, the recommended usage is that converting once and power-down the remaining period. So, the consumption current of NA2202/ 2203/ 2204 can be reduced. It is the optimum conversion method for "switching input signals with multiplexer" and "low power consumption".



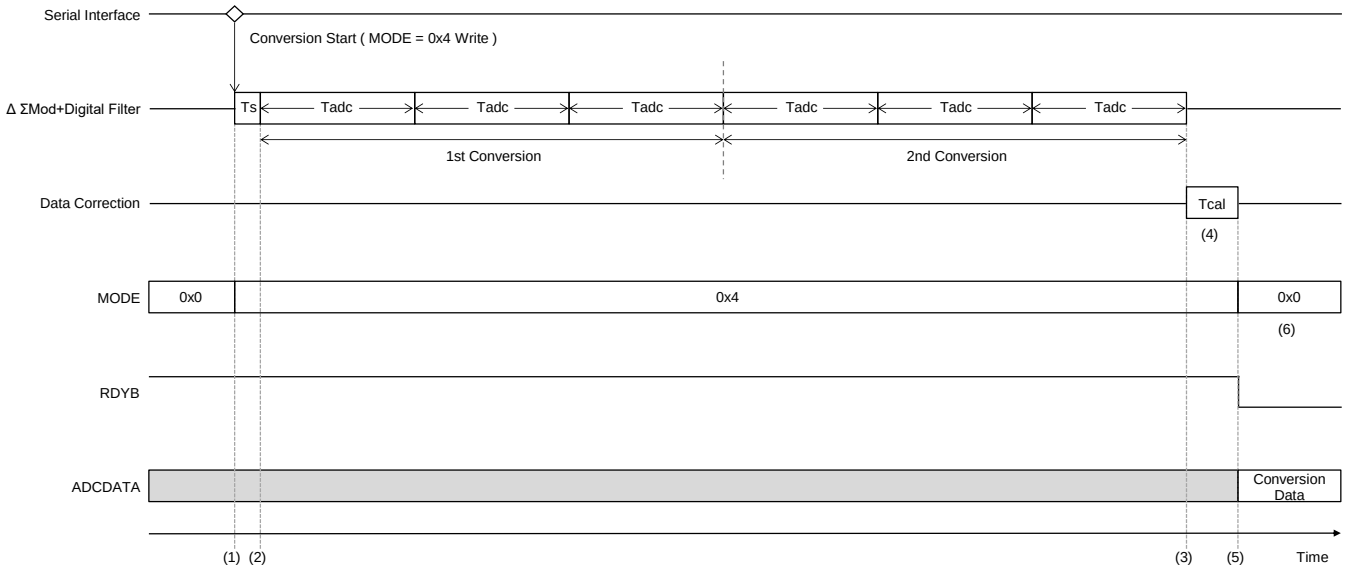
Single conversion timing

STEP	DETAILS
(1)	Set to single conversion. (MODE bit in CTRL register = "0x2")
(2)	After the set-up time (T_s), start the conversion.
(3)	Conversion completed with conversion time (3 x T_{adc}). The conversion data is the result of the convolution integration of 3 x T_{adc}. (ΔΣ Mod + Digital Filter)
(4)	Data is corrected with calculation time (T_{cal}).
(5)	Conversion data stored in ADCDATA register. At that time, RDYB bit changes from "1" to "0".
(6)	Shift to Idle state. (MODE bit= ”0x0”)

“Single conversion + CHOP” operation (MODE = 0x4)

Single conversion performs single conversion twice. By change VINxP and VINxN at the second conversion, the NA2202/2203/2204 offset can be removed in real time. The change of VINxP and VINxN is done automatically by the internal switch.

With single conversion, it is the optimum conversion method for "when you want to calibrate the offset in real time". Though, the data rate is half of single conversion.



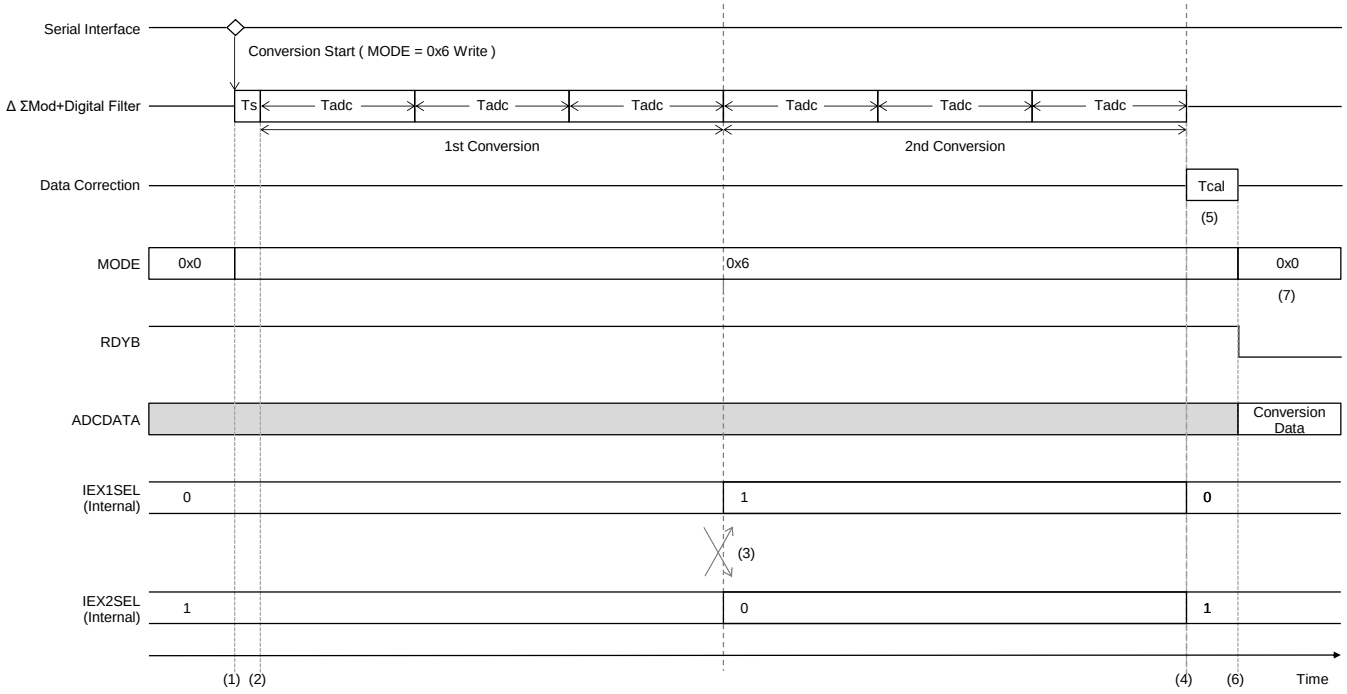
Single conversion + CHOP timing

STEP	DETAILS
(1)	Set to single conversion + CHOP. (MODE bit in CTRL register = "0x4")
(2)	After the set-up time (T_s), start the conversion.
(3)	Conversion completed in conversion time (6 x T_{adc}). The conversion data is the result of the convolution integration of 6 x T_{adc}. (1st & 2nd conversion of "ΔΣ Mod + Digital Filter".)
(4)	Data is corrected in calculation time (T_{cal}).
(5)	Conversion data stored in ADCDATA register. At that time, RDYB bit changes from "1" to "0".
(6)	Shift to Idle state. (MODE bit= ”0x0”)

“Single conversion + CHOP + IEX CHOP” operation (MODE = 0x6)

Single conversion performs single conversion twice. By change VINxP and VINxN at the second conversion, the NA2202/ 2203/ 2204 offset can be removed in real time. The change of VINxP and VINxN is done automatically by the internal switch. The excitation current setting is automatically switched in conjunction with the CHOP operation.

With single conversion, it is the optimum conversion method for "when you want to measure 3-wire RTD with high accuracy". Though, the data rate is half of single conversion.



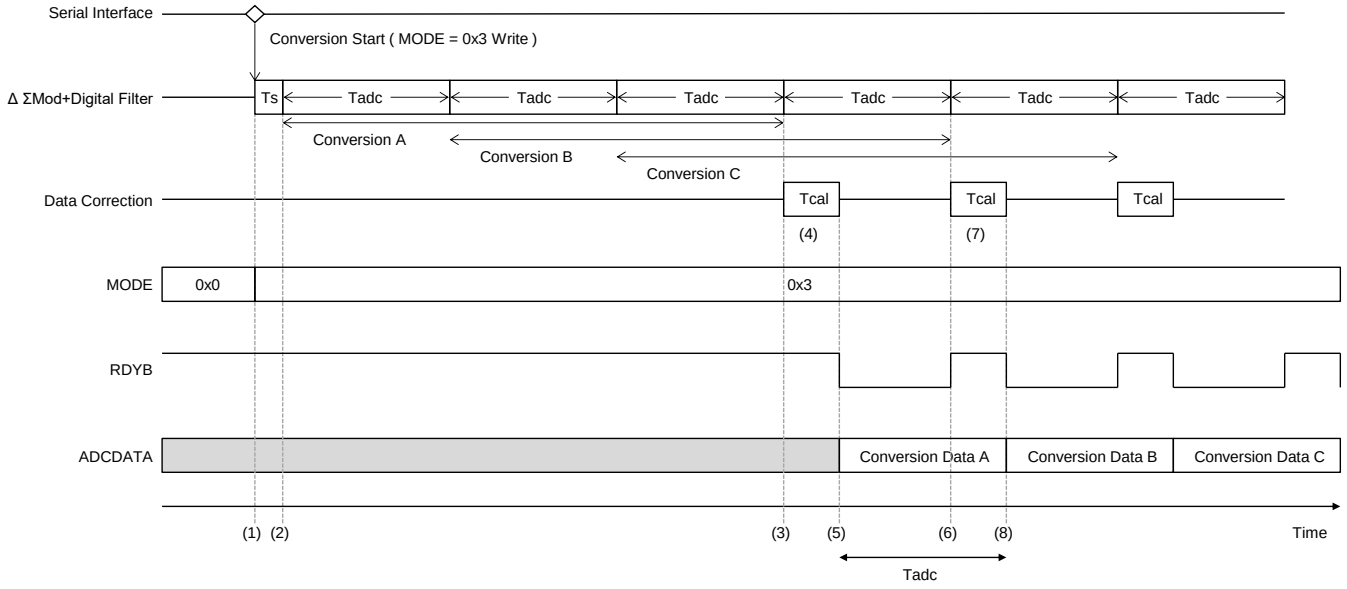
Single conversion + CHOP + IEX CHOP timing

STEP	DETAILS
(1)	Set to single conversion + CHOP + IEX CHOP. (MODE bit in CTRL register = "0x6")
(2)	After the set-up time (T_s), start the conversion.
(3)	The setting IEX1SEL / IEX2SEL of the excitation current source is switched in conjunction with the CHOP operation that switches the input polarity in the second conversion.
(4)	Conversion completed in conversion time (6 x T_{adc}). The conversion data is the result of the convolution integration of 6 x T_{adc}. (1st & 2nd conversion of "ΔΣ Mod + Digital Filter".)
(5)	Data is corrected in calculation time (T_{cal}).
(6)	Conversion data stored in ADCDATA register. At that time, RDYB bit changes from "1" to "0".
(7)	Shift to Idle state. (MODE bit= ”0x0”)

Continuous conversion operation (MODE = 0x3)

When input signals are switched by the multiplexer, the same waiting time as the first conversion (conversion A) is required. When input signal is not switched by multiplexer, wait time after the second conversion (conversion B) is unnecessary.

It is the optimum conversion method for "when input is not switched by multiplexer" and "when you want to maximize data rate". The data rate is three times that of single conversion.



Continuous conversion timing

STEP	DETAILS
(1)	Set to continuous conversion. (MODE bit in CTRL register = "0x3")
(2)	After the set-up time (T_s), start the conversion.
(3)	Conversion A (1'st) completed in conversion time (3 x T_{adc}). The conversion data A is the result of the convolution integration of conversion A ("3 x T_{adc}" of ΔΣ Mod + Digital Filter")
(4)	Data is corrected in calculation time (T_{cal})
(5)	Conversion data A (1'st) stored in ADCDATA register. At that time, RDYB bit changes from "1" to "0".
(6)	After completion of conversion B (2'nd), RDYB bit changes from "0" to "1". The conversion data B is the result of the convolution integration of conversion B ("3 x T_{adc}" of ΔΣ Mod + Digital Filter)
(7)	Data is corrected in calculation time (T_{cal}).
(8)	Conversion data B (2'nd) stored (overwrite) in ADCDATA register. At that time, RDYB bit changes from "1" to "0".

Repeat steps (5) to (8) until the operation mode is set to idle (MODE bit is set to "0x0").
After the conversion stops, a wait time of 3μsec or more is required to start the next conversion.

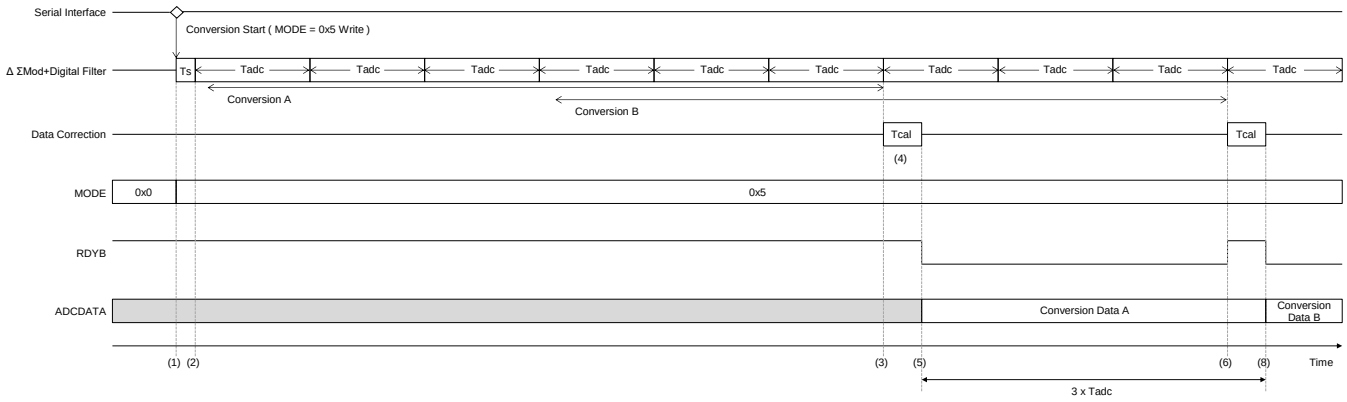
“Continuous conversion + CHOP” operation (MODE = 0x5)

By changing VINxP and VINxN every "3 x T_{adc}", the NA2202/2203/2204 offset can be removed in real time. The change of VINxP and VINxN is done automatically by the internal switch.

When input signals are switched by the multiplexer, the same waiting time as the first conversion (conversion A) is required. When input signal is not switched by multiplexer, wait time after the second conversion (conversion B) is unnecessary.

As with “single conversion + CHOP” operation, offset of whole chip can be calibrated in real time.

It is the optimal conversion method for "when you want to calibrate offsets in real time" with continuous conversion. Though, the data rate is 1/3 of continuous conversion. (Same data rate as single conversion)



Continuous conversion + CHOP timing

STEP	DETAILS
(1)	Set to continuous conversion + CHOP. (MODE bit in CTRL register = "0x5")
(2)	After the set-up time (T_S), start the conversion.
(3)	Conversion A (1’st) completed in conversion time (6 x T_{adc}). The conversion data A is the result of the convolution integration of conversion A (“6 x T_{adc}” of ΔΣ Mod + Digital Filter”)
(4)	Data is corrected in calculation time (T_{cal}).
(5)	Conversion data A (1’st) stored in ADCDATA register. At that time, RDYB bit changes from "1" to "0".
(6)	After completion of conversion B (2’nd), RDYB bit changes from "0" to "1". The conversion data B is the result of the convolution integration of conversion B (“6 x T_{adc}” of ΔΣ Mod + Digital Filter)
(7)	Data is corrected in calculation time (T_{cal}).
(8)	Conversion data B (2’nd) stored (overwrite) in ADCDATA register. At that time, RDYB bit changes from "1" to "0".

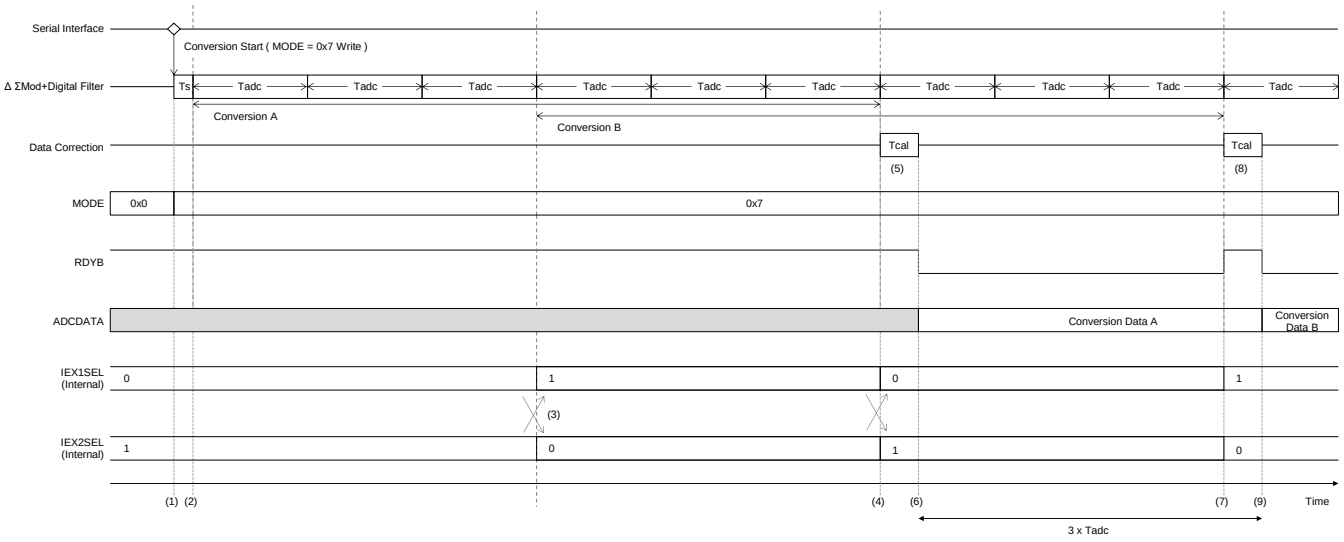
Repeat steps (5) to (8) until the operation mode is set to idle (MODE bit is set to "0x0").
After the conversion stops, a wait time of 3µsec or more is required to start the next conversion.

“Continuous conversion + CHOP + IEX CHOP” operation (MODE = 0x7)

By changing VINxP and VINxN every "3 x T_{adc}", the NA2200/ 2203/ 2204 offset can be removed in real time. The change of VINxP and VINxN is done automatically by the internal switch.
The excitation current setting is automatically switched in conjunction with the CHOP operation.

When input signals are switched by the multiplexer, the same waiting time as the first conversion (conversion A) is required. When input signal is not switched by multiplexer, wait time after the second conversion (conversion B) is unnecessary.

As with “single conversion + CHOP” operation, offset of whole chip can be calibrated in real time.



Continuous conversion + CHOP +IEX CHOP timing

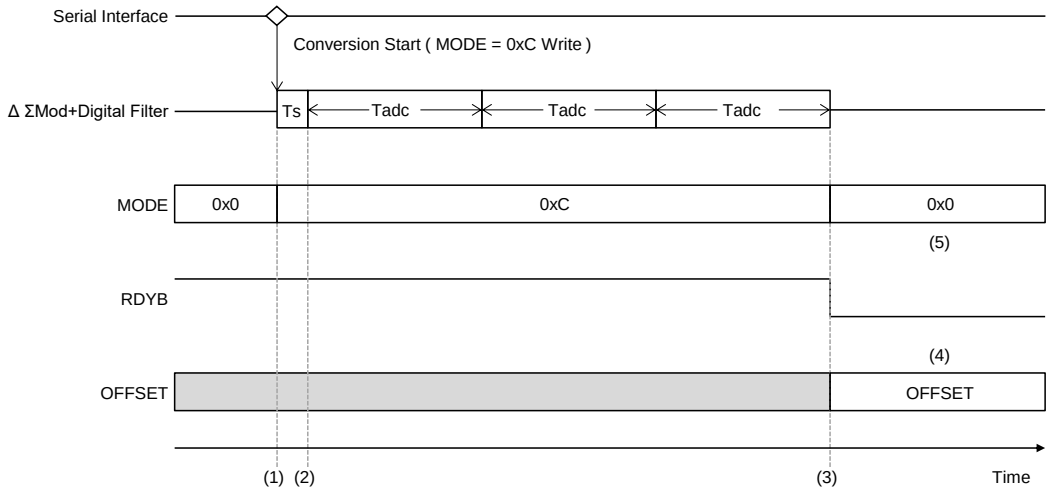
STEP	DETAILS
(1)	Set to continuous conversion + CHOP + IEX CHOP. (MODE bit in CTRL register = "0x7")
(2)	After the set-up time (T_s), start the conversion.
(3)	The setting IEX1SEL / IEX2SEL of the excitation current source is switched in conjunction with the CHOP operation that switches the input polarity in the conversion time (3 x T_{adc}).
(4)	Conversion A (1’st) completed in conversion time (6 x T_{adc}). The conversion data A is the result of the convolution integration of conversion A (“6 x T_{adc}” of ΔΣ Mod + Digital Filter”)
(5)	Data is corrected in calculation time (T_{cal}).
(6)	Conversion data A (1’st) stored in ADCDATA register. At that time, RDYB bit changes from "1" to "0".
(7)	After completion of conversion B (2’nd), RDYB bit changes from "0" to "1". The conversion data B is the result of the convolution integration of conversion B (“6 x T_{adc}” of ΔΣ Mod + Digital Filter) The setting IEX1SEL / IEX2SEL of the excitation current source is switched.
(8)	Data is corrected in calculation time (T_{cal}).
(9)	Conversion data B (2’nd) stored (overwrite) in ADCDATA register. At that time, RDYB bit changes from "1" to "0".

Repeat steps (6) to (9) until the operation mode is set to idle (MODE bit is set to "0x0").
After the conversion stops, a wait time of 3μsec or more is required to start the next conversion.

With continuous conversion, it is the optimum conversion method for "when you want to measure 3-wire RTD with high accuracy". Though, the data rate is 1/3 of continuous conversion. (Same data rate as single conversion)

Offset calibration operation (MODE = 0xC)

Timing is almost the same as single conversion operation.
Calculate the offset amount and save it in the OFFSET register (OFFSET1, OFFSET2).



Offset calibration timing

STEP	DETAILS
(1)	Set to offset calibration. (MODE bit in CTRL register = “0xC”)
(2)	After the set-up time (T_s), start the conversion.
(3)	Conversion is complete in conversion time (3 xT_{adc}).
(4)	Conversion data stored in OFFSET register (OFFSET1, OFFSET2). At that time, RDYB bit changes from "1" to "0".
(5)	Shift to Idle state. (MODE bit= ”0x0”)

For offset calibration, use the CHSELP / CHSELN bits in the CTRL register to select the input channel.
In addition, select the REF_INT_EN bit in the OPTION0 register.

When the offset calibration command is executed, the following processing is automatically performed.

- Using the input channel selected by the CHSELP / CHSELN bit, AD conversion is performed with the reference voltage source of the ADC selected by the REF_INT_EN bit of the OPTION0 register, and the offset is calculated.
- Store calculated offset in OFFSET registers.

The example of internal ADC offset calibration.

(1) REF_INT_EN = 0 (ADC reference voltage = external reference VREFP / VREFN used)

When setting the following PGA gains and input channels, and the offset calibration command is executed, the offset calibration is performed.

- Set PGA1 to OFF (PGA1EN = 0x0) and set the PGA2 gain to “x1” (PGA2GAIN = 0x0).
- Applying VREFN internally to the positive and negative inputs of the ADC. (CHSELP = 0xB, CHSELN = 0xB)
- Calculate the offset.
- Store calculated offset in OFFSET registers.

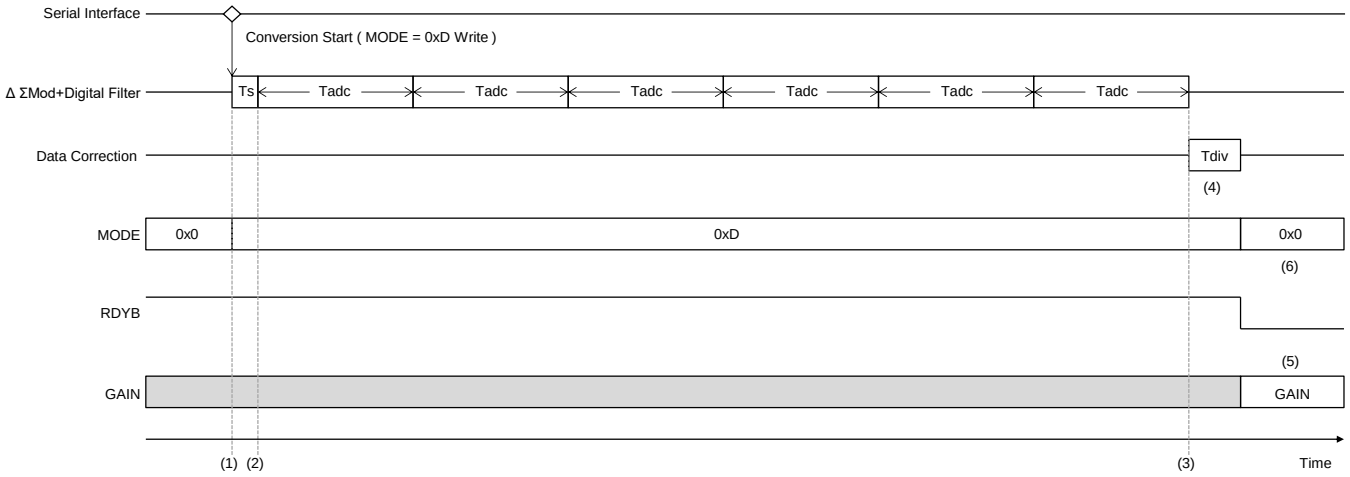
(2) REF_INT_EN = 1 (ADC reference voltage = internal reference INT VREF / AVSS used)

When setting the following PGA gains and input channels, and the offset calibration command is executed, the offset calibration is performed.

- Set PGA1 to OFF (PGA1EN = 0x0) and set the PGA2 gain to “x1” (PGA2GAIN = 0x0).
- Applying AVSS internally to the positive and negative inputs of the ADC. (CHSELP = 0x9, CHSELN = 0x9)
- Calculate the offset.
- Store calculated offset in OFFSET registers.

Gain calibration operation (MODE = 0xD)

Timing is almost the same as “single conversion + CHOP” operation.
Calculate the gain factor and save it in the GAIN register (GAIN1, GAIN2).



Gain calibration timing

STEP	DETAILS
(1)	Set to gain calibration. (MODE bit in CTRL register = “0xD”)
(2)	After the set-up time (T_s), start the conversion.
(3)	Conversion is complete in conversion time (6 xT_{adc}).
(4)	The slope (gain) coefficient is calculated in the gain coefficient calculation time (T_{div}).
(5)	The GAIN registers (GAIN 1, GAIN 2) are updated. At that time, RDYB bit changes from "1" to "0".
(6)	Shift to Idle state. (MODE bit= ”0x0”)

For gain calibration, use the CHSELP / CHSELN bits in the CTRL register to select the input channel.
In addition, select the REF_INT_EN bit in the OPTION0 register.

When the gain calibration command is executed, the following process is automatically performed.

- Using the input channel selected by the CHSELP / CHSELN bit, AD conversion is performed with the reference voltage source of the ADC selected by the REF_INT_EN bit of the OPTION0 register, and the gain coefficient is calculated.
- Store calculated gain coefficient in GAIN registers.

The example of internal ADC gain calibration.

(3) REF_INT_EN = 0 (ADC reference voltage = external reference VREFP / VREFN used)

When setting the following PGA gains and input channels, and the gain calibration command is executed, the gain calibration is performed.

- Set PGA1 to OFF (PGA1EN = 0x0) and set the PGA2 gain to “x1” (PGA2GAIN = 0x0).
- Applying VREF internally to the positive and negative inputs of the ADC.
  (CHSELP = 0xA, CHSELN = 0xB)
- Calculate the gain coefficient.
- Store calculated gain coefficient in GAIN registers.

(4) REF_INT_EN = 1 (ADC reference voltage = internal reference INTVREF / AVSS used)

When setting the following PGA gains and input channels, and the gain calibration command is executed, the gain calibration is performed.

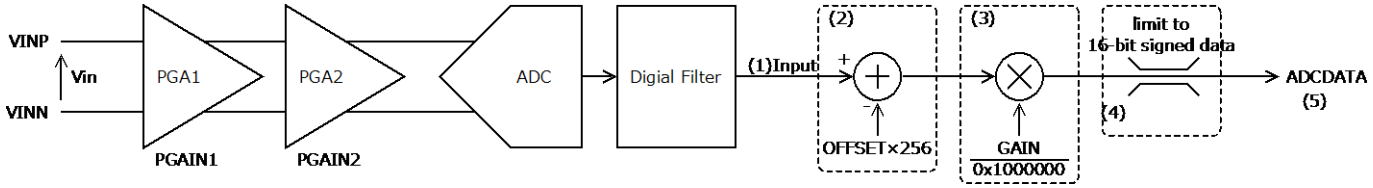
- Set PGA1 to OFF (PGA1EN = 0x0) and set the PGA2 gain to “x1” (PGA2GAIN = 0x0).
- Applying INTVREF and AVSS internally to the positive and negative inputs of the ADC.
  (CHSELP = 0x8, CHSELN = 0x9)
- Calculate the gain coefficient.
- Store calculated gain coefficient in GAIN registers.

■ Data Calibration Flow / Combination of conversion operation and calibration operation <NA2202>

"Data calibration flow" and "Combination of conversion operation and calibration operation" are explained.

Single conversion or Continuous conversion

The figure below is a calibration flow block diagram of "single conversion" or "continuous conversion".
The offset calibration uses the value of the OFFSET register (OFFSET1, OFFSET2).
The gain calibration uses the values of the GAIN register (GAIN1, GAIN2).



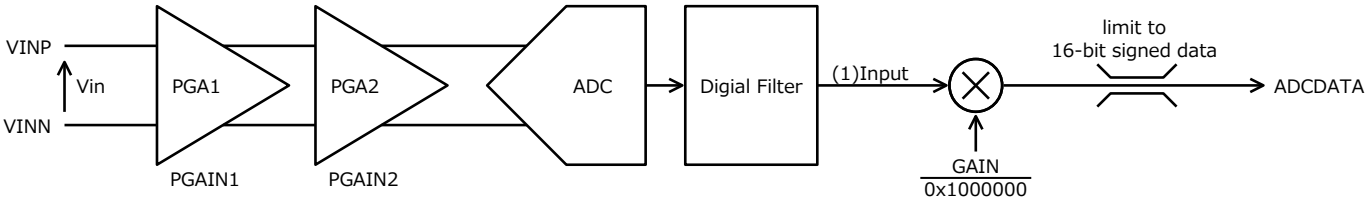
STEP	DETAILS
(1)	"Input" is the following value for the input voltage V_{in}. The full scale of the digital filter is two times signed 24 bits (16777216 = 8388608 x 2). $\text{Input} = \frac{V_{in}}{VREF} \times PGAIN1 \times PGAIN2 \times 16777216$
(2)	Subtract "OFFSETx256" calculated by offset calibration operation from "Input".
(3)	Multiply the result of step (2) by "GAIN" calculated by the gain calibration operation. In order to convert to signed 16-bit full scale, 1 / (0x1000000) is also multiplied.
(4)	Confirm whether "-32768 ≤ (3) result ≤ +32768" is satisfied. If it is not satisfied, set the OV bit of the CTRL register to "1". If it is satisfied, set the OV bit of the CTRL register to "0".
(5)	Store the calculation result in the ADCDATA register. If "OV=1" in step (4), the ADCDATA register is the minimum value (-32768) or the maximum value (+32767). $\text{ADCDATA} = (Input - OFFSET \times 256) \times \frac{GAIN}{0x1000000}$ $= \left(\frac{V_{in}}{VREF} \times PGAIN1 \times PGAIN2 \times 16777216 - OFFSET \times 256\right) \times \frac{GAIN}{0x1000000}$

(Example) When applying PGAIN1 = PGAIN2 = 1, OFFSET = 0, GAIN = 0x10000, VREF = 3.3V, V_{in} = 1V,
--> ADCDATA code is "9930"

$$\text{ADCDATA} = \left(\frac{1V}{3.3V} \times 1 \times 1 \times 16777216 - 0\right) \times \frac{0x8000}{0x1000000} = 9930$$

“Single conversion + CHOP” or “Continuous conversion + CHOP”

The figure below is a block diagram of the calibration flow of "single conversion + CHOP" or "continuous conversion + CHOP".
Since offset is removed by CHOP operation, the offset register value is not used for offset calibration.
Otherwise, it is the same operation as "1. Single conversion or Continuous conversion" on the previous page.



“Single conversion + CHOP + IEX CHOP” or “Continuous conversion + CHOP + IEX CHOP”

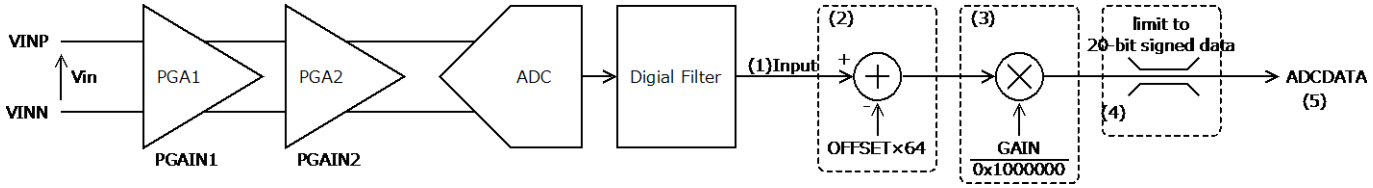
“Single conversion + CHOP + IEX CHOP” or “Continuous conversion + CHOP + IEX CHOP” replaces the excitation current source in conjunction with CHOP operation
Otherwise, it is the same operation as "2. Single conversion + CHOP or Continuous conversion + CHOP".

■ Data Calibration Flow / Combination of conversion operation and calibration operation <NA2203>

"Data calibration flow" and "Combination of conversion operation and calibration operation" are explained.

Single conversion or Continuous conversion

The figure below is a calibration flow block diagram of "single conversion" or "continuous conversion".
The offset calibration uses the value of the OFFSET register (OFFSET1, OFFSET2).
The gain calibration uses the values of the GAIN register (GAIN1, GAIN2).



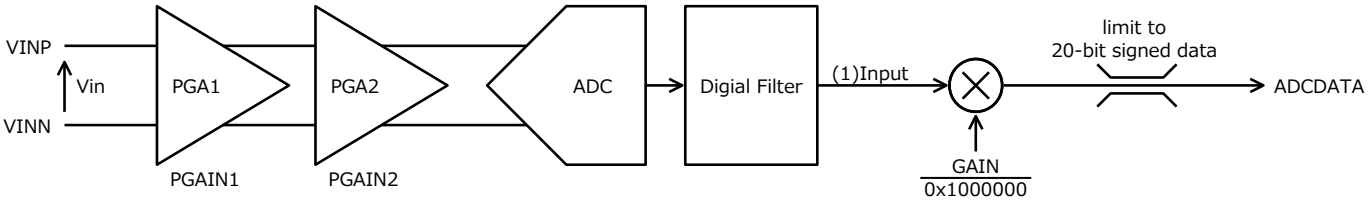
STEP	DETAILS
(1)	"Input" is the following value for the input voltage V_{in}. The full scale of the digital filter is two times signed 24 bits (16777216 = 8388608 x 2). $\text{Input} = \frac{V_{in}}{VREF} \times PGAIN1 \times PGAIN2 \times 16777216$
(2)	Subtract "OFFSETx64" calculated by offset calibration operation from "Input".
(3)	Multiply the result of step (2) by "GAIN" calculated by the gain calibration operation. In order to convert to signed 20-bit full scale, 1 / (0x1000000) is also multiplied.
(4)	Confirm whether "-524288 ≤ (3) result ≤ +524287" is satisfied. If it is not satisfied, set the OV bit of the CTRL register to "1". If it is satisfied, set the OV bit of the CTRL register to "0".
(5)	Store the calculation result in the ADCDATA register. If "OV=1" in step (4), the ADCDATA register is the minimum value (-524288) or the maximum value (+524287). $\text{ADCDATA} = (Input - OFFSET \times 64) \times \frac{GAIN}{0x1000000}$ $= \left(\frac{V_{in}}{VREF} \times PGAIN1 \times PGAIN2 \times 16777216 - OFFSET \times 64\right) \times \frac{GAIN}{0x1000000}$

(Example) When applying PGAIN1 = PGAIN2 = 1, OFFSET = 0, GAIN = 0x10000, VREF = 3.3V, V_{in} = 1V,
--> ADCDATA code is "158875"

$$\text{ADCDATA} = \left(\frac{1V}{3.3V} \times 1 \times 1 \times 16777216 - 0\right) \times \frac{0x80000}{0x1000000} = 158875$$

“Single conversion + CHOP” or “Continuous conversion + CHOP”

The figure below is a block diagram of the calibration flow of "single conversion + CHOP" or "continuous conversion + CHOP".
Since offset is removed by CHOP operation, the offset register value is not used for offset calibration.
Otherwise, it is the same operation as "Single conversion or Continuous conversion" on the previous page.



“Single conversion + CHOP + IEX CHOP” or “Continuous conversion + CHOP + IEX CHOP”

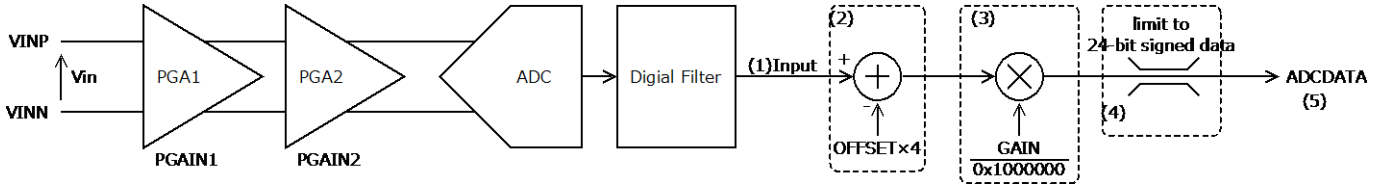
“Single conversion + CHOP + IEX CHOP” or “Continuous conversion + CHOP + IEX CHOP” replaces the excitation current source in conjunction with CHOP operation
Otherwise, it is the same operation as "Single conversion + CHOP or Continuous conversion + CHOP".

■ Data Calibration Flow / Combination of conversion operation and calibration operation <NA2204>

"Data calibration flow" and "Combination of conversion operation and calibration operation" are explained.

Single conversion or Continuous conversion

The figure below is a calibration flow block diagram of "single conversion" or "continuous conversion".
The offset calibration uses the value of the OFFSET register (OFFSET1, OFFSET2).
The gain calibration uses the values of the GAIN register (GAIN1, GAIN2).



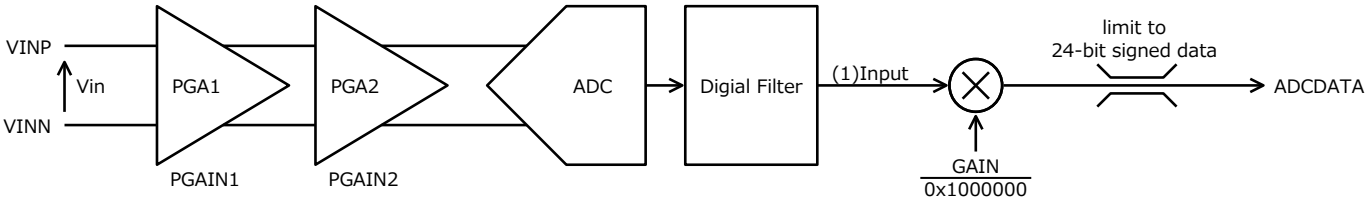
STEP	DETAILS
(1)	"Input" is the following value for the input voltage V_{in}. The full scale of the digital filter is two times signed 24 bits (1677216 = 8388608 x 2). $\text{Input} = \frac{V_{in}}{VREF} \times PGAIN1 \times PGAIN2 \times 16777216$
(2)	Subtract "OFFSETx4" calculated by offset calibration operation from "Input".
(3)	Multiply the result of step (2) by "GAIN" calculated by the gain calibration operation. In order to convert to signed 24-bit full scale, 1 / (0x1000000) is also multiplied.
(4)	Confirm whether "-8388608 ≤ (3) result ≤ +8388607" is satisfied. If it is not satisfied, set the OV bit of the CTRL register to "1". If it is satisfied, set the OV bit of the CTRL register to "0".
(5)	Store the calculation result in the ADCDATA register. If "OV=1" in step (4), the ADCDATA register is the minimum value (-8388608) or the maximum value (+8388607). $\text{ADCDATA} = (Input - OFFSET \times 4) \times \frac{GAIN}{0x1000000}$ $= \left(\frac{V_{in}}{VREF} \times PGAIN1 \times PGAIN2 \times 16777216 - OFFSET \times 4\right) \times \frac{GAIN}{0x1000000}$

(Example) When applying PGAIN1 = PGAIN2 = 1, OFFSET = 0, GAIN = 0x10000, VREF = 3.3V, V_{in} = 1V,
--> ADCDATA code is "2542002"

$$\text{ADCDATA} = \left(\frac{1V}{3.3V} \times 1 \times 1 \times 16777216 - 0\right) \times \frac{0x800000}{0x1000000} = 2542002$$

“Single conversion + CHOP” or “Continuous conversion + CHOP”

The figure below is a block diagram of the calibration flow of "single conversion + CHOP" or "continuous conversion + CHOP".
Since offset is removed by CHOP operation, the offset register value is not used for offset calibration.
Otherwise, it is the same operation as "1. Single conversion or Continuous conversion" on the previous page.



“Single conversion + CHOP + IEX CHOP” or “Continuous conversion + CHOP + IEX CHOP”

“Single conversion + CHOP + IEX CHOP” or “Continuous conversion + CHOP + IEX CHOP” replaces the excitation current source in conjunction with CHOP operation
Otherwise, it is the same operation as "2. Single conversion + CHOP or Continuous conversion + CHOP".

■ SPI Interface [NA2202/2203/2204]

The interface is 4-wire SPI communication of CSB, SCK, SDI, SDO / RDYB. In case, CSB fixed to GND, NA2200 can use as 3-wire SPI communication device.

When CSB is “1”, SCK and SDI are invalid. SDO / RDYB becomes high impedance.
After CSB changes from “1” to “0”, SPI communication always starts with a command byte.
When CSB is “0”, SCK and SDI become valid, and these can communicate.

SDI is captured on the falling edge of SCK and SDO / RDYB is synchronized with the rising edge of SCK.
Bits are transferred in order from the MSB.

SPI communication is performed as follows.

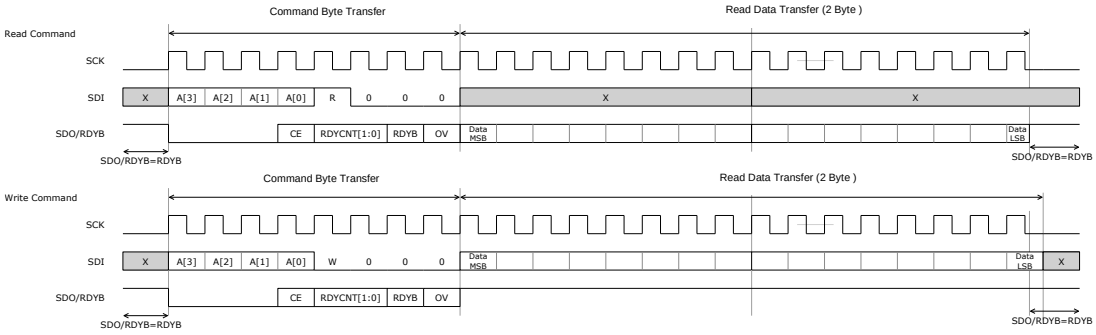
Step	DETAILS
(1)	Command byte transfer
(2)	Read or write data transfer (2 byte or 3 byte data transfer)

When the data transfer is completed, it waits for the command byte.
When SPI communication is not in progress, the RDYB bit value of the CTRL register is output from SDO / RDYB.
RDYB bit outputs "1" or "0" depending on the ADC operation state. (1: Conversion in progress, 0: Conversion end)

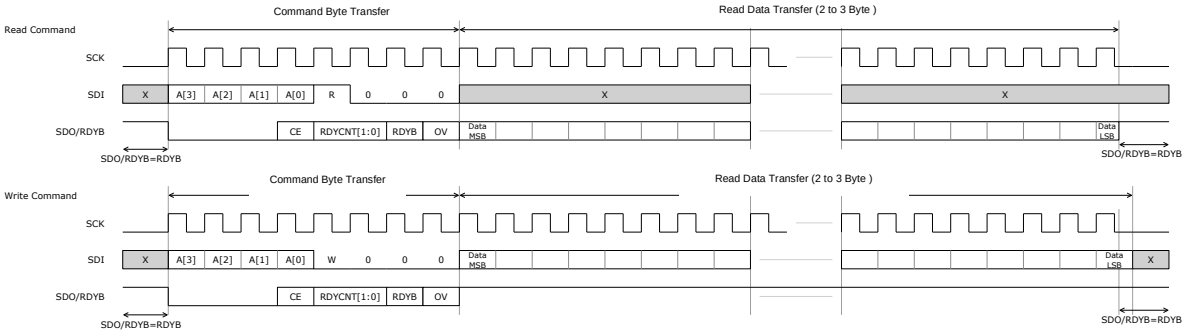
The above state is supplied from the NA2202/2203/2204 to the master device (microcomputer and others).
Therefore, the master device can confirm the conversion end without monitoring the NA2202/2203/2204 periodically.

< Reading / Writing >

NA2202

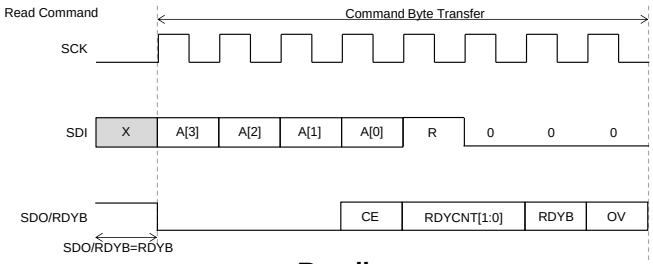


NA2203/NA2204

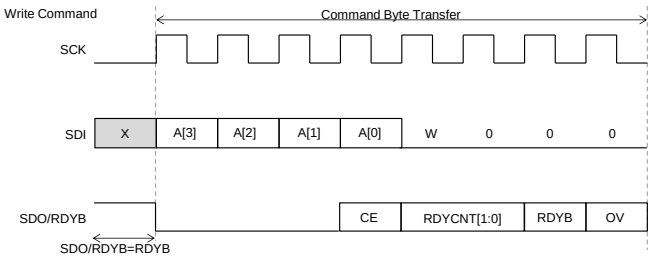


SPI communication format

SPI command byte



Reading



Writing

Read command (Byte)

BIT	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
BIT NAME	-	-	-	CE	RDYCNT		RDYB	OV
R / W	-	-	-	R	R		R	R
VALUE	0	0	0	-	-		-	-

BIT	BIT NAME	FUNCTION
[7:5]	-	-
[4]	CE	Returns the same value as the CE bit of the OPTION0 register
[3:2]	RDYCNT	Returns the same value as the RDYCNT bit of the CTRL register
[1]	RDYB	Returns the same value as the RDYB bit of the CTRL register
[0]	OV	Returns the same value as the OV bit of the CTRL register

Write command (Byte)

BIT	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
BIT NAME	A				RW	ZERO		
R / W	W				W	W		
VALUE	-				-	0		

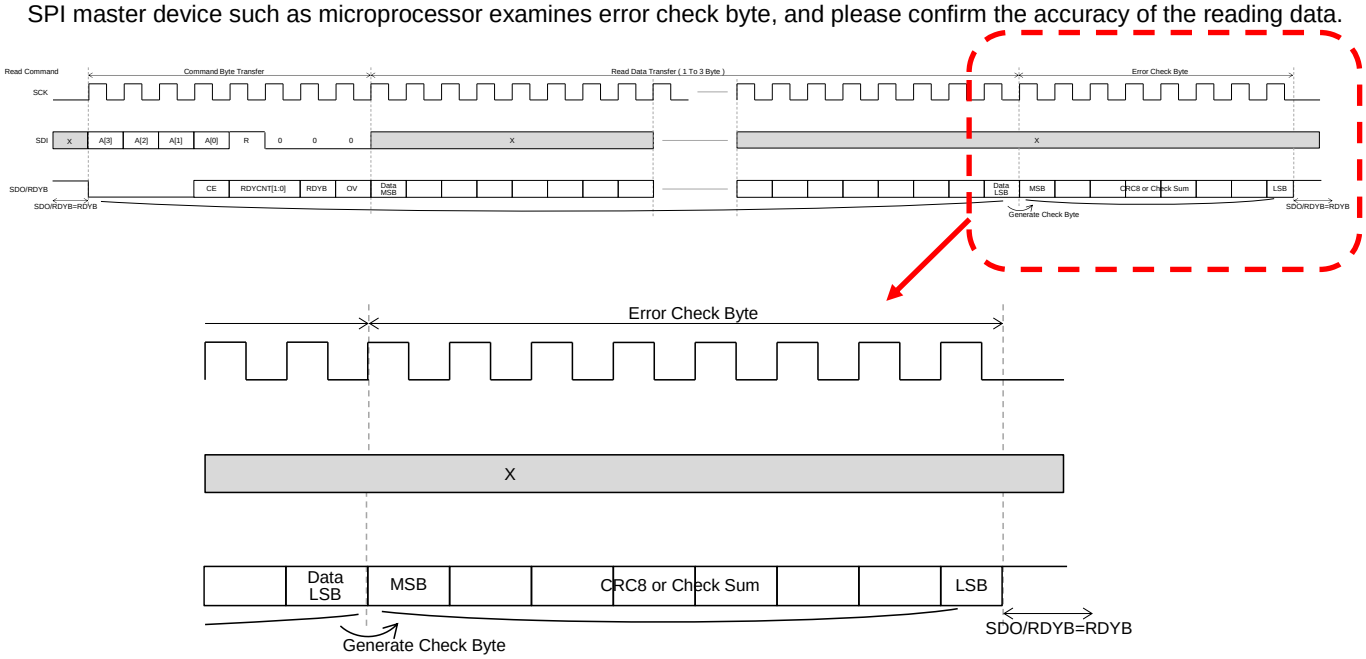
BIT	BIT NAME	FUNCTION
[7:4]	A	Specify the register address to be accessed.
[3]	RW	Specify the direction of communication. (Write or Read) 0: Write 1: Read
[2:0]	ZERO	Always write "0"

SPI communication error detection

SPI communication error detection is valid, in case CEMODE bit of the OPTION0 register (Register address: 0x7) sets to CRC8 mode or Check Sum mode.
When the communication error detection is enable, one byte of Error check byte is added after read or write data transfer.

Read mode

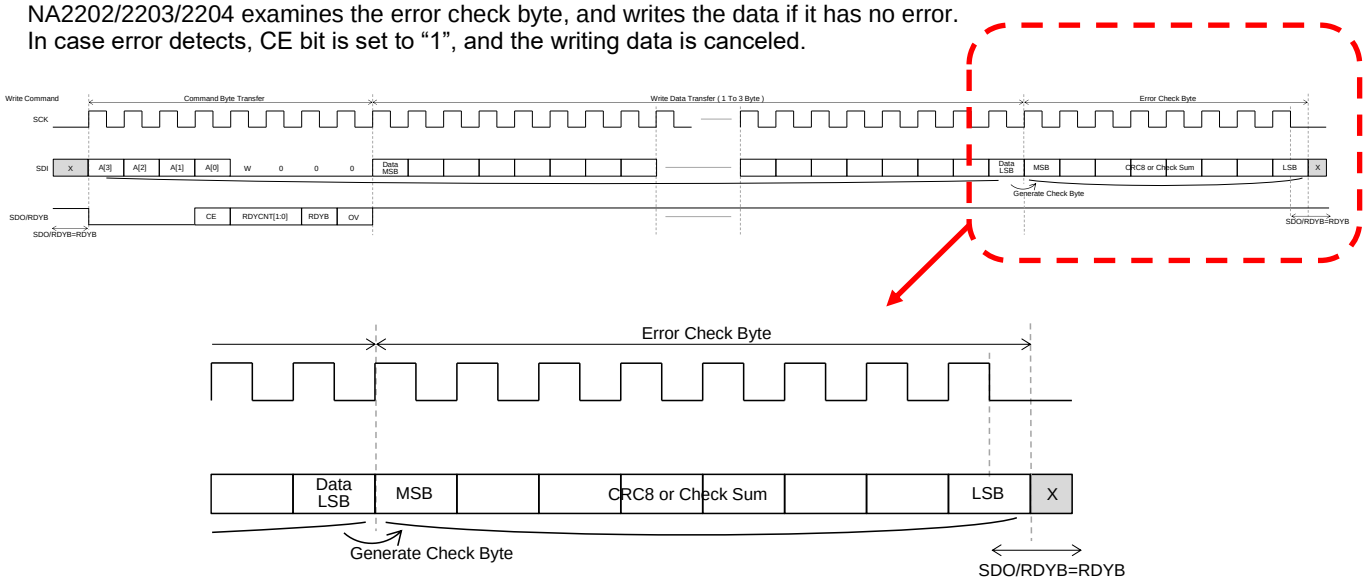
NA2202/2203/2204 outputs the error check byte, after calculating CRC8 or Check Sum from command byte and reading data.
SPI master device such as microprocessor examines error check byte, and please confirm the accuracy of the reading data.



SPI communication format with error check byte: Reading

Write mode

Write the data by adding CRC8 or Check Sum to the command byte and the writing data bytes.
NA2202/2203/2204 examines the error check byte, and writes the data if it has no error.
In case error detects, CE bit is set to “1”, and the writing data is canceled.



SPI communication format with error check byte: Writing

CRC8 mode

Generally, CRC has a stronger error check function than Check Sum, though it has a large MCU source because of a complex calculation.

Error check byte with CRC8 mode is CRC-8-ATM (x^8+x^2+x+1).
Initial value is 0xFF.
In case data has 3 bytes, calculating as follow.

Step	DESCRIPTION
(1)	It takes Ex-OR of “MSB byte of data” and ”Initial value: 0xFF”. (MSB: Most Significant Bit, XOR: Exclusive OR)
(2)	If MSB of the result (1) is “1”, shift the data 1 bit to the left. And takes XOR of it and “00000111”. or If MSB of the result (1) is “0”, shift the data 1 bit to the left.
(3)	If MSB of the result (2) is “1”, shift the data 1 bit to the left. And takes XOR of it and “00000111”. or If MSB of the result (2) is “0”, shift the data 1 bit to the left.
(4)	Repeat the step (3) six times. (from (2) to (4), shift the data 1 bit to the left eight times)
(5)	It takes XOR of “the result (4)” and ”middle byte of data”.
(6)	If MSB of the result (5) is “1”, shift the data 1 bit to the left. And takes XOR of it and “00000111”. or If MSB of the result (5) is “0”, shift the data 1 bit to the left.
(7)	If MSB of the result (6) is “1”, shift the data 1 bit to the left. And takes XOR of it and “00000111”. or If MSB of the result (6) is “0”, shift the data 1 bit to the left.
(8)	Repeat the step (7) six times. (from (6) to (8), shift the data 1 bit to the left eight times)
(9)	It takes XOR of “the result (8)” and ”LSB byte of data”. (LSB: Least Significant Bit)
(10)	If MSB of the result (9) is “1”, shift the data 1 bit to the left. And takes XOR of it and “00000111”. or If MSB of the result (9) is “0”, shift the data 1 bit to the left.
(11)	If MSB of the result (10) is “1”, shift the data 1 bit to the left. And takes XOR of it and “00000111”. or If MSB of the result (10) is “0”, shift the data 1 bit to the left.
(12)	Repeat the step (11) six times. (from (9) to (11), shift the data 1 bit to the left eight times) The calculation of CRC8 is finished.

The calculation method is shown as below.
The below is considered as the calculation method when the writing data is “0x201012”.
(Register Address is set to “0x2”, and writing data is set to “0x1012” in the IEXCONF register.)

Writing data: 00100000 00010000 00010010 (0x201012)
Initial value: 11111111 (0xFF)

Step (1)

MSB of Writing data	00100000	(0x20)
Initial value	11111111	(0xFF)
XOR	11011111	

Step (2)

If MSB of result (1) is “1”, shifts it 1bit to the left	10111110	(1st time)
Polynomial	00000111	
XOR	10111001	

Step (3)

If MSB of result (2) is “1”, shifts it 1bit to the left	01110010	(2nd time)
Polynomial	00000111	
XOR	01110101	

Step (4): Repeat step (3) 6 times.

Shift 1bit to the left	11101010	(3rd time)
If MSB of the above data is “1”, shifts it 1 bit to the left	11010100	(4th time)
Polynomial	00000111	
XOR	11010011	
If MSB of the above data is “1”, shifts it 1 bit to the left	10100110	(5th time)
Polynomial	00000111	
XOR	10100001	
If MSB of the above data is “1”, shifts it 1 bit to the left	01000010	(6th time)
Polynomial	00000111	
XOR	01000101	
Shift 1bit to the left	10001010	(7th time)
If MSB of the above data is “1”, shifts it 1 bit to the left	00010100	(8th time)
Polynomial	00000111	
XOR	00010011	(0x13)

Step (5)

The result (4)	00010011	(0x13)
Middle byte of writing data	00010000	(0x10)
XOR	00000011	

Step (6)

Shift 1bit to the left	00000110	(1st time)

Step (7)

Shift 1bit to the left	00001100	(2nd time)

Step (8): Repeat step (7) 6 times.

Shift 1bit to the left	00011000	(3rd time)		
Shift 1bit to the left	00110000	(4th time)		
Shift 1bit to the left	01100000	(5th time)		
Shift 1bit to the left	11000000	(6th time)		
If MSB of the data is “1”, shifts it 1 bit to the left			10000000	(7th time)
Polynomial	00000111			
XOR	10000111			
If MSB of the data is “1”, shifts it 1 bit to the left			00001110	(8th time)
Polynomial	00000111			
XOR	00001001	(0x09)		

Step (9)

The result (8)	00001001	(0x09)
LSB byte of writing data	00010010	(0x12)
XOR	00011011	

Step (10)

Shift 1bit to the left	00110110	(1st time)

Step (11)

Shift 1bit to the left	01101100	(2nd time)

Step (12): Repeat step (11) 6 times.

Shift 1bit to the left	11011000	(3rd time)		
If MSB of the data is “1”, shifts it 1 bit to the left			10110000	(4th time)
Polynomial	00000111			
XOR	10110111			
If MSB of the data is “1”, shifts it 1 bit to the left			01101110	(5th time)
Polynomial	00000111			
XOR	01101001			
Shift 1bit to the left	11010010			(6th time)
If MSB of the data is “1”, shifts it 1 bit to the left			10100100	(7th time)
Polynomial	00000111			
XOR	10100011			
If MSB of the data is “1”, shifts it 1 bit to the left			01000110	(8th time)
Polynomial	00000111			
XOR	01000001	(0x41)		

The calculation result is “0x41”.
You need add error check byte 0x41 (01000001) with CRC8 mode, if writing data is “0x201012”.

The calculation result is changed because of initial data.
Initial data is 1 byte (8bits), so there are 256 calculation results.

In fact, CPU program calculates error check byte with CRC8.
Initial value is changed as below, error check byte changes.

- Initial value: 0x00 → error check byte: 0x6A
- Initial value: 0x80 → error check byte: 0x61

```
#include <stdio.h>
unsigned char crc8_gen( const unsigned char *buffer, size_t size){
   const unsigned char polynomial = 0x07; /* x^8 + x^2 + x + 1 */
   unsigned char crc = 0xFF; /* CRC initial value = 0xFF */
   unsigned char data;
   int bit_count;
   size_t i=0;

   for ( ; i < size; i++) {
      data = crc ^ *buffer++;
      for ( bit_count = 0; bit_count < 8; bit_count++ ){
         if ( ( data & 0x80 ) != 0 ) {
            data <<= 1;
            data ^= polynomial;
         } else {
            data <<= 1;
         }
      }
      crc =data;
   }
   return crc;
}

int main () {
   unsigned char buffer[3];
   unsigned char crc8;

  /* Example:
        Write 0x1012 to IEXCONF Register.
        Command 0x201012
  */
  buffer[0] = 0x20; /* Command Byte ( Address=2, Write) */
  buffer[1] = 0x10; /* Write Data MS Byte */
  buffer[2] = 0x12; /* Write Data LS Byte */

  crc8 =crc8_gen( buffer, 3 );
  printf( "CRC8 = 0x%02X¥n", crc8 );
  /* Result : CRC8 = 0x41 */

  return 0;
}
```

Check Sum mode

The error check byte added in Check Sum mode is calculated by the following procedure.
In case data is 3 byte, calculating as below.

Step	DESCRIPTION
(1)	Adding MSB byte, Middle byte and LSB byte of the data. Overflow is ignored. MSB: Most Significant Bit, LSB: Least Significant Bit)
(2)	The bits of result (1) inverted (1's complement) is error check byte.

The calculation method is shown as below.
The below is considered as the calculation method when the writing data is "0x201012".
(Register Address is set to "0x2", and writing data is set to "0x1012" in the IEXCONF register.)

Writing data: 00100000 00010000 00010010 (0x201012)

Step (1)

MSB byte	00100000	(0x20)
Middle byte	00010000	(0x10)
LSB byte	00010010	(0x12)
Addition result	01000010	(0x42)

Step (2)

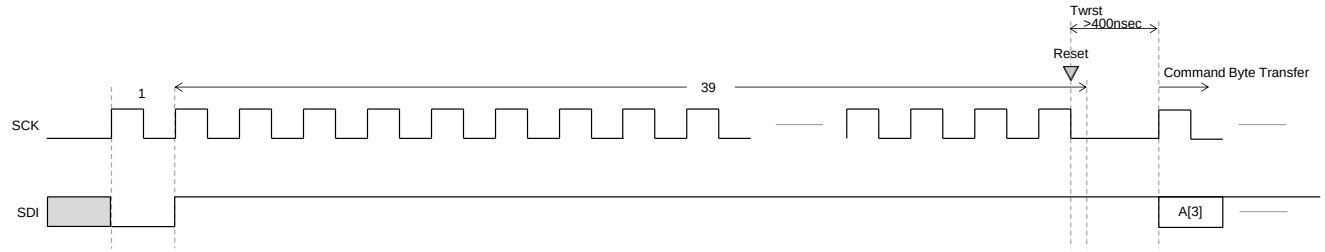
The result of step (1)	01000010	(0x42)
1' complement	10111101	(0xBD)

The calculation result is "0xBD".
You need add error check byte (0xBD) with Check Sum mode, if writing data is "0x201012".

SPI reset command

Transferring SDI=1 continuously for 39 bits after SDI=0 resets the chip.
In normal operation, since there is "0" in the ZERO [1: 0] bits of the SPI command byte, SDI=1 never becomes 39 consecutive bits.

Wait at least 400nsec after reset and transfer the command byte of operation start. 400nsec is the minimum required for internal startup time.

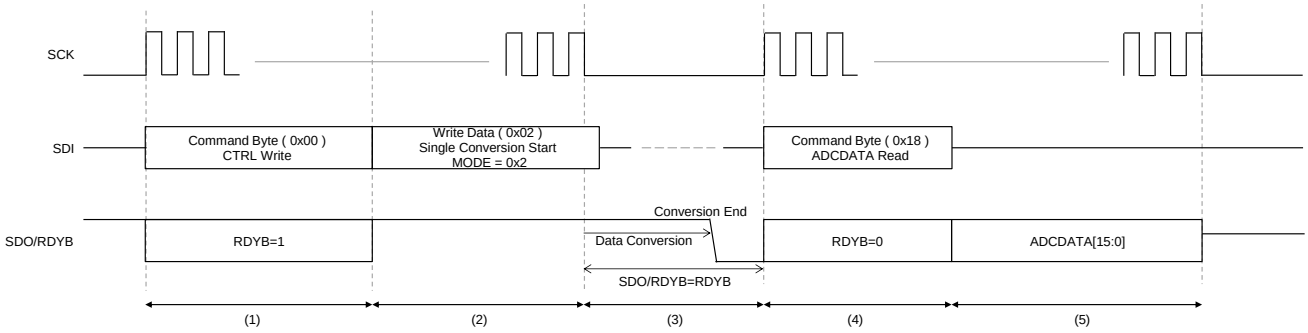


SPI reset command

SPI communication example

< Single conversion >

This is an example of communication with the PGA gain setting implemented. (Processing in the shortest time)



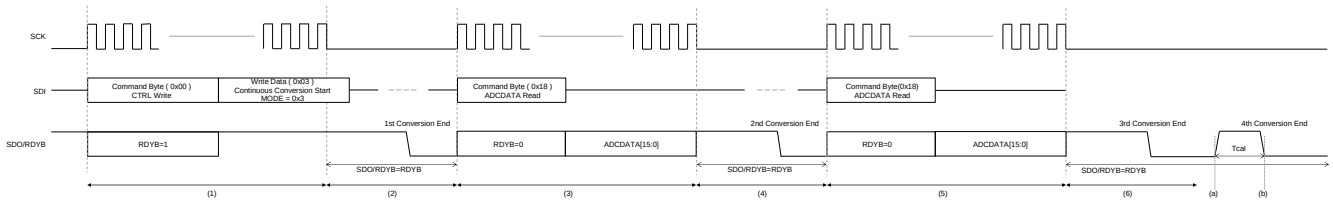
Single conversion example

STEP	DETAILS
(1)	Specify the address "0x0" of the CTRL register.
(2)	Specify single conversion "0x2" (= MODE).
(3)	Performs single conversion. (Conversion time + setup time + data correction time (= 1 / DR + T_s + T_{cal}))
(4)	Specify the ADCDATA register (0x1).
(5)	Read the conversion data (ADCDATA register).

The table below shows the time when CLKDIV = 0 and the operation clock of SPI is 5 Mbps.
It is understood that the time of SPI communication << conversion time.

OSR	Conversion time (1/DR+T_s+T_{cal}) [µsec]	SPI communication time ((1)+(2)+(4)+(5)) [µsec]
512	1255	8 (= 1/(5[Mbit/s]) x 5[byte] x 8[bit/byte])
256	640	
128	333	
64	180	

< Continuous conversion >



Continuous conversion example

STEP	DETAILS
(1)	Specify the address "0x0" of the CTRL register and specify continuous conversion "0x3" (= MODE).
(2)	Perform continuous conversion (first time). After conversion, SDO / RDYB changes from "1" to "0".
(3)	Specify the address "0x1" of the ADCDATA register. SDO / RDYB changes from "0" to "1" when conversion data (ADCDATA register) is read.
(4)	Perform continuous conversion (second time). After conversion, SDO / RDYB changes from "1" to "0".
(5)	Specify the address "0x1" of the ADCDATA register. SDO / RDYB changes from "0" to "1" when conversion data (ADCDATA register) is read.
(6)	Perform continuous conversion (third time). After conversion, SDO / RDYB changes from "1" to "0".

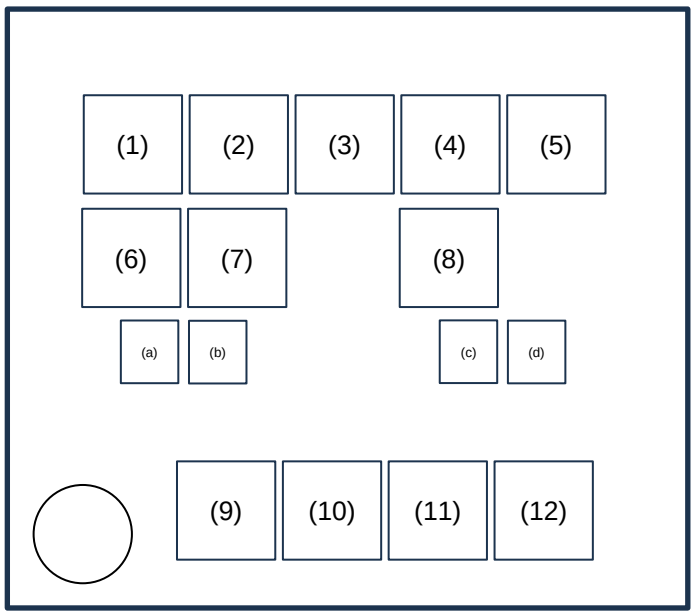
SDO / RDYB is kept "0" when reading the third conversion result is not performed.
If reading is not performed, it operates as follows.

(a) SDO / RDYB changes from "0" to "1" when the fourth AD conversion before data correction ends.
(b) After the data correction time (T_{cal}), SDO / RDYB changes from "1" to "0".

At the point (a) above, the third conversion data is discarded.
If conversion data (ADCDATA register) is not read before the next (a) comes, the fourth data is also discarded. In order to read data safely, it is necessary to read the conversion data before (a) comes.

MARKING SPECIFICATION (QFN4040-24-NB)

(1)(2)(3)(4)(5)(6)(7) Product Code Refer to *Part Marking List*
(8) to (12) , (a) to (d) Control Number



1Pin

Part Marking List（QFN4040-24-NB）

Product Name	(1)	(2)	(3)	(4)	(5)	(6)	(7)
NA2202ABAE2S	A	2	2	0	2	A	S
NA2203NBAE2S	A	2	2	0	3	A	S
NA2204NBAE2S	A	2	2	0	4	A	S

NOTICE

There can be variation in the marking when different AOI (Automated Optical Inspection) equipment is used. In the case of recognizing the marking characteristic with AOI, please contact our sales or distributor before attempting to use AOI.

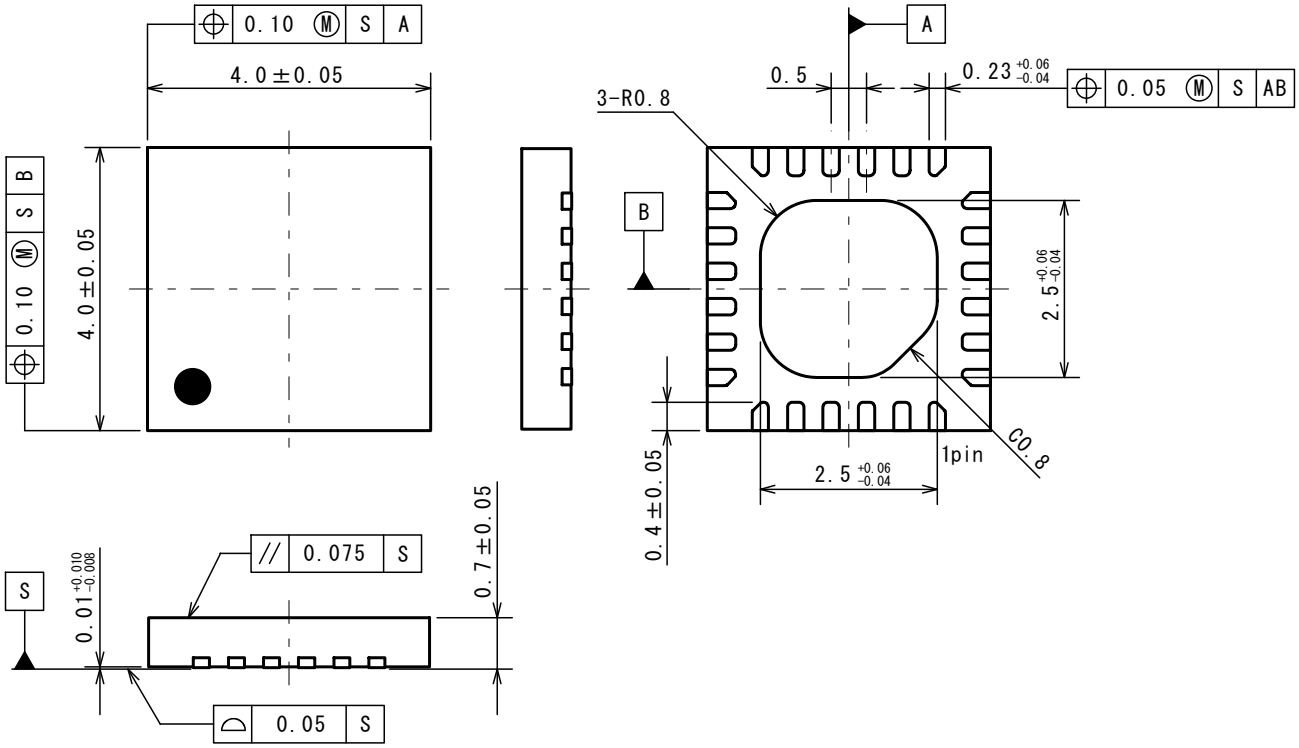
Nisshinbo Micro Devices Inc.

QFN4040-24-NB

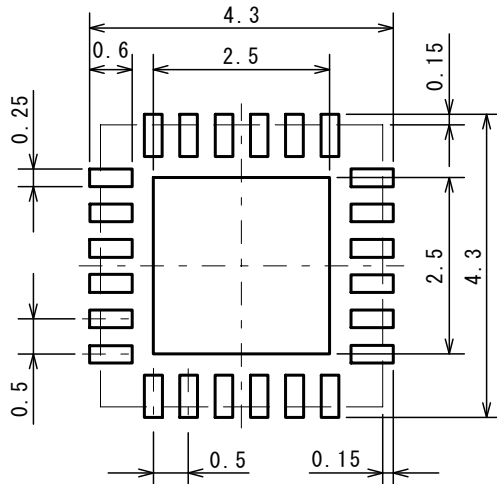
PI-QFN4040-24-NB-E-B

■ PACKAGE DIMENSIONS

UNIT: mm



■ EXAMPLE OF SOLDER PADS DIMENSIONS



Nisshinbo Micro Devices Inc.

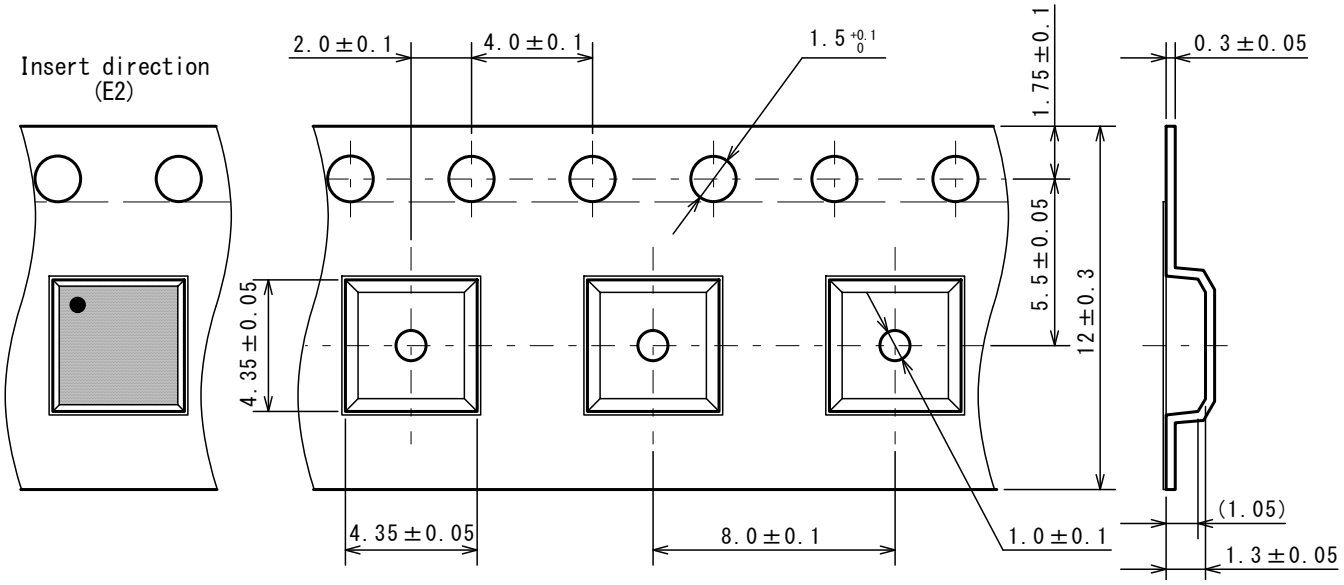
QFN4040-24-NB

PI-QFN4040-24-NB-E-B

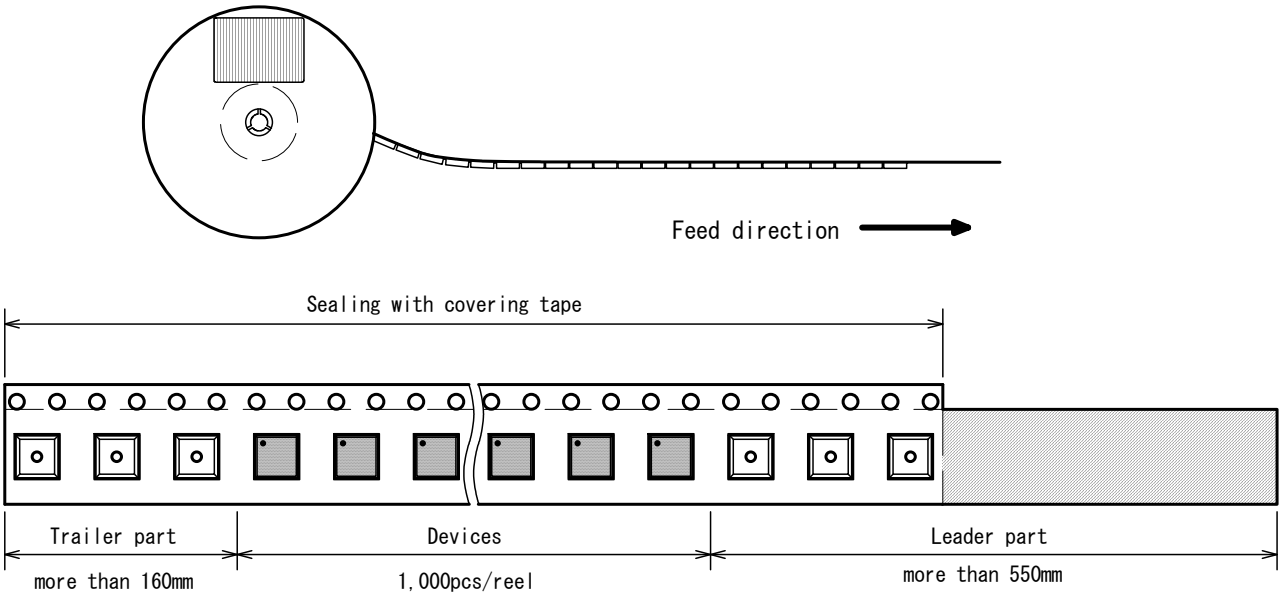
■ PACKING SPEC

UNIT: mm

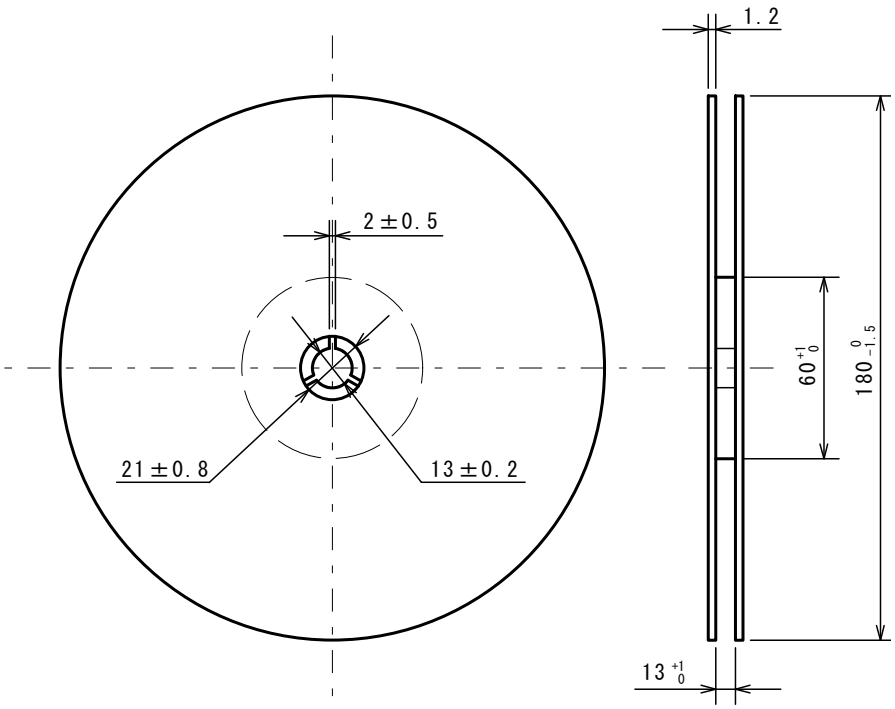
(1) Taping dimensions / Insert direction



(2) Taping state



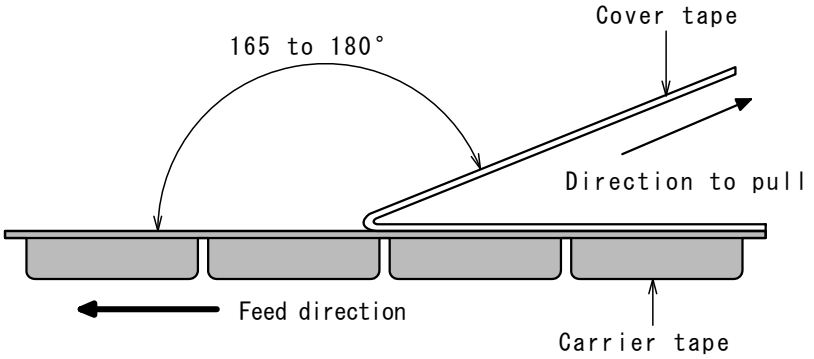
(3) Reel dimensions



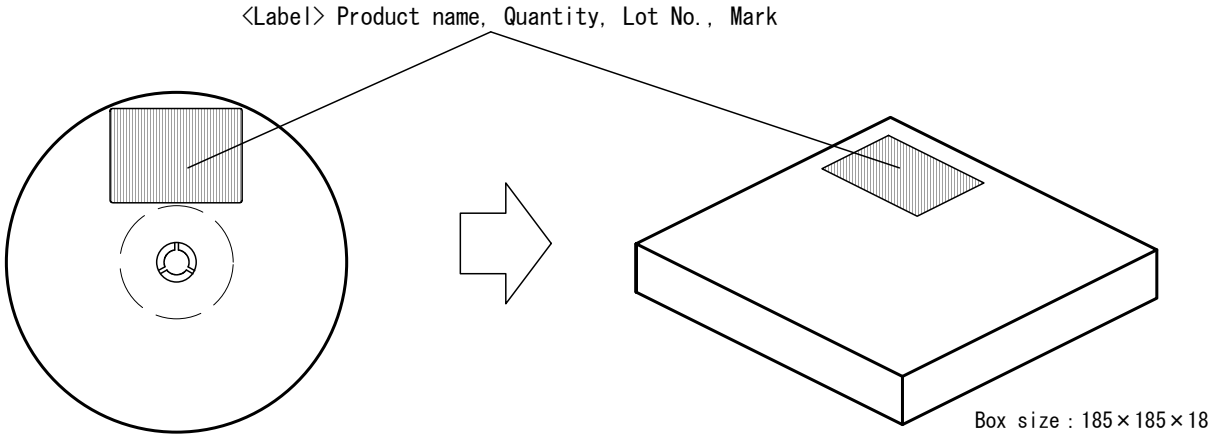
(4) Peeling strength

Peeling strength of cover tape

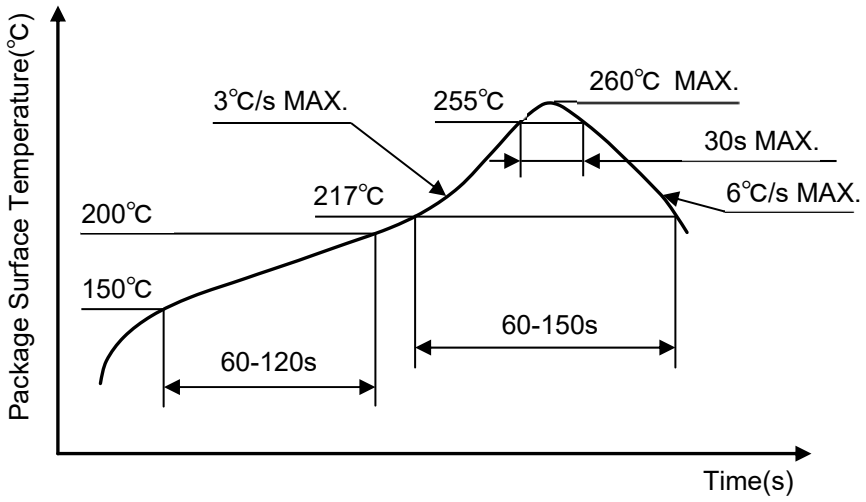
- Peeling angle 165 to 180° degrees to the taped surface.
- Peeling speed 300mm/min
- Peeling strength 0.1 to 1.3N



(5) Packing state



■ **HEAT-RESISTANCE PROFILES**



Reflow profile

■ REVISION HISTORY

Date	Revision	Changes
Jun. 6th, 2024	Ver. 1.0	Initial release Preliminary Datasheet
Aug. 30th. 2024	Ver.1.1	Replacement to Typical Application Circuit Error correction
Apr. 3rd. 2025	Ver. 1.2	Spell error correction Added block diagram

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    - Equipment Used in the Deep Sea
    - Power Generator Control Equipment (nuclear, steam, hydraulic, etc.)
    - Life Maintenance Medical Equipment
    - Fire Alarms / Intruder Detectors
    - Vehicle Control Equipment (automotive, airplane, railroad, ship, etc.)
    - Various Safety Devices
    - Traffic control system
    - Combustion equipment

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    In the case of a product purchased through an authorized distributor or directly from us, the warranty period for this product shall be one (1) year after delivery to your company. For defective products that occurred during this period, we will take the quality warranty measures described in section 8-2. However, if there is an agreement on the warranty period in the basic transaction agreement, quality assurance agreement, delivery specifications, etc., it shall be followed.
    8-2. Quality Warranty Remedies
    When it has been proved defective due to manufacturing factors as a result of defect analysis by us, we will either deliver a substitute for the defective product or refund the purchase price of the defective product.
    Note that such delivery or refund is sole and exclusive remedies to your company for the defective product.
    8-3. Remedies after Quality Warranty Period
    With respect to any defect of this product found after the quality warranty period, the defect will be analyzed by us. On the basis of the defect analysis results, the scope and amounts of damage shall be determined by mutual agreement of both parties. Then we will deal with upper limit in Section 8-2. This provision is not intended to limit any legal rights of your company.
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10. The X-ray exposure can influence functions and characteristics of the products. Confirm the product functions and characteristics in the evaluation stage.
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