Motion SPM® 5 Series

FSB50550BB

General Description

The FSB50550BB is an advanced Motion SPM 5 module providing a fully−featured, high−performance inverter output stage for AC Induction, BLDC and PMSM motors. These modules integrate optimized gate drive of the built−in MOSFETs (FRFET® technology) to minimize EMI and losses, while also providing multiple on−module protection features including under−voltage lockouts and thermal monitoring. The built−in high−speed HVIC requires only a single supply voltage and translates the incoming logic−level gate inputs to the high−voltage, high−current drive signals required to properly drive the module's internal MOSFETs. Separate open−source MOSFET terminals are available for each phase to support the widest variety of control algorithms.

Features

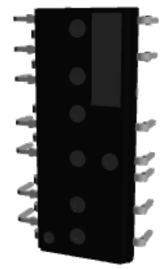
- Gate Driver Resistance R_{ON} = 4.5 kΩ, R_{OFF} = 1.2 kΩ
- Optimized for over 10 kHz Switching Frequency
- 500 V FRFET MOSFET 3−Phase Inverter with Gate Drivers and Protection
- Built−In Bootstrap Diodes Simplify PCB Layout
- Separate Open−Source Pins from Low−Side MOSFETs for Three−Phase Current−Sensing
- Active−HIGH Interface, Works with 3.3/5 V Logic, Schmitt−Trigger Input
- Optimized for Low Electromagnetic Interference
- HVIC Temperature−Sensing Built−In for Temperature Monitoring
- HVIC for Gate Driving and Under−Voltage Protection
- Isolation Rating: 1500 V_{rms}/min.
- This Device is Pb−Free and is RoHS Compliant

Applications

- 3−Phase Inverter Driver for Small Power AC Motor Drives

Related Source

- RD−FSB50450AS − Reference Design for Motion SPM 5 Series Ver.2
- AN−9082 − Motion SPM5 Series Thermal Performance by Contact Pressure



SPM5T−021/21LD
CASE MODET

MARKING DIAGRAM

FSB50550BB
ZKKXYY

FSB50550BB	= Specific Device Code
Z	= Assembly Code
KK	= Lot Run Traceability Code
XYY	= Date Code

ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

ORDERING INFORMATION

Device	Device Marking	Package	Packing Type	Quantity
FSB50550BB	FSB50550BB	SPM5T−021 (Pb−Free)	Rail	15

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Rating	Unit
INVERTER PART (Each MOSFET Unless Otherwise Specified)				
V_{DSS}	Drain−Source Voltage of Each MOSFET		500	V
*$I_{D\ 25}$	Each MOSFET Drain Current, Continuous	T_C = 25°C	3.0	A
*$I_{D\ 80}$	Each MOSFET Drain Current, Continuous	T_C = 80°C	1.9	A
*I_{DP}	Each MOSFET Drain Current, Peak	T_C = 25°C, PW < 100 μs	7.0	A
*I_{DRMS}	Each FRFET Drain Current, Rms	T_C = 80°C, F_{PWM} < 20 kHz	1.3	A_{rms}
CONTROL PART (Each HVIC Unless Otherwise Specified)				
V_{DD}	Control Supply Voltage	Applied Between V_{DD} and COM	20	V
V_{BS}	High−side Bias Voltage	Applied Between V_B and V_S	20	V
V_{IN}	Input Signal Voltage	Applied Between IN and COM	−0.3~V_{DD} + 0.3	V
BOOTSTRAP DIODE PART (Each Bootstrap Diode Unless Otherwise Specified.)				
V_{RRMB}	Maximum Repetitive Reverse Voltage		500	V
* I_{FB}	Forward Current	T_C = 25°C	0.5	A
* I_{FPB}	Forward Current (Peak)	T_C = 25°C, Under 1 ms Pulse Width	2.0	A
THERMAL RESISTANCE				
$R_{th(j-c)Q}$	Junction to Case Thermal Resistance (Note 1)	Each FET under inverter operating condition (Note 1)	8.9	°C/W
TOTAL SYSTEM				
T_J	Operating Junction Temperature		−40~150	°C
T_{STG}	Storage Temperature		−40~125	°C
V_{ISO}	Isolation Voltage	60 Hz, Sinusoidal, 1 minute, Connect Pins to Heat Sink Plate	1500	V_{rms}

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

NOTES:
1. For the measurement point of case temperature T_C, Please refer to Figure 4.
2. Marking “ * ” is calculation value or design factor.

PIN DESCRIPTIONS

Pin No.	Pin Name	Pin Description
1	COM	IC Common Supply Ground
2	$V_{B(U)}$	Bias Voltage for U−Phase High−Side MOSFET Driving
3	$V_{DD(U)}$	Bias Voltage for U−Phase IC and Low−Side MOSFET Driving
4	$IN_{(UH)}$	Signal Input for U−Phase High−Side
5	$IN_{(UL)}$	Signal Input for U−Phase Low−Side
6	N.C	No Connection
7	$V_{B(V)}$	Bias Voltage for V−Phase High Side MOSFET Driving
8	$V_{DD(V)}$	Bias Voltage for V−Phase IC and Low Side MOSFET Driving
9	$IN_{(VH)}$	Signal Input for V−Phase High−Side
10	$IN_{(VL)}$	Signal Input for V−Phase Low−Side
11	N.C	No Connection
12	$V_{B(W)}$	Bias Voltage for W−Phase High−Side MOSFET Driving
13	$V_{DD(W)}$	Bias Voltage for W−Phase IC and Low−Side MOSFET Driving
14	$IN_{(WH)}$	Signal Input for W−Phase High−Side
15	$IN_{(WL)}$	Signal Input for W−Phase Low−Side
16	V_{TS}	Output for HVIC Temperature Sensing
17	P	Positive DC−Link Input
18	U, $V_{S(U)}$	Output for U−Phase & Bias Voltage Ground for High−Side MOSFET Driving
19	N_U	Negative DC−Link Input for U−Phase
20	N_V	Negative DC−Link Input for V−Phase
21	V, $V_{S(V)}$	Output for V−Phase & Bias Voltage Ground for High−Side MOSFET Driving
22	N_W	Negative DC−Link Input for W−Phase
23	W, $V_{S(W)}$	Output for W Phase & Bias Voltage Ground for High−Side MOSFET Driving

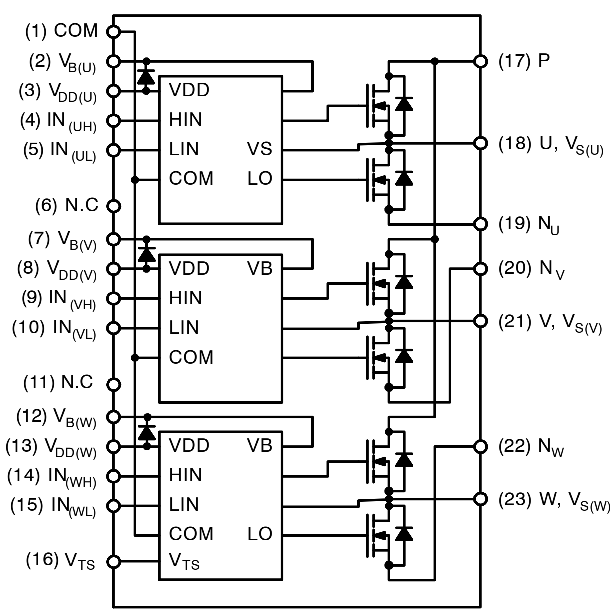


Figure 1. Pin Configuration and Internal Block Diagram (Bottom View)

NOTE:
3. Source terminal of each low−side MOSFET is not connected to supply ground or bias voltage ground inside Motion SPM 5 product. External connections should be made as indicated in Figure 3.

ELECTRICAL CHARACTERISTICS (T_J = 25°C, V_{DD} = V_{BS} = 15 V Unless Otherwise Specified.)

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
INVERTER PART (Each MOSFET Unless Otherwise Specified)							
BV_{DSS}	Drain – Source Breakdown Voltage	V_{IN} = 0 V, I_D = 1 mA (Note 4)		500	–	–	V
I_{DSS}	Zero Gate Voltage Drain Current	V_{IN} = 0 V, V_{DS} = 500 V		–	–	1	mA
$R_{DS(on)}$	Static Drain – Source Turn−On Resistance	V_{DD} = V_{BS} = 15 V, V_{IN} = 5 V, I_D = 1.2 A		–	2.3	3.0	Ω
V_{SD}	Drain – Source Diode Forward Voltage	V_{DD} = V_{BS} = 15 V, V_{IN} = 0 V, I_D = −1.2 A		–	–	1.3	V
t_{ON}	Switching Times	V_{PN} = 300 V, V_{DD} = V_{BS} = 15 V, I_D = 1.2 A V_{IN} = 0 V ↔ 5 V, Inductive Load L = 3 mH High− and Low−Side MOSFET Switching (Note 5)		460	780	1100	ns
t_{OFF}				1001	1660	2300	ns
t_{rr}				–	230	–	ns
E_{ON}				–	69	–	μJ
E_{OFF}				–	17	–	μJ
RBSOA	Reverse Bias Safe Operating Area	V_{PN} = 400 V, V_{DD} = V_{BS} = 15 V, I_D = I_{DP}, V_{DS} = BV_{DSS}, T_J = 150°C High− and Low−Side MOSFET Switching (Note 6)		Full Square			
CONTROL PART (Each HVIC Unless Otherwise Specified)							
I_{QDD}	Quiescent V_{DD} Current	V_{DD} = 15 V, V_{IN} = 0 V	Applied between V_{DD} and COM	–	–	200	μA
I_{QBS}	Quiescent V_{BS} Current	V_{BS} = 15 V, V_{IN} = 0 V	Applied between $V_{B(U)}$ – U, $V_{B(V)}$ – V, $V_{B(W)}$ – W	–	–	100	μA
I_{PDD}	Operating V_{DD} Supply Current	V_{DD} – COM	V_{DD} = 15 V, f_{PWM} = 20 kHz, duty = 50%, Applied to One PWM Signal Input for Low−Side	–	–	900	μA
I_{PBS}	Operating V_{BS} Supply Current	$V_{B(U)}$ – $V_{S(U)}$, $V_{B(V)}$ – $V_{S(V)}$, $V_{B(W)}$ – $V_{S(W)}$	V_{DD} = V_{BS} = 15 V, f_{PWM} = 20 kHz, Duty = 50%, Applied to One PWM Signal Input for High−Side	–	–	800	μA
UV_{DDD}	Low−Side Under−Voltage Protection (Figure 8)	V_{DD} Under−Voltage Protection Detection Level		7.4	8.0	9.4	V
UV_{DDR}		V_{DD} Under−Voltage Protection Reset Level		8.0	8.9	9.8	V
UV_{BSD}	High−Side Under−Voltage Protection (Figure 9)	V_{BS} Under−Voltage Protection Detection Level		7.4	8.0	9.4	V
UV_{BSR}		V_{BS} Under−Voltage Protection Reset Level		8.0	8.9	9.8	V
V_{TS}	HVIC Temperature Sensing Voltage Output	V_{DD} = 15 V, T_{HVIC} = 25°C (Note 7)		600	790	980	mV
V_{IH}	ON Threshold Voltage	Logic HIGH Level	Applied between V_{IN} and COM	–	–	2.9	V
V_{IL}	OFF Threshold Voltage	Logic LOW Level		0.8	–	–	V
R_{ON}	Gate Driver ON Output Resistance			3.6	4.5	5.4	kΩ
R_{OFF}	Gate Driver OFF Output Resistance			0.96	1.2	1.44	kΩ
BOOTSTRAP DIODE PART (Each Bootstrap Diode Unless Otherwise Specified)							
V_{FB}	Forward Voltage	I_F = 0.1 A, T_C = 25°C (Note 8)		–	2.5	–	V
t_{rrB}	Reverse Recovery Time	I_F = 0.1 A, T_C = 25°C		–	80	–	ns

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

RECOMMENDED OPERATING CONDITION

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{PN}	Supply Voltage	Applied between P and N	–	300	400	V
V_{DD}	Control Supply Voltage	Applied between V_{DD} and COM	13.5	15.0	18.5	V
V_{BS}	High−Side Bias Voltage	Applied between V_B and V_S	13.5	15.0	18.5	V
$V_{IN(ON)}$	Input ON Threshold Voltage	Applied between V_{IN} and COM	3.0	–	V_{DD}	V
$V_{IN(OFF)}$	Input OFF Threshold Voltage		0	–	0.6	V
t_{dead}	Blanking Time for Preventing Arm−Short	$V_{DD} = V_{BS}$ = 13.5~16.5 V, $T_J \leq$ 150°C	2	–	–	μs
		$V_{DD} = V_{BS}$ = 12.3~14.4 V, $T_J \leq$ 150°C	1	–	–	μs
f_{PWM}	PWM Switching Frequency	$T_J \leq$ 150°C	–	15	–	kHz

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

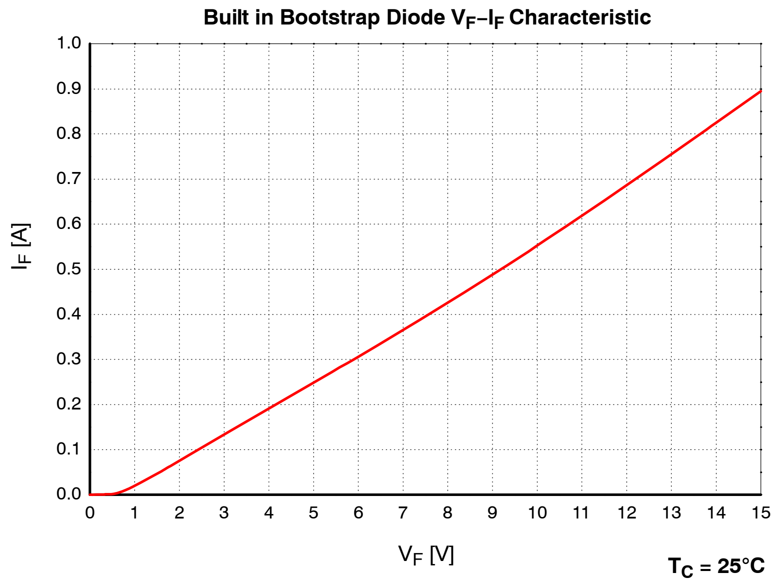
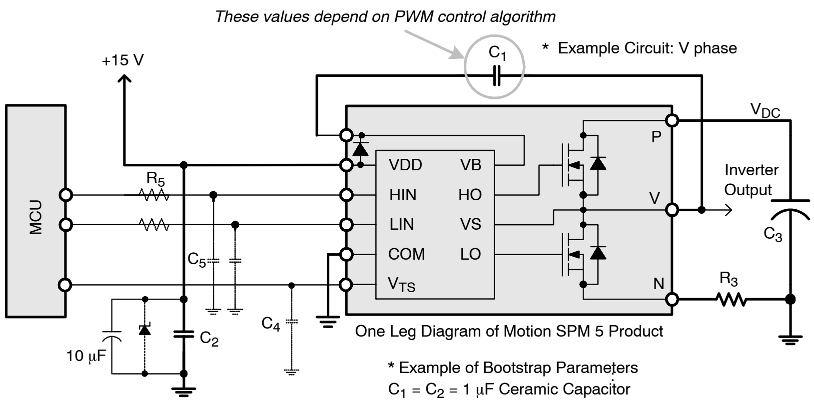


Figure 2. Built in Bootstrap Diode Characteristics (Typical)

NOTES:
4. BV_{DSS} is the absolute maximum voltage rating between drain and source terminal of each MOSFET inside Motion SPM 5 product. V_{PN} should be sufficiently less than this value considering the effect of the stray inductance so that V_{PN} should not exceed BV_{DSS} in any case.
5. t_{ON} and t_{OFF} include the propagation delay of the internal drive IC. Listed values are measured at the laboratory test condition, and they can be different according to the field applications due to the effect of different printed circuit boards and wirings. Please see Figure 6 for the switching time definition with the switching test circuit of Figure 7.
6. The peak current and voltage of each MOSFET during the switching operation should be included in the Safe Operating Area (SOA). Please see Figure 7 for the RBSOA test circuit that is same as the switching test circuit.
7. V_{ts} is only for sensing−temperature of module and cannot shutdown MOSFETs automatically.
8. Built in bootstrap diode includes around 15 Ω resistance characteristic. Please refer to Figure 2.



HIN	LIN	Output	Note
0	0	Z	Both FRFET Off
0	1	0	Low side FRFET On
1	0	V_{DC}	High side FRFET On
1	1	Forbidden	Shoot through
Open	Open	Z	Same as (0,0)

Figure 3. Recommended MCU Interface and Bootstrap Circuit with Parameters

NOTES:
9. Parameters for bootstrap circuit elements are dependent on PWM algorithm. For 15 kHz of switching frequency, typical example of parameters is shown above.
10. RC−coupling (R_5 and C_5) and C_4 at each input of Motion SPM and MCU (Indicated as Dotted Lines) may be used to prevent improper signal due to surge−noise.
11. Bold lines should be short and thick in PCB pattern to have small stray inductance of circuit, which results in the reduction of surge−voltage. Bypass capacitors such as C_1, C_2 and C_3 should have good high−frequency characteristics to absorb high−frequency ripple−current.

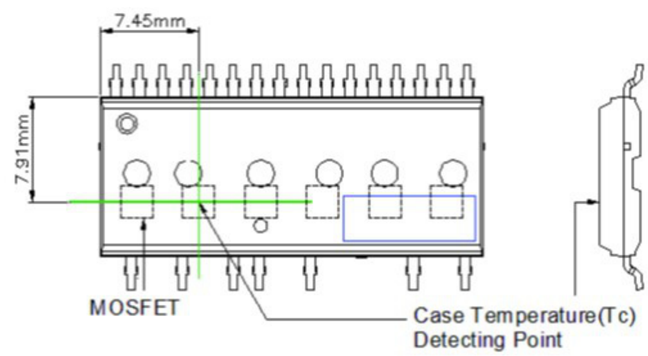


Figure 4. Case Temperature Measurement

NOTE:
12. Attach the thermocouple on top of the heat−sink of SPM 5 package (between SPM 5 package and heatsink if applied) to get the correct temperature measurement.

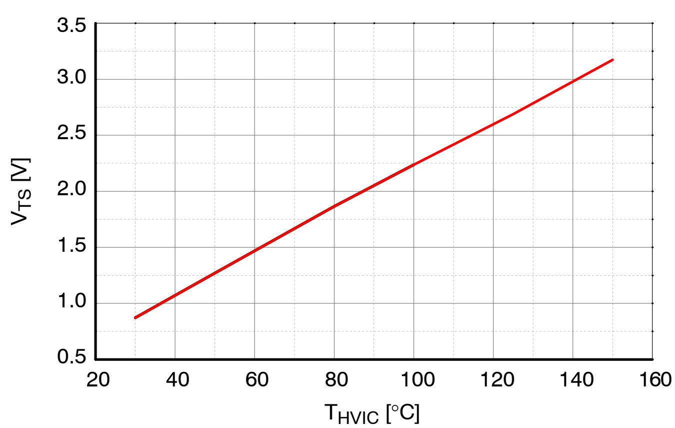


Figure 5. Temperature Profile of V_{TS} (Typical)

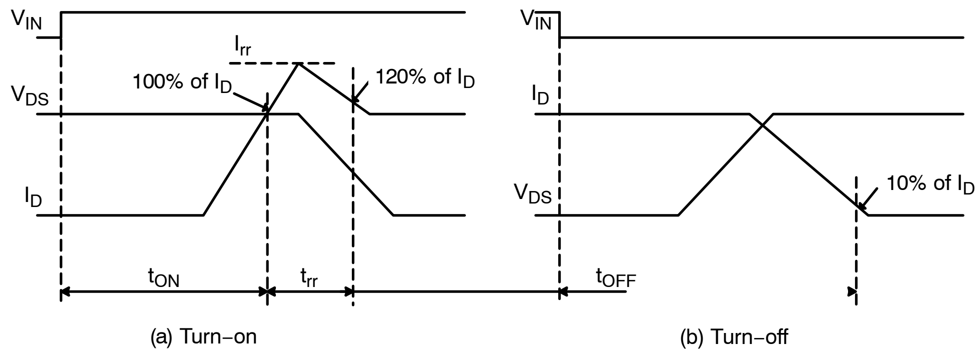


Figure 6. Switching Time Definitions

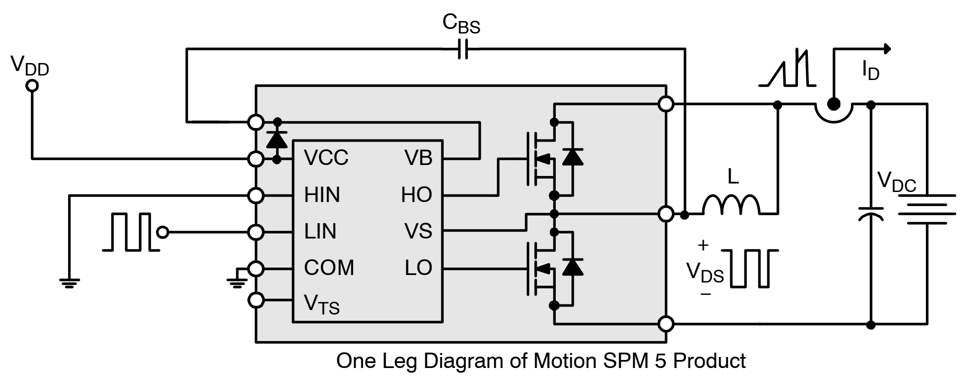


Figure 7. Switching and RBSOA (Single−Pulse) Test Circuit (Low−side)

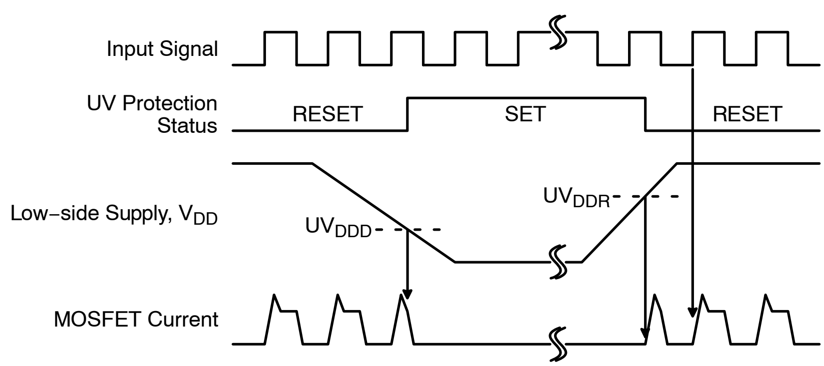


Figure 8. Under−Voltage Protection (Low−Side)

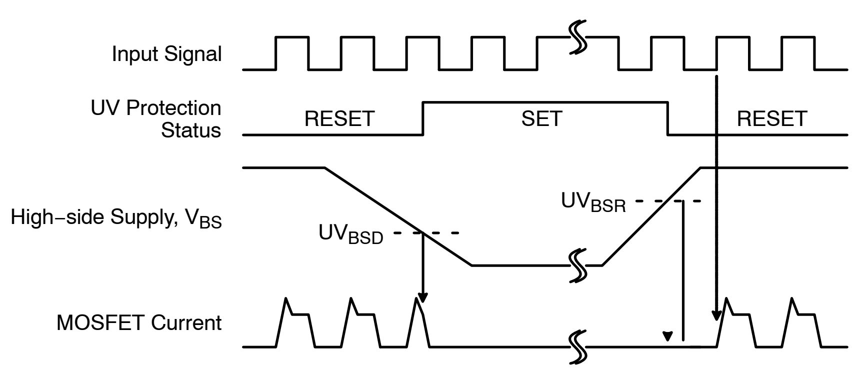


Figure 9. Under−Voltage Protection (High−Side)

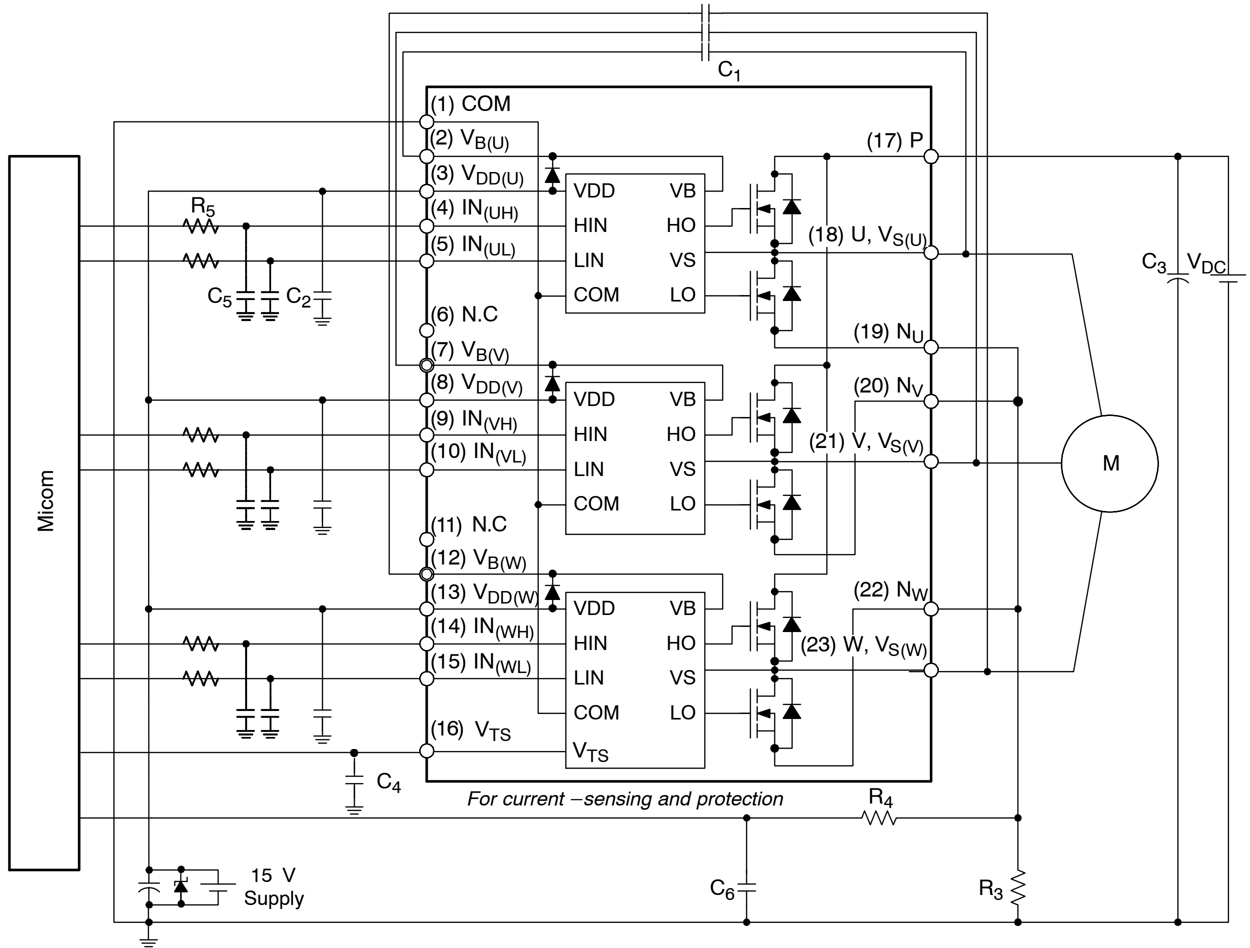


Figure 10. Example of Application Circuit

NOTES:

13. About pin position, refer to Figure 1.
14. RC−coupling (R_5 and C_5, R_4 and C_6) and C_4 at each input of Motion SPM 5 product and MCU are useful to prevent improper input signal caused by surge−noise.
15. The voltage−drop across R_3 affects the low−side switching performance and the bootstrap characteristics since it is placed between COM and the source terminal of the low−side MOSFET. For this reason, the voltage drop across R_3 should be less than 1 V in the steady−state.
16. Ground−wires and output terminals, should be thick and short in order to avoid surge−voltage and malfunction of HVIC.
17. All the filter capacitors should be connected close to Motion SPM 5 product, and they should have good characteristics for rejecting high−frequency ripple current.

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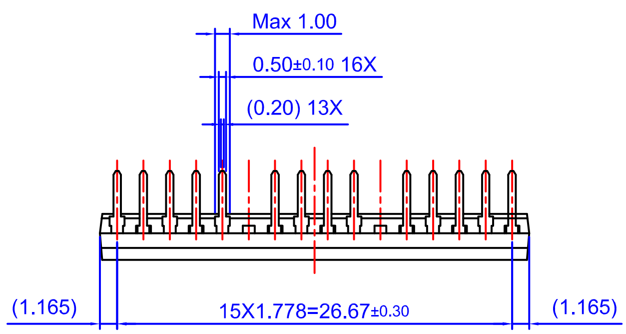

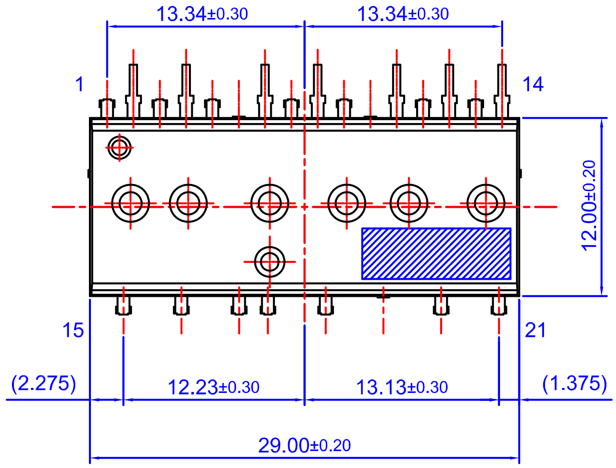

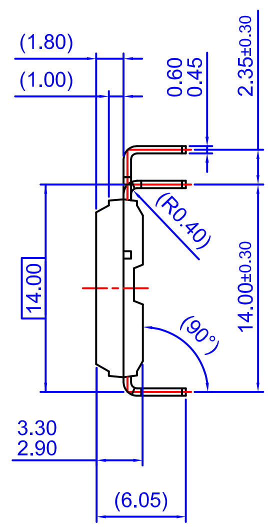

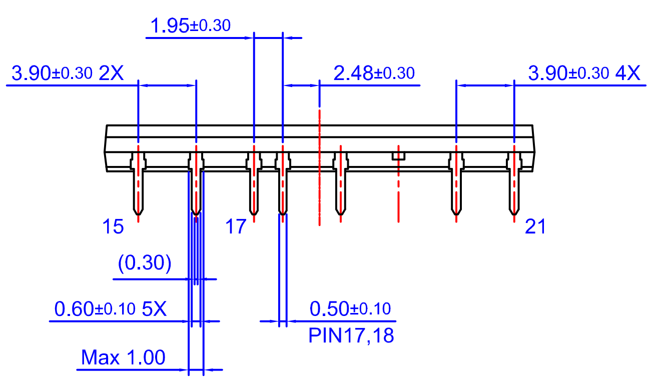

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