Evaluating the ADAQ7767-1 Flexible Resistive Input, Anti-Alias, 24-Bit, 1 MSPS, µModule DAQ Solution

FEATURES

- Fully featured evaluation board for the ADAQ7767-1
- On-board IEPE sensor interface
- On-board reference and power supply circuits
- PC software for control and data analysis of time and frequency domain
- System demonstration platform-compatible (SDP-H1, high speed controller board (EVAL-SDP-CH1Z))
- Optional PMOD connector

EVALUATION KIT CONTENTS

- EV-ADAQ7767-1FMC1Z evaluation board

EQUIPMENT NEEDED

- SDP-H1 controller board, system demonstration platform
- DC and AC signal source (Audio Precision® or similar high performance signal source)
- PC running Windows 7, Windows 8, or Windows 10 with USB 2.0 port

SOFTWARE NEEDED

- **Analysis | Control | Evaluation (ACE) Software**
- ADAQ7767-1 ACE plug-In

EVALUATION BOARD PHOTOGRAPH

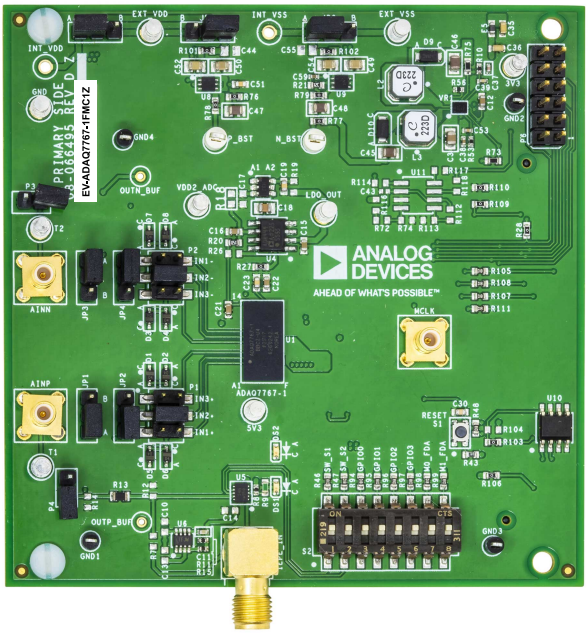


Figure 1. Evaluation Board Photograph

GENERAL DESCRIPTION

The EV-ADAQ7767-1FMC1Z evaluation kit enables simple evaluation of the ADAQ7767-1, flexible resistive input, anti-alias, 24-bit, 1 MSPS, µModule® data acquisition (DAQ) solution. The EV-ADAQ7767-1FMC1Z is used alongside a downloadable evaluation software to fully configure the features of the ADAQ7767-1 and display the conversion results in the time and frequency domains.

The EV-ADAQ7767-1FMC1Z connects to the USB port of a PC via the SDP-H1 system demonstration platform board. By default, the 3.3 V rail is supplied by the SDP-H1 and regulated by the on-board power solution to ±15 V and +5.3 V to power the ADAQ7767-1 and its support components. An integrated electronic piezoelectric (IEPE)-interface and a pair of input buffers are included to evaluate the ADAQ7767-1 across a variety of input types.

For a full description of the ADAQ7767-1, see the ADAQ7767-1 data sheet, which must be consulted in conjunction with this user guide when using the EV-ADAQ7767-1FMC1Z evaluation board. For the current schematic, layouts, and bill of materials, see the EVAL-ADAQ7767-1 product page.

TABLE OF CONTENTS

REVISION HISTORY

3/2024—Revision 0: Initial Version

QUICK START GUIDE

To begin using the EV-ADAQ7767-1FMC1Z, take the following steps:

1. Ensure the SDP-H1 controller board is disconnected from the PC, and then, install the ACE (Analysis, Control, Evaluation) software to evaluate the ADAQ7767-1. Restart the PC after the software installation is complete. For complete software installation instructions, see the Software Installation Procedures section.
2. Connect the SDP-H1 controller board to the unpowered EV-ADAQ7767-1FMC1Z evaluation board. The J4 connector of the SDP-H1 board connects to the receiving socket, P5, on the EV-ADAQ7767-1FMC1Z printed circuit board (PCB), as shown in Figure 2.
3. Ensure that the hardware links are in place according to the desired operation. For more details see Table 3.
4. Connect the 12 V DC supply to the SDP-H1 controller board and then connect the SDP-H1 to the PC using the supplied USB cable. Choose to automatically search for the drivers for the SDP-H1 if prompted by the operating system.
5. Launch the ACE (Analysis, Control, Evaluation) software from the **Analog Devices** subfolder in the **Programs** menu.
6. Double click **ADAQ7767-1 Board** to open the **ADAQ7767-1 Board View** window. The light emitting diode (LED) (DS2) then turns on to indicate that the board is powered up.
7. Double click the **ADAQ7767-1 Chip** icon in the **ADAQ7767-1 Board View** window to open the **ADAQ7767-1 Chip View** window.
8. Click **Proceed to Analysis** to show the **ADAQ7767-1 Analysis** window (see Figure 20).
9. Apply an input signal at AINP, AINN or through the optional IEPE input (IEPE_IN), then click **Run Once**.
10. To power off, first disconnect the input signal, close the software, and then, press the **Reset** button on the SDP-H1 board before disconnecting the power or USB.

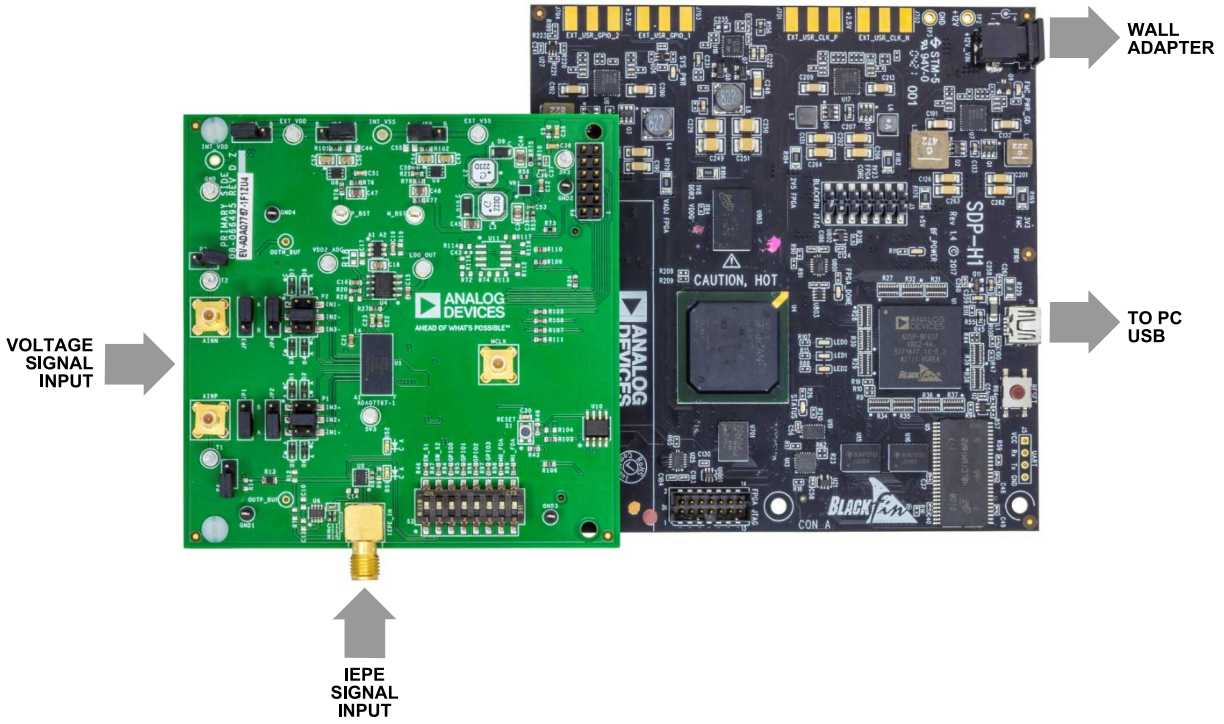


Figure 2. Evaluation Board Setup

EXAMPLE DATA CAPTURE FOR THE AC SIGNAL

To capture data for the AC signal, take the following steps:

1. Start the ACE Software software. On power-up, the ACE Software default sets the input range to **IN2**, ADC power mode to **fast**, and the filter to **wideband low ripple** with an ODR = **256 ksps**.
2. Connect the analog input signal (10.6 V_P) to AINP and AINN, and use IN2+ and IN2− as the input pins to the ADAQ7767-1 by setting the P1 and P2 jumpers (default: IN2, G = 4/11 V/V).
3. To see the result directly, click **Run Once** (which captures 8192 samples by default).
4. The sampled data is now present in the data capture tabs (**ADAQ7767-1 Board Waveform**, **ADAQ7767-1 Board Histogram**, and **ADAQ7767-1 Board FFT**). To view the results, change between each of these tabs. Note that these settings give a dynamic range of approximately 106 dB, which can be seen in the **Results** section of the **ADAQ7767-1 Board FFT** tab.

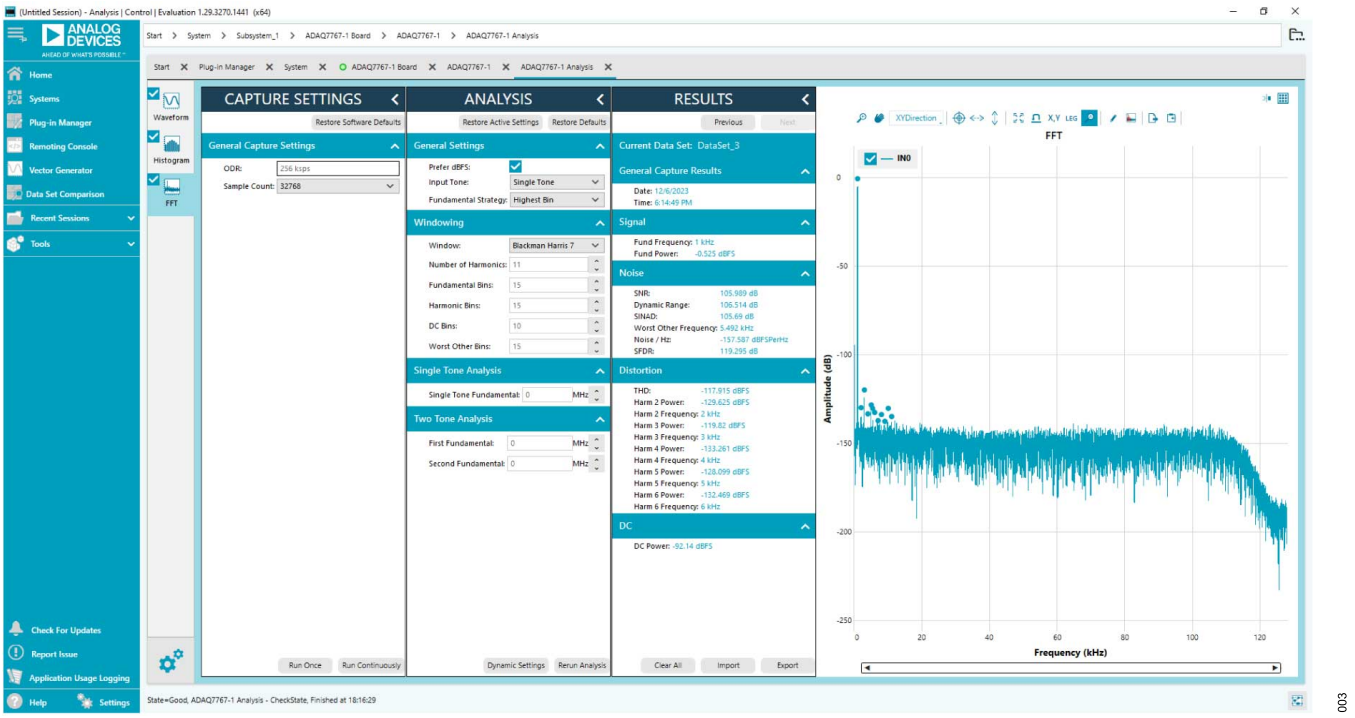


Figure 3. FFT of 10.6 V_P, a 1 kHz Fully Differential Signal Applied to IN2+ and IN2− Pins of the ADAQ7767-1

EXAMPLE DATA CAPTURE FOR THE DC SIGNAL

A sinc3 filter with ODR = 50 SPS is a sweet spot for measurement of a pure DC signal because the sinc notch appears at 50 Hz and can be used to reject the 50 Hz line frequency. Take the following steps to setup the device under test (DUT) for a 50 SPS sinc3 filter:

1. As an example for RMS noise, short the AINP and AINN connectors to GND and use IN2+ and IN2− as input pins to the ADAQ7767-1 by setting the P1 and P2 jumpers (default: IN2+ and IN2−, and G = 4/11 V/V).
2. Within the **ADAQ7767-1 Board Chip View** the **ACE Software**, click the **Filter Configuration** icon.
3. Use the drop-down menu to select **Sinc3** (programmable decimation rate) option as shown in Figure 4.
4. To configure the **Sinc3 Dec-Rate**, type **13FF** in the text box near the lower right corner as shown in Figure 5, which is also reflected in the SINC3_DEC_RATE_LSB and SINC3_DEC_RATE_MSB registers located within the memory map of the ACE software. Then, click **Apply Changes** for this to take effect.
5. Adjust the number of samples to be collected accordingly before **Run Once** is clicked. Collecting the default 8192 samples at 50 SPS takes 8192/50/60 = 2.73 minutes.
6. Set to 1024 samples, which takes approximately 20 seconds.
7. The same condition (sinc3 = 50 SPS) is used to measure the low frequency noise, as specified in the ADAQ7767-1 data sheet. In the **ADAQ7767-1 Board Histogram** tab, noise is displayed as a transition noise in LSB. To compare the referred to input (RTI), low frequency noise in µV RMS found in the ADAQ7767-1 data sheet, apply the following formula:

$$\begin{aligned} RTI\ \ Noise &= \text{Transition Noise} \times 1\ \text{LSB} \\ &= \text{Transition Noise} \times \frac{4.096}{2^{24-1} \times AFE\_GAIN} \\ &= \text{Transition Noise} \times \frac{488\ \text{nV}}{AFE\_GAIN} \end{aligned} \quad (1)$$

For example, using IN2+ and IN2− with the measured transition noise = 0.778 LSB = 1.044 µV RMS RTI.

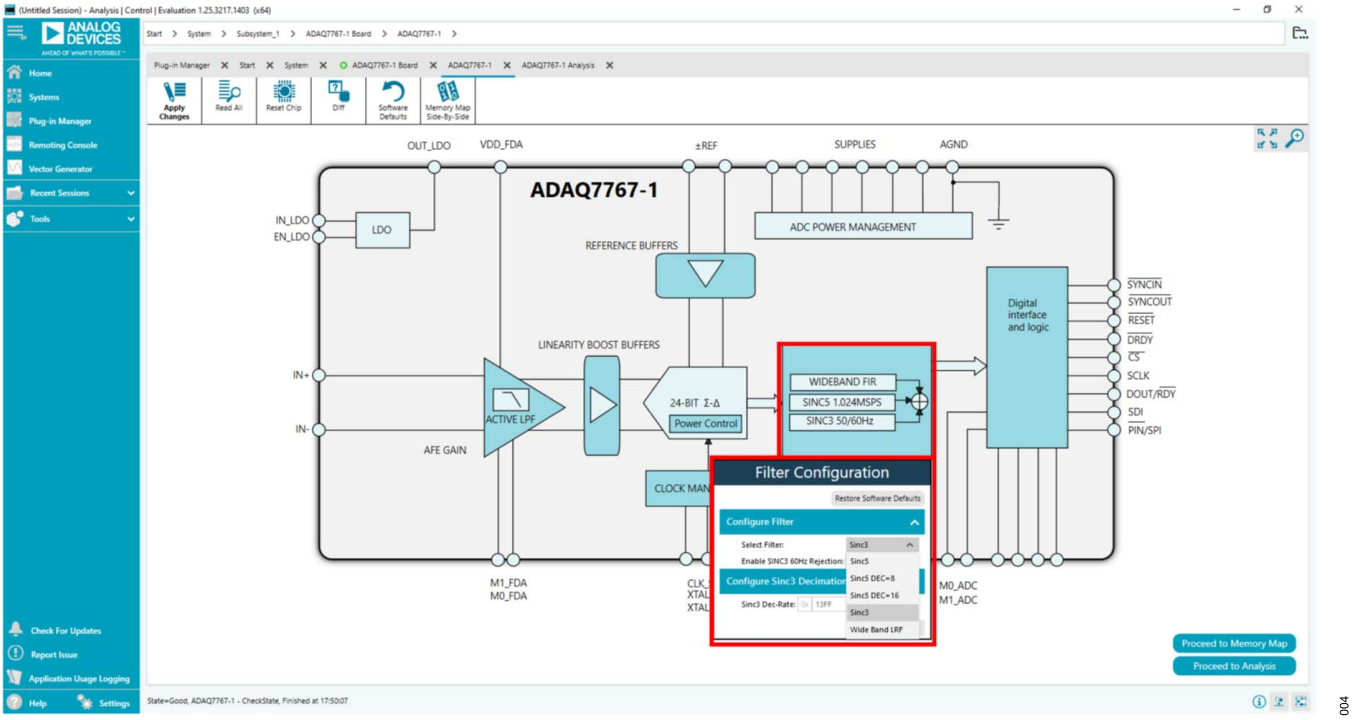
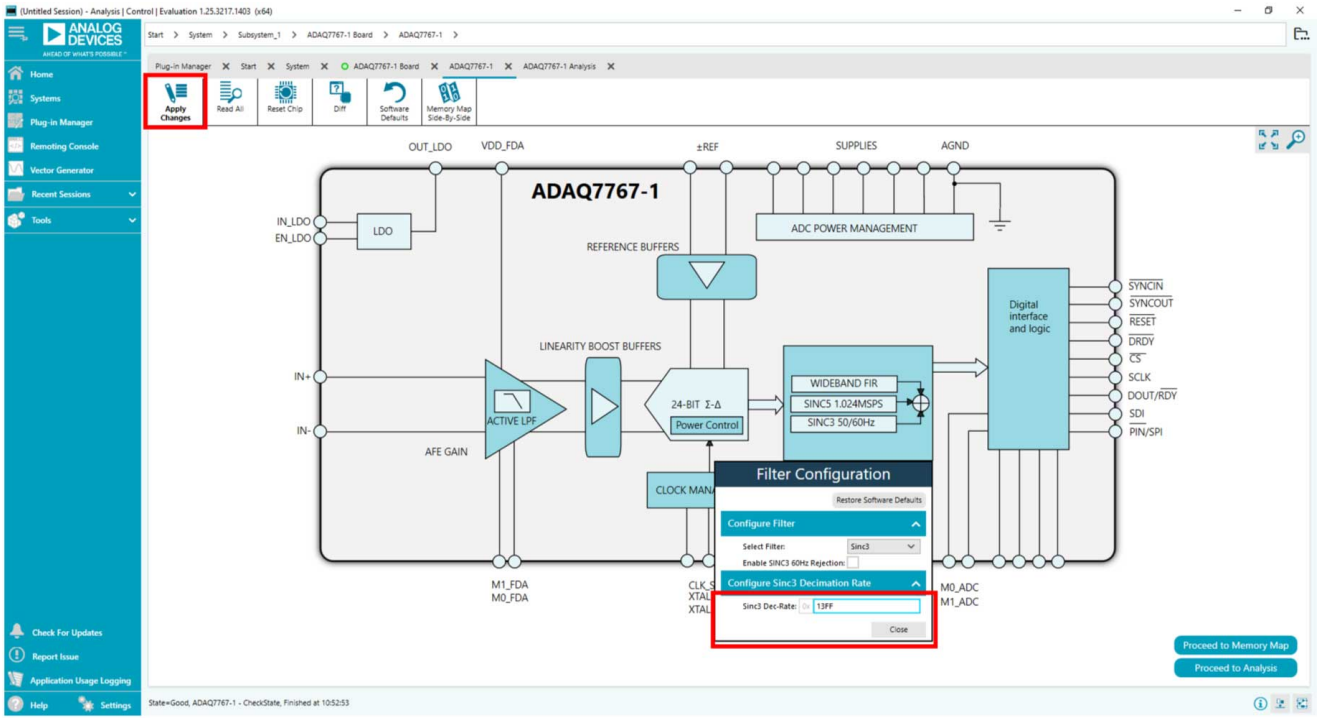


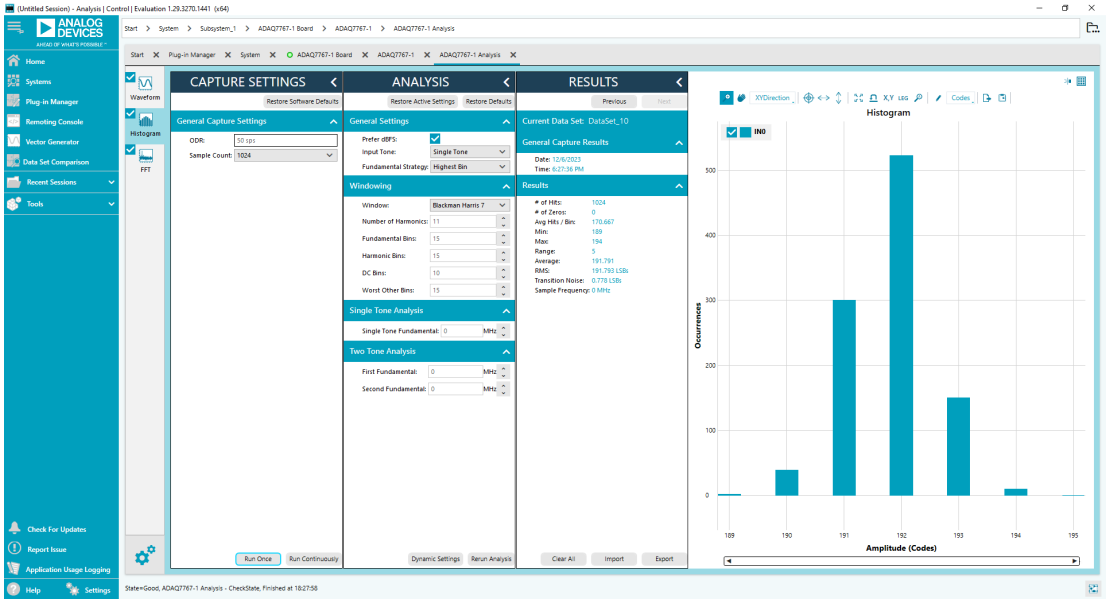
Figure 4. Set the Digital Filter Type

EXAMPLE DATA CAPTURE FOR THE DC SIGNAL



005

Figure 5. Set the Sinc3 Filter Decimation Ratio



006

Figure 6. Histogram of Output Codes with IN2+ and IN2− Shorted to GND and Sinc3 = 50 SPS

EXAMPLE DATA CAPTURE FOR THE DC SIGNAL

HOW TO CALCULATE THE SINC3_DEC_RATE VALUE

By default, the EV-ADAQ7767-1FMC1Z provides the DUT with a MCLK of approximately 16.384 MHz.

To achieve an ODR = 50 SPS using the sinc3 filter, use the following equation:

$$ODR = \frac{MCLK}{MCLK\_DIV \times DEC\_RATE} \quad (2)$$

Determine the DEC_RATE, and assume the ADAQ7767-1 is using an MCLK_DIV = 2:

$$DEC\_RATE = \frac{MCLK}{MCLK\_DIV \times ODR} = 163,840 \quad (3)$$

The SINC3_DEC_RATE_MSB and SINC3_DEC_RATE_LSB registers (Register 0x1A and Register 0x1B, respectively) increment the value in the registers by one and then multiply them by 32 to give the actual decimation rate. To set the decimation rate to 163,840, use the following equation:

$$Value = \frac{DEC\_RATE}{32} - 1 = 5119 \quad (4)$$

The values written to the sinc3 decimation registers are 5119 or 0x13FF.

Refer to the ADAQ7767-1 data sheet for more information on the DUT register configuration.

EVALUATION BOARD HARDWARE

Figure 7 shows the simplified block diagram of the EV-ADAQ7767-1FMC1Z evaluation board connected to the SDP-H1 controller board. The EV-ADAQ7767-1FMC1Z is installed with the featured ADAQ7767-1 µModule (U1) and ADR444 4.096 V reference (U4), and the on-board power solution consisting of the ADP5076 (VR1), ADP7142 (U8), ADP7182 (U9), and LTC3526LB-2 (U7). A pair of ADA4625-1 (U2 and U3) op amps can be used to buffer the inputs, while the on-board IEPE interface can be used to bias the IEPE sensor used as an input to the signal chain.

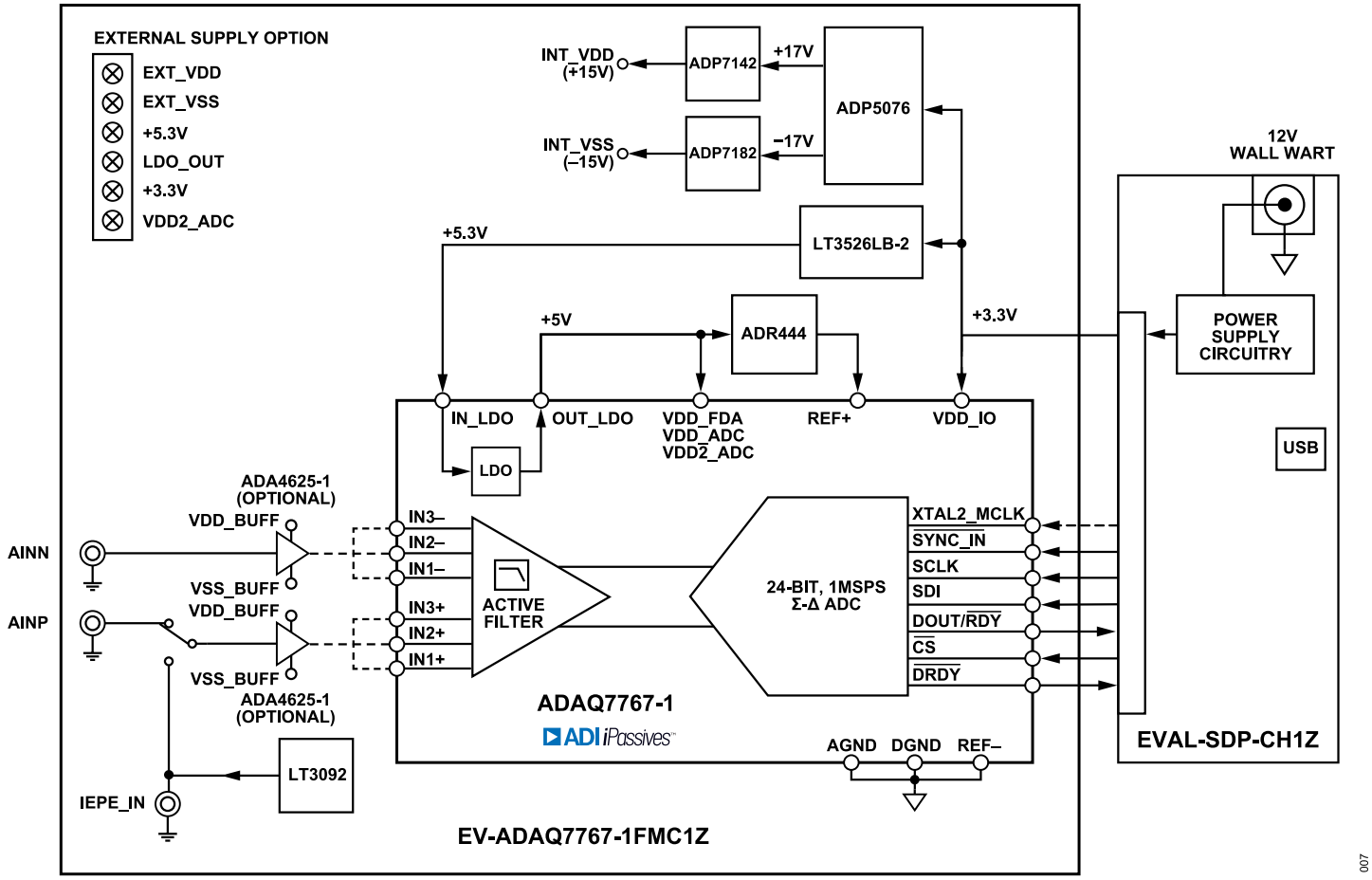


Figure 7. Simplified Evaluation Board Block Diagram

EVALUATION BOARD HARDWARE

ANALOG INPUTS

The analog inputs, AINP and AINN, are accessible either through the Subminiature Version B (SMB) connectors, or the turrets (T1 and T2). A Subminiature Version A (SMA) connector is also provided to connect to the IEPE sensor, which receives its current bias from the on-board IEPE interface.

The default settings of the EV-ADAQ7767-1FMC1Z are as follows:

- Analog inputs to ADAQ7767-1 obtained from AINP and AINN, and IEPE_IN is disconnected by P4.
- The AINP and AINN inputs are buffered by a pair of optional amplifiers, ADA4625-1 (U2 and U3).
- Using the ADR444 (U4) as a 4.096 V reference and the IN2+ and IN2− inputs of the ADAQ7767-1, the full-scale differential input range is ±11.2 V.

See Table 2 for the suggested power supply rails and Table 3 for the necessary jumper positions and link options for the different input configurations and input ranges. It is recommended to use a low distortion AC source, such as the Audio Precision APx555 series, when evaluating the dynamic performance of the ADAQ7767-1.

IEPE INTERFACE

An IEPE sensor can be used as an input to the EV-ADAQ7767-1FMC1Z through the SMA connector at IEPE_IN. The on-board IEPE interface biases the IEPE sensor, which operates by providing a 24 V rail at HV_VDD via the on-board supply or an external supply, and switches on SW_S1 and SW_S2 on the S2 mechanical switch. Inserting P4 connects the IEPE input to the ADAQ7767-1. With a dropout of 1.2 V across the current source (LT3092, U6) delivering a 4.5 mA bias to the IEPE sensor, this circuit complies to the usable excitation voltage and current bias of a typical IEPE interface (see Figure 7). For overvoltage protection from the IEPE sensor, the ADG5421F (U5) fault protection switch is placed at the IEPE input. Under normal operating conditions, the IEPE LED indicator (DS1) is on.

Most IEPE sensors have their output biased at 8 V to 14 V, with an AC swing ±5 V around the bias. The EV-ADAQ7767-1FMC1Z can be modified to allow an AC-coupled or DC-coupled IEPE input. By default, the 0 Ω resistor at R13 configures the IEPE input to be DC-coupled. The ADAQ7767-1 28 V (IN3) input is designed to allow direct DC-coupled connections to IEPE sensors. For an AC-coupled IEPE input, simply replace R13 with a ceramic capacitor, and insert a resistor at R14 to implement a high-pass filter with a cut-off frequency at the subhertz range. The AC-coupled IEPE signal swing is suitable for the 4.096 V (IN1) or the 11.2 V (IN2) input ranges of the ADAQ7767-1, depending on the AC swing of the IEPE sensor.

Table 1 summarizes the recommended jumper settings related to using an IEPE sensor input.

Table 1. Jumper Settings when Applying an IEPE Sensor Input

Function	Link	Recommended Jumper Position for IEPE Input	Comment
IEPE Input	P4	Insert jumper	Connects IEPE_IN to ADAQ7767-1.
Single-Ended Input	P3	Insert jumper	Shorts AINN to GND to allow single-ended input.
Input Buffer U2	JP1	Position A	U2 acts as a high-impedance buffer to IEPE_IN.
	JP2	Position A	
Input Buffer U3	JP3	Position B	Bypasses U3 to allow direct INx− short to GND.
	JP4	Position B	
Input Range	P1, P2	Connect Pin 1 and Pin 2 (IN3+ and IN3−)	Recommends use of IN3 (28 V) input range, which is designed for a DC-coupled IEPE sensor input.
IEPE Input Coupling	R13	0 Ω at R13	IEPE input is DC-coupled (default). Optionally, replace R13 with a capacitor to have an AC-coupled IEPE input.
IEPE Interface Supply (HV_VDD)	JP5	Position A	IEPE interface uses on-board supply INT_VDD (default). Optionally, change to Position B to use an external supply, EXT_VDD.
S2	SW_S1	High	ADG5421F Channel 1 Enable. Connects IEPE interface to IEPE_IN.
		Low	Disconnects IEPE interface from IEPE_IN.
	SW_S2	High	ADG5421F Channel 2 Enable. Connects IEPE_IN to ADAQ7767-1.
		Low	Disconnects IEPE_IN from ADAQ7767-1.

EVALUATION BOARD HARDWARE

POWER SUPPLIES

The EV-ADAQ7767-1FMC1Z obtains its power from the 3.3 V rail of the SDP-H1 by default, which is boosted and regulated to provide the supply rails required by the ADAQ7767-1, voltage reference, additional signal conditioning, and the IEPE interface.

The ADAQ7767-1 contains an internal 5 V low dropout (LDO) regulator with the purpose of simplifying the power solution and layout of the signal chain µModule. Together with this internal LDO regulator, the ADAQ7767-1 can operate with only a 5.3 V and 3.3 V rail. In the EV-ADAQ7767-1FMC1Z, the 3.3 V from the SDP-H1 directly powers the VDD_IO. This 3.3 V rail is boosted to 5.3 V by the LTC3526LB-2, which is then regulated by the internal LDO regulator to 5 V, powering VDD_FDA, VDD_ADC, VDD2_ADC, the ADR444 reference voltage, and the ADA4807-1 optional reference buffer. The 5.3 V LED (DS2) is on when a 5.3 V rail is powered by the on-board or external 5.3 V supply.

The higher voltage rails used by the input buffers and the IEPE interface, VDD/VSS_BUF and HV_VDD, are connected to the on-board rails, INT_VDD and INT_VSS, which are powered by the ADP5076 dual switching regulator, ADP7142 positive LDO regulator, and ADP7182 negative LDO regulator, as shown in Figure 8. This power tree boosts and regulates the 3.3 V to a default of +15 V and −15 V. For the larger input signal covered by the IN3 (28 V) range, the buffers and IEPE interface may require a higher voltage supply. In this case, the voltage of the rails can be increased to 28 V by moving the 0 Ω links at the feedback resistors of the ADP5076, ADP7124, and ADP7182. As an option, VDD/VSS_BUF and HV_VDD can also be connected to the external supply rails, EXT_VDD and EXT_VSS. See Table 2 for the recommended power supply rails when using the buffers and/or the IEPE interface and Table 3 for the power supply link options.

Each supply is decoupled at the point where the supply enters the EV-ADAQ7767-1FMC1Z and again at the point where the EV-ADAQ7767-1FMC1Z connects to each device. The ADAQ7767-1 has built-in, 0.1 µF supply decoupling capacitors on the VDD_FDA, VDD_ADC, VDD2_ADC, and VDD_IO supply pins.

The power solution for the EV-ADAQ7767-1FMC1Z was designed with the aid of LTpowerCAD. This tool is helpful in planning and designing power systems, with component recommendations to optimize the overall power solution.

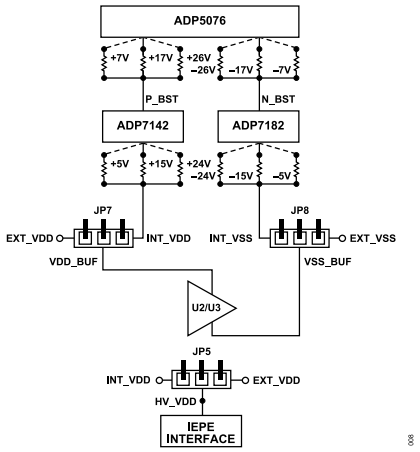


Figure 8. VDD_BUF, VSS_BUF, and HV_VDD Jumper Settings

Table 2. Recommended Power Supply Rails when Using Input Buffers and/or An IEPE Interface

Input Range (V)	ADAQ7767-1 Input Pins	IEPE Supply HV_VDD (V)	Buffer Supply VDD_BUF (V)		Comments
			Positive	Negative	
±4.096 (Voltage Input to AINP/AINN)	IN1+ and IN1−	Not applicable	P_BST = 17 VDD_BUF = INT_VDD = 15	N_BST = −17 VSS_BUF = INT_VSS = −15	By default, buffers use on-board supplies, INT_VDD and INT_VSS, set at ±15V.
±4.096 (AC-Coupled IEPE Input to IEPE_IN)	IN1+ to IEPE_IN IN1− to GND	HV_VDD = EXT_VDD = 24	P_BST = 17 VDD_BUF = INT_VDD = 15	N_BST = −17 VSS_BUF = INT_VSS = −15	If input is from an IEPE sensor applied to IEPE_IN using this input range, AC-coupled IEPE_IN to the buffer by replacing R13 with a capacitor. Connect HV_VDD to EXT_VDD and externally supply EXT_VDD with 24 V.
±11.2 (Voltage Input to AINP/AINN)	IN2+ and IN2−	Not applicable	P_BST = 17, VDD_BUF = INT_VDD = 15	N_BST = −17, VSS_BUF = INT_VSS = −15	By default, buffers use on-board supplies, INT_VDD and INT_VSS, set at ±15 V.
±11.2 (AC-Coupled IEPE Input to IEPE_IN)	IN2+ to IEPE_IN	HV_VDD = EXT_VDD = 24	P_BST = 17	N_BST = −17	If input is from an IEPE sensor applied to IEPE_IN using this input range, AC-coupled IEPE_IN to the buffer by replacing R13 with a capacitor. Connect HV_VDD to EXT_VDD and

EVALUATION BOARD HARDWARE

Table 2. Recommended Power Supply Rails when Using Input Buffers and/or An IEPE Interface (Continued)

Input Range (V)	ADAQ7767-1 Input Pins	IEPE Supply HV_VDD (V)	Buffer Supply VDD_BUF (V)		Comments
			Positive	Negative	
	IN2− to GND		VDD_BUF = INT_VDD = 15	VSS_BUF = INT_VSS = −15	externally supply EXT_VDD with 24 V.
2.5 to 21.5 Unipolar Single-Ended (Either DC-Coupled IEPE Input to IEPE_IN or Voltage Input to AINP/AINN)	IN3+ = Input	P_BST = 26	P_BST = 26	N_BST = −7	This input range is designed for DC-coupled IEPE inputs. Change supply rails to suit input range. Caution: ensure that VDD_BUF – VSS_BUF does not exceed the ADA4625-1 operating voltage of 36 V.
	IN3− to GND	HV_VDD = INT_VDD = 24	VDD_BUF = INT_VDD = 24	VSS_BUF = INT_VSS = −5	
−2.5 to −21.5, Unipolar Single-Ended (Voltage Input to AINP/AINN)	IN3+ = Input	Not applicable	P_BST = 7	N_BST = −26	Change supply rails to suit input range. Caution: ensure that VDD_BUF – VSS_BUF does not exceed the ADA4625-1 operating voltage of 36 V.
	IN3− to GND		VDD_BUF = INT_VDD = 5	VSS_BUF = INT_VSS = −24	
−2.5 to −21.5 Unipolar Single-Ended (IEPE)	Not applicable	Not applicable	Not applicable	Not applicable	Range not available for on-board IEPE interface, IEPE_IN.

EVALUATION BOARD HARDWARE

HARDWARE LINK OPTIONS

Multiple link options must be set correctly for the appropriate operating setup before applying the power and signal to the EV-ADAQ7767-1FMC1Z. Table 3 shows the default link positions for the EV-ADAQ7767-1FMC1Z.

Table 3. Default Links and Link Options

Function	Link	Default Position	Comment
Input Buffer U2	JP1	Position A	AINP is buffered by default. Optionally, bypass the buffer by changing JP1 and JP2 to Position B.
	JP2	Position A	
Input Buffer U3	JP3	Position A	AINN is buffered by default. Optionally, bypass the buffer by changing JP3 and JP4 to Position B.
	JP4	Position A	
Input Range	P1/P2	Connect Pin 3 and Pin 4 (IN2+ and IN2−)	The IN2 input range is selected by default. Optionally, connect Pin 5 and Pin 6 (IN1+ and IN1−) for both P1 and P2 to use IN1, and connect Pin 1 and Pin 2 (IN3+ and IN3−) for both P1 and P2 to use IN3.
Single-Ended Input	P3	No connect	AINN is floating by default. Optionally, for a single-ended input, insert a jumper at P3 to short AINN to GND. In addition, bypass Buffer U3 by changing JP3 and JP4 to Position B.
IEPE Input	P4	No connect	The analog inputs to the ADAQ7767-1 are obtained from AINP and AINN by default. Optionally, insert jumpers at P3 and P4 and mechanically switch on SW_S1 and SW_S2 from S2 to use the IEPE sensor as an input. In addition, bypass Buffer U3 by changing JP3 and JP4 to Position B.
IEPE Interface Supply (HV_VDD)	JP5	Position A	The IEPE interface uses an on-board supply, INT_VDD. Optionally, change to Position B to use the external supply, EXT_VDD.
Buffer Supply (VDD_BUF)	JP7	Position A	Buffers use the on-board supply, INT_VDD, by default. Optionally, change to Position B to use the external supply, EXT_VDD.
Buffer Supply (VSS_BUF)	JP8	Position A	Buffers use the on-board supply, INT_VSS, by default. Optionally, change to Position B to use the external supply, EXT_VSS.
S2	SW_S1	Low	ADG5421F Channel 1 Enable. Disconnects the IEPE interface from IEPE_IN.
		High	Connects the IEPE interface to IEPE_IN
	SW_S2	Low	ADG5421F Channel 2 Enable. Disconnects IEPE_IN from the ADAQ7767-1.
		High	Connects IEPE_IN to the ADAQ7767-1. To use the IEPE sensor as input, insert jumpers at P3 and P4 and switch on SW_S1 and SW_S2. In addition, bypass Buffer U3 by changing JP2 and JP4 to Position B.
	GPIO0, GPIO1, GPIO2, GPIO3	All low, disconnected	Reserved. Do not use.
	M0_FDA, M1_FDA	All low, disconnected	Reserved. Do not use.
IEPE Input Coupling	R13	0 Ω at R13	The IEPE input is DC-coupled by default. Optionally, replace R13 with a capacitor to have an AC-coupled IEPE input.
3.3 V Supply	R106	0 Ω at R106	The 3.3V supply is from the EVAL-SDP-CH1Z by default. Optionally, remove R106 and connect the external supply to the 3V3 turret.
5.3 V Supply	R57	0 Ω at R57	The IN_LDO pin of the ADAQ7767-1 uses the on-board 5.3 V supply. LED DS1 is on. Optionally, remove R57 and connect the external supply to the 5V3 turret.

EVALUATION BOARD HARDWARE

Table 3. Default Links and Link Options (Continued)

Function	Link	Default Position	Comment
VDD2_ADC Supply	R16	0 Ω at R16	The VDD2_ADC pin of the ADAQ7767-1 uses the internal LDO regulator by default. Optionally, remove R16 and connect the external supply to the VDD2_ADC turret.
ADP5076 VR1 Positive Output Voltage (P_BST)	R67	0 Ω at R67	P_BST is set at 17 V by default. Optionally, move 0 Ω to R68 to set P_BST = 26 V. In addition, set the ADP7142 output voltage, INT_VDD, to 24 V by moving the 0 Ω from R91 to R92. Also, optionally move 0 Ω to R69 to set P_BST = 7 V. In addition, set the ADP7142 output voltage, INT_VDD, to 5 V by moving the 0 Ω from R91 to R100.
	R68	R68 not placed	
	R69	R69 not placed	
ADP5076 VR1 Negative Output Voltage (N_BST)	R61	0 Ω at R61	N_BST is set at −17 V by default. Optionally, move 0 Ω to R66 to set N_BST = −26 V. In addition, set the ADP7182 output voltage, INT_VSS, to −24 V by moving 0 Ω from R80 to R82. Also, optionally, move 0 Ω to R71 to set N_BST = −7 V. In addition, set the ADP7182 output voltage, INT_VSS, to −5 V by moving 0 Ω from R80 to R85.
	R66	R66 not placed	
	R71	R71 not placed	
ADP7142 Output Voltage (INT_VDD)	R91	0 Ω at R91	INT_VDD at 15 V by default. Optionally, move 0 Ω to R92 to set INT_VDD = 24 V. In addition, set the ADP5076 positive output voltage, P_BST, to 26 V by moving 0 Ω from R67 to R68.Also, optionally move 0 Ω to R100 to set INT_VDD = 5 V. In addition, set the ADP5076 positive output voltage, P_BST, to 7 V by moving 0 Ω from R67 to R69.
	R92	R92 not placed	
	R100	R100 not placed	
ADP7182 Output Voltage (INT_VSS)	R80	0 Ω at R80	INT_VSS is at −15 V by default. Optionally, move 0 Ω to R82 to set INT_VSS = −24 V. In addition, set the ADP5076 negative output voltage, N_BST, to −26 V by moving 0 Ω from R61 to R66. Also, optionally, move 0 Ω to R85 to set INT_VSS = −5 V. In addition, set the ADP5076 negative output voltage, N_BST, to −7 V by moving 0 Ω from R61 to R71.
	R82	R82 not placed	
	R85	R85 not placed	
Reference Buffer A2	R20	11 Ω at R20	Reference Buffer A2 is bypassed; the ADR444 (voltage reference) output directly connects to the ADAQ7767-1 by default. Optionally, remove 11 Ω at R20 and insert 0 Ω at R19, R26, and R18 to use the reference buffer.
	R19	R19 not placed	
	R26	R26 not placed	
	R18	R18 not placed	

EVALUATION BOARD HARDWARE

ON-BOARD CONNECTORS

Table 4 provides information about the external on-board connectors on the EV-ADAQ7767-1FMC1Z.

Table 4. On-Board Connectors

Connector	Function
AINP/AINN	SMB analog inputs for AC signals
T1/T2	Turrets for DC analog inputs
IEPE_IN	SMA for the IEPE sensor input
MCLK	SMB for the external MCLK
P5	FMC connects all digital signals to the SDP-H1 controller board
P6	PMOD connector allows the user to interface with the board
LDO_OUT	Turret to connect to the external voltage reference input and voltage reference buffer supply
3V3	Turret to connect to the external 3.3 V supply
5V3	Turret to connect to the external 5.3 V supply
VDD2_ADC	Turret to connect to the external VDD2_ADC supply
EXT_VDD	Turret to connect to the external positive supply for the buffers and/or the IEPE interface
EXT_VSS	Turret to connect to the external negative supply for the buffers

EVALUATION BOARD SOFTWARE

SOFTWARE INSTALLATION PROCEDURES

Before using the EV-ADAQ7767-1FMC1Z, download and install the **Analysis | Control | Evaluation (ACE) Software**. In addition, download the ADAQ7767-1 ACE plug-in from the **ACE Evaluation Board Plug-ins** section of the **ACE Software** page or from the EV-ADAQ7767-1FMC1Z product page.

The **ACE Software** is a desktop software application that allows the evaluation and control of multiple evaluation systems across the Analog Devices, Inc., product portfolio. The installation process consists of the ACE Software and SDP-H1 driver installations.

Warning

To ensure that the evaluation system is correctly recognized when it is connected to the PC, install the ACE Software and the SDP-H1 driver before connecting the EV-ADAQ7767-1FMC1Z and the SDP-H1 controller board to the USB port of the PC.

Installing the ACE Software

To install the ACE software, take the following steps:

1. Download the ACE software to a Windows®-based PC.
2. Double-click the **ACEInstall.exe** file to begin the installation. By default, the software is saved at **C:\Program Files (x86)\Analog Devices\ACE**.
3. A dialog box appears seeking permission to allow the program to make changes to the PC. Click **Yes** to begin the installation process.
4. Click **Next >** to continue the installation, as shown in Figure 9.

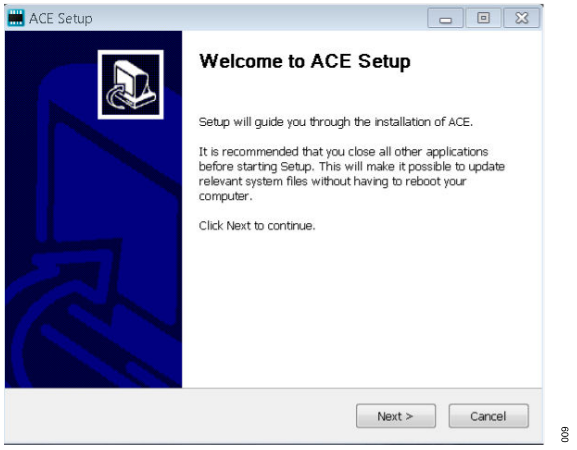


Figure 9. Evaluation Software Install Confirmation

5. Read the software license agreement and click **I Agree** (see Figure 10).

Figure 10. License Agreement

6. Choose an installation location and click **Next** (see Figure 11).

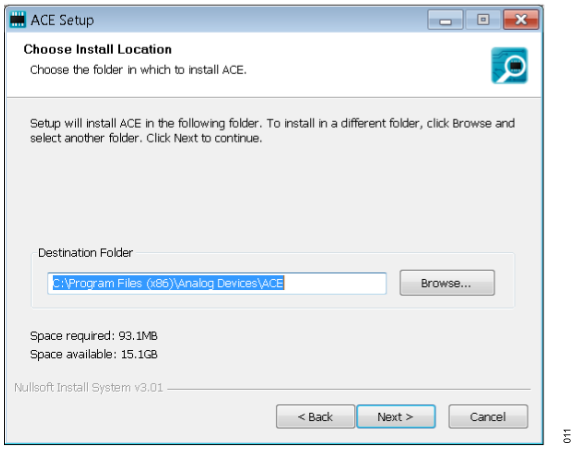


Figure 11. Choose Install Location

7. Select the **Pre-Requisites** checkbox to include the installation of the SDP-H1 driver. Click **Install** (see Figure 12).

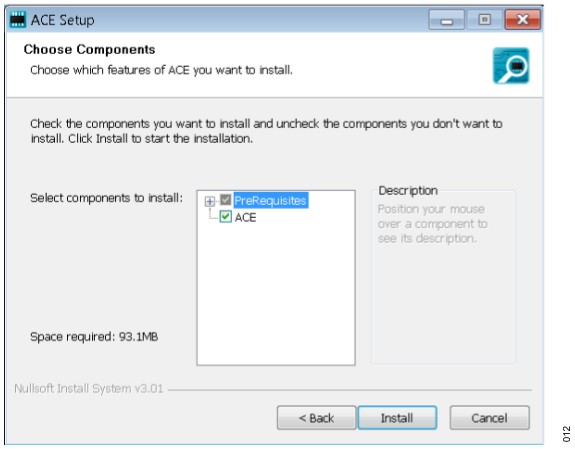


Figure 12. Choose Components

8. The **Windows Security** screen appears. Click **Install** (see Figure 13). The installation is in progress. No action is required (see Figure 14).

EVALUATION BOARD SOFTWARE

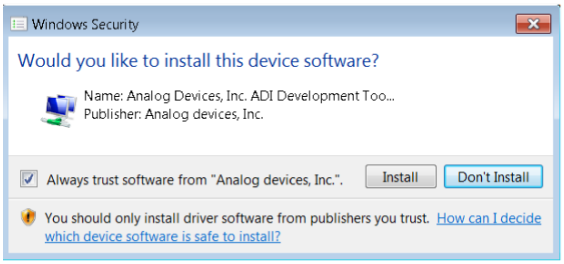


Figure 13. Windows Security Window

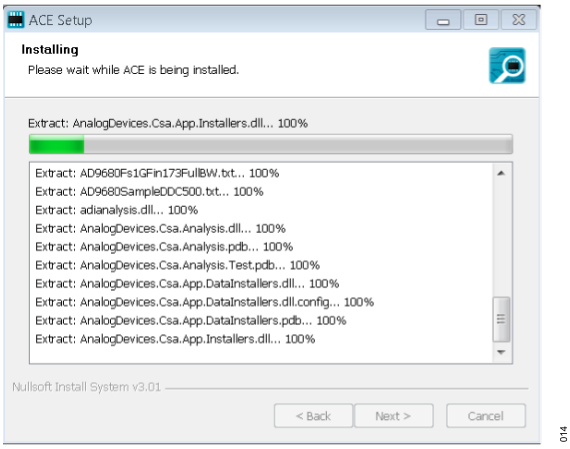


Figure 14. Installation in Progress

9. The installation is complete (see Figure 15). Click **Next >** and then **Finish** to complete.

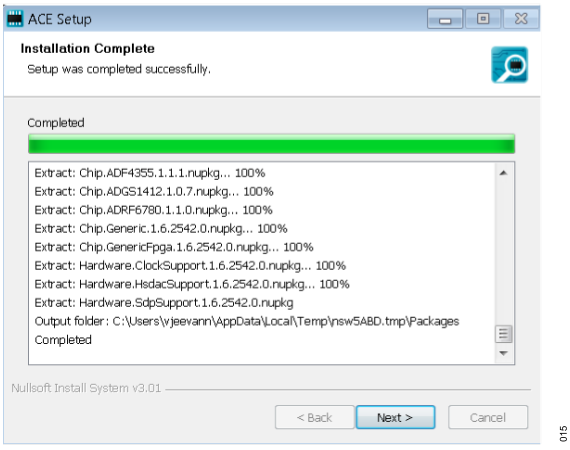


Figure 15. Installation Complete

EVALUATION BOARD SETUP PROCEDURES

The EV-ADAQ7767-1FMC1Z connects to the SDP-H1. The SDP-H1 is the communication link between the PC and the EV-ADAQ7767-1FMC1Z. Figure 2 shows a diagram of the connections between the EV-ADAQ7767-1FMC1Z and the SDP-H1.

CONNECTING THE EV-ADAQ7767-1FMC1Z AND THE SDP-H1 TO A PC

After installing the **ACE Software**, take the following steps to set up the EV-ADAQ7767-1FMC1Z and SDP-H1:

1. Ensure that all configuration links are in the appropriate positions, as detailed in Table 3.
2. Connect the EV-ADAQ7767-1FMC1Z securely to the 160-way connector on the SDP-H1. The EV-ADAQ7767-1FMC1Z does not require an external power supply adapter.
3. Connect the SDP-H1 to the PC via the USB cable included in the SDP-H1 kit.

After completing the steps in the Evaluation Board Software section and the Evaluation Board Hardware section, set up the system for data capture as follows:

1. Run the **Found New Hardware Wizard** after the SDP-H1 system demonstration platform controller board is plugged into the computer. If using Windows XP, you may need to search for the SDP-H1 drivers. Automatically search for the drivers for the SDP-H1 controller board if prompted by the operating system.
2. Check that the EV-ADAQ7767-1FMC1Z is connecting to the computer correctly using the **Device Manager** of the PC. Access the **Device Manager** as follows:
   a. Right click **My Computer** for Windows 7 or **This PC** for Windows 8 and Windows 10 and then click **Manage**.
   b. A dialog box appears asking for permission to allow the program to make changes to the computer. Click **Yes**.
   c. The **Computer Management** window appears. Click **Device Manager** from the list of **System Tools** (see Figure 16).
      1. If the SDP-H1 controller board appears under **ADI Development Tools**, the driver software is installed, and the EV-ADAQ7767-1FMC1Z is connecting to the PC correctly.

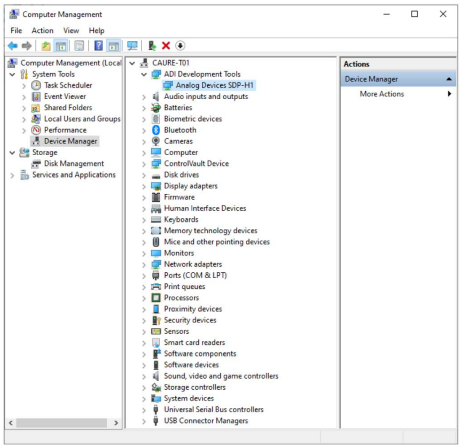


Figure 16. Checking That the Evaluation Board Is Connected to the PC Correctly

EVALUATION BOARD SOFTWARE

LAUNCHING THE SOFTWARE

When the EV-ADAQ7767-1FMC1Z and SDP-H1 boards are properly connected to the PC, launch the **ACE Software**. To launch the **ACE Software**, take the following steps:

1. From the **Start** menu, select **All Programs** > **Analog Devices > ACE > ACE.exe** to open the main software screen (see Figure 17).
2. The **ADAQ7767-1 Board** icon appears in the **Attached Hardware** section.
3. If the EV-ADAQ7767-1FMC1Z is not connected to the USB port via the SDP-H1 controller board when the software is launched, the **ADAQ7767-1 Board** icon does not appear in the **Attached Hardware** section. Connect the EV-ADAQ7767-1FMC1Z and SDP-H1 board to the USB port of the PC and wait a few seconds, then continue following these instructions.
4. Double-click the **ADAQ7767-1 Board** icon to open the **ADAQ7767-1 Board View** (see Figure 18).
5. Double click the **ADAQ7767-1 Board Chip** icon to open the **ADAQ7767-1 Board Chip View** (see Figure 19).
6. Click **Software Defaults** and then click **Apply Changes**.
7. Click **Proceed to Analysis** to open the **ADAQ7767-1 Board Analysis** window shown in Figure 20.

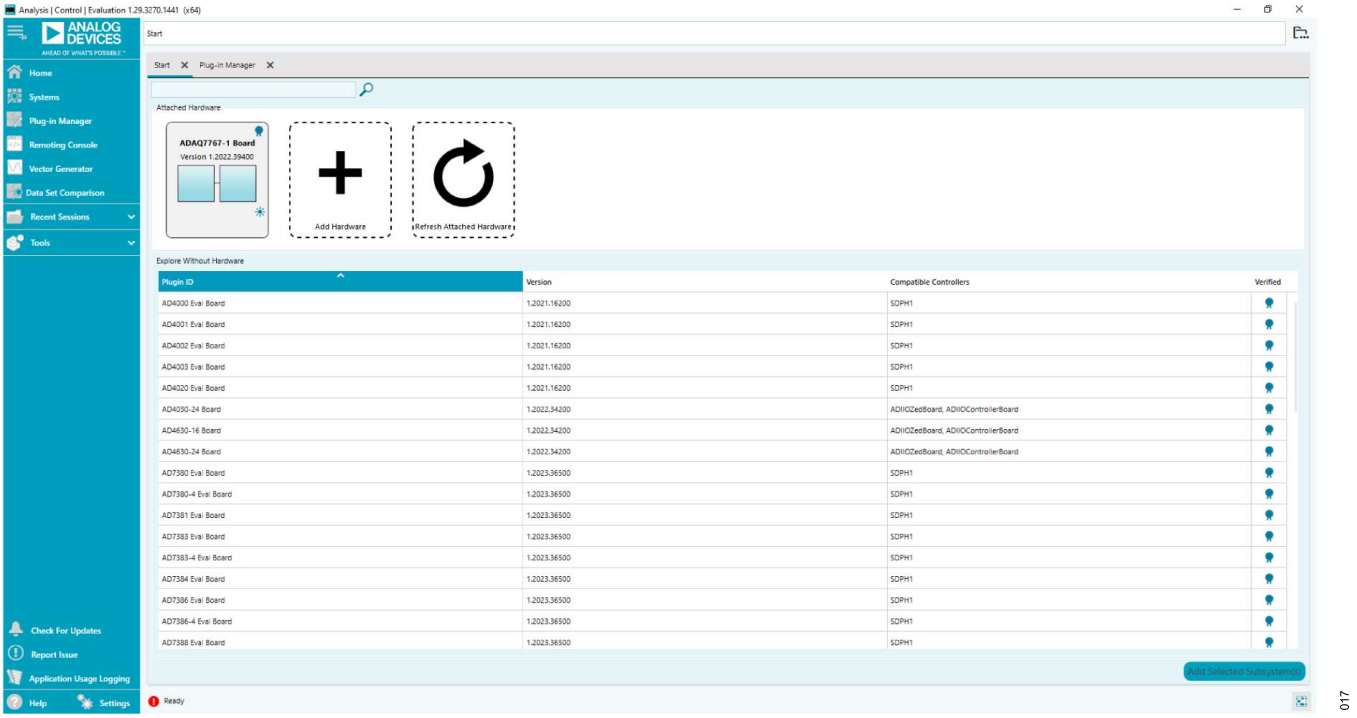
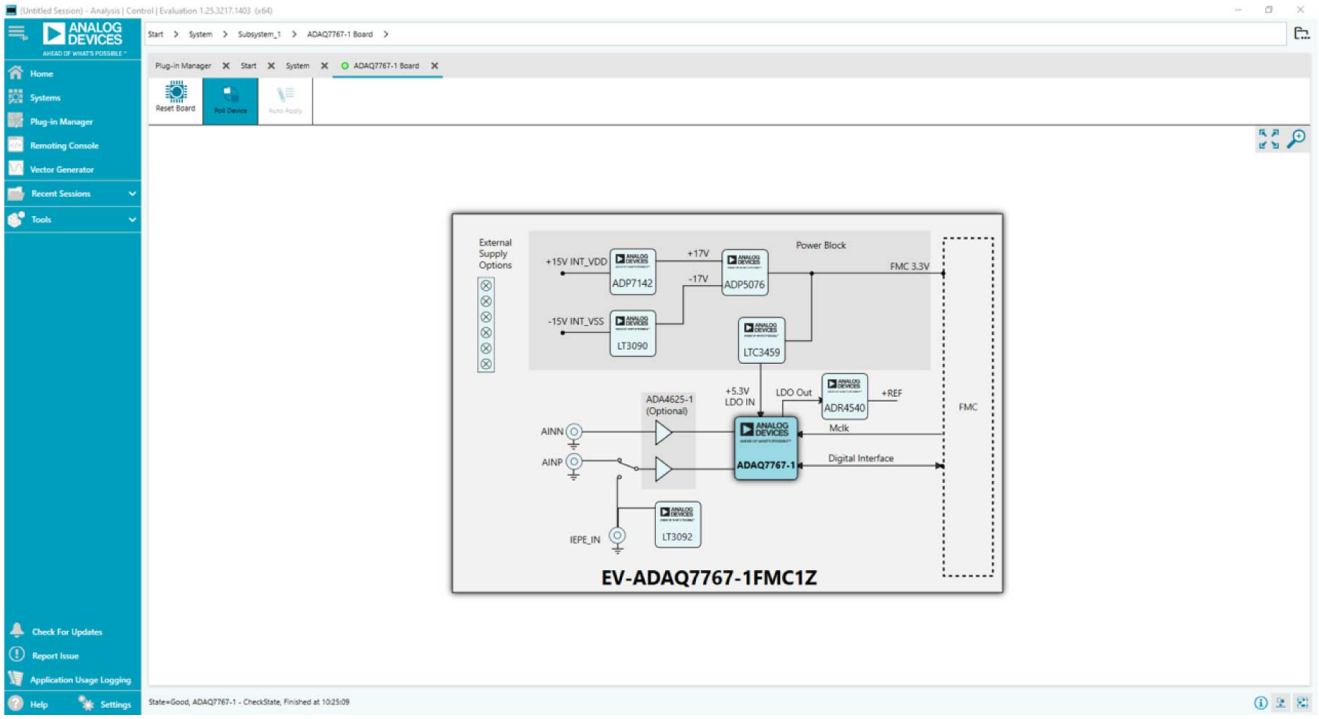


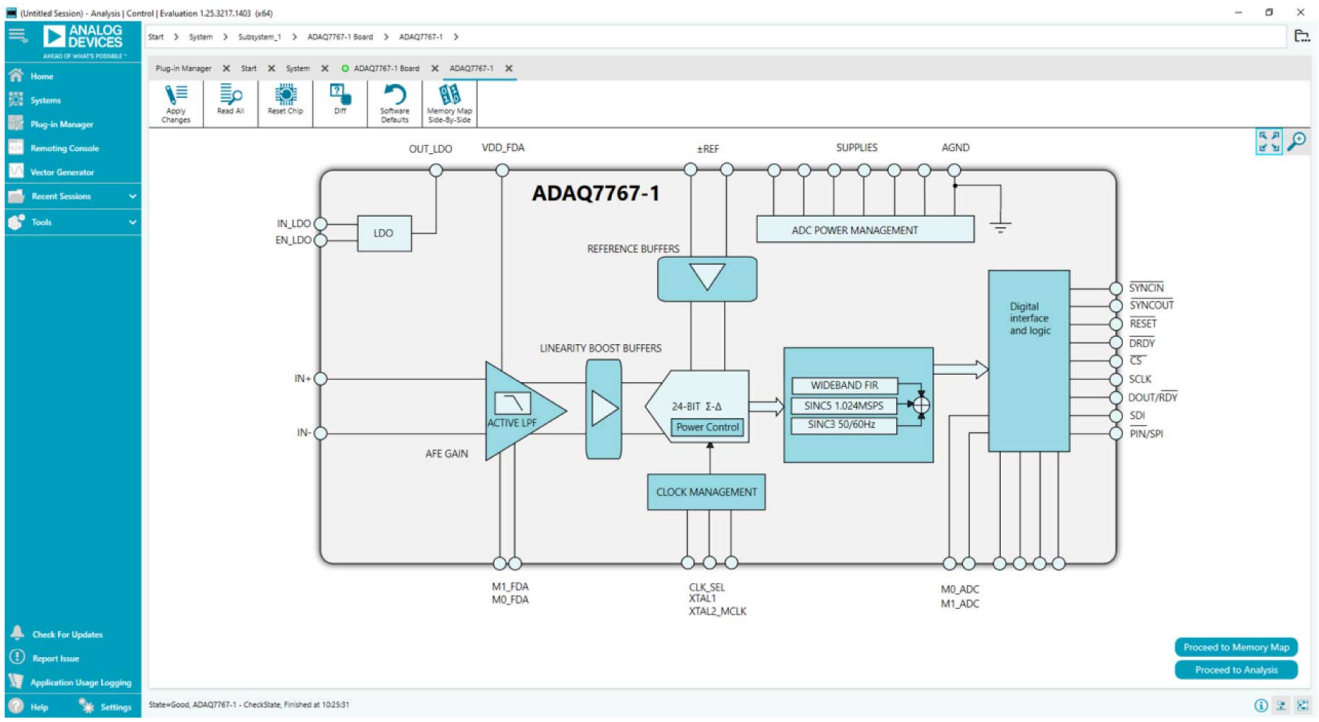
Figure 17. ADAQ7767-1 Board ACE Software Main Window

EVALUATION BOARD SOFTWARE



018

Figure 18. ADAQ7767-1 Board View



019

Figure 19. ADAQ7767-1 Board Chip View

EVALUATION BOARD SOFTWARE

DESCRIPTION OF THE ANALYSIS WINDOW

Click **Proceed to Analysis** in the **ADAQ7767-1 Board Chip View** window (see Figure 19) to open the **ADAQ7767-1 Board Analysis** window. The **ADAQ7767-1 Board Analysis** window showcases the performance of the EV-ADAQ7767-1FMC1Z. Before performing any measurements, set the **CAPTURE SETTINGS** and **ANALYSIS** settings.

The **ADAQ7767-1 Board Analysis** window contains the **ADAQ7767-1 Board Waveform** (see Figure 21), **ADAQ7767-1 Board Histogram** (see Figure 22), and **ADAQ7767-1 Board FFT** tabs (see Figure 23).

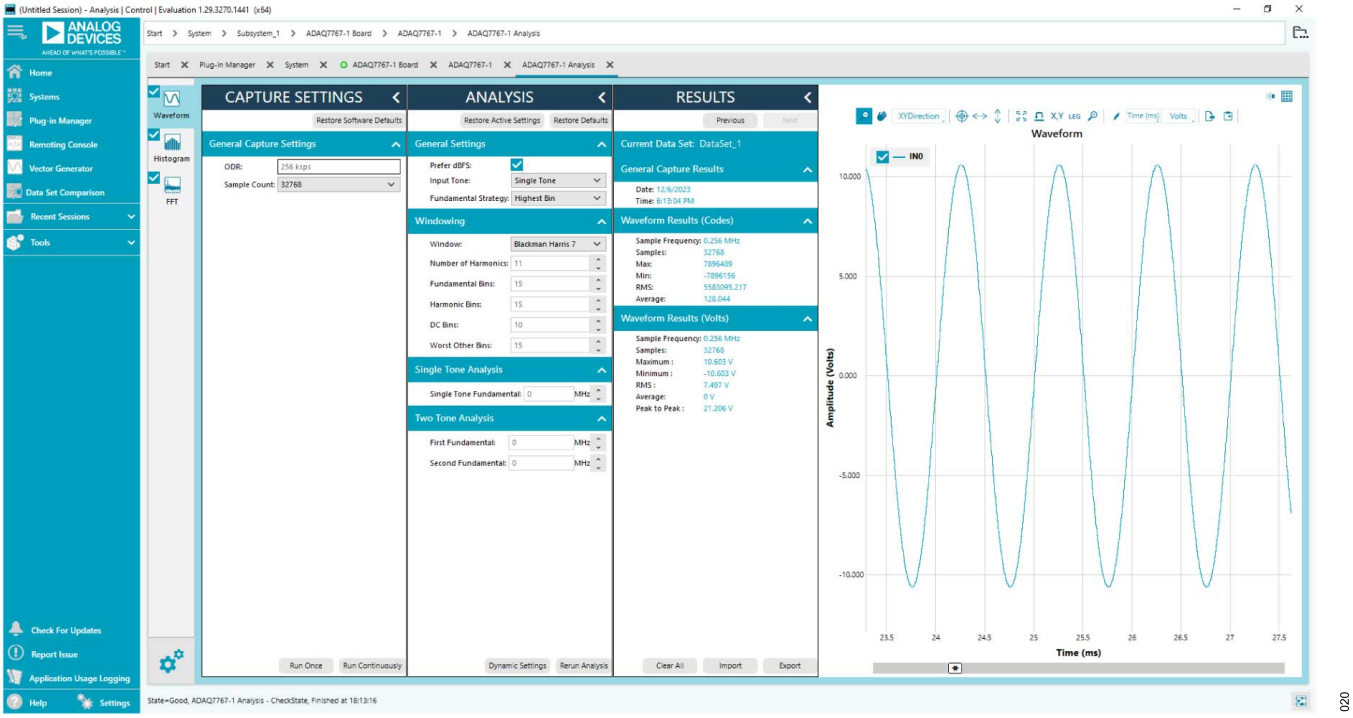


Figure 20. ADAQ7767-1 Board Analysis Window

EVALUATION BOARD SOFTWARE

CAPTURE SETTINGS

The output data rate (**ODR:**) is automatically calculated by the software based on the selected ADC filter settings. By default, **ODR:** is set to 256 kSPS (see Figure 20).

The **Sample Count:** is set to 8192 samples by default, but it can be changed to a selection from the dropdown menu, ranging from 512 to 131072 samples.

Click **Run Once** in the **CAPTURE SETTINGS** section to start a data capture of the samples at the sample rate specified in the **Sample Count** dropdown menu. These samples are stored on the FPGA device and are only transferred to the PC when the sample frame is complete.

Click **Run Continuously** in the **CAPTURE SETTINGS** section to start a data capture that gathers samples continuously with one batch of data at a time, which runs the **Run Once** operation continuously.

ANALYSIS

The **General Settings** section sets up the preferred configuration of the fast Fourier transform (FFT) analysis. This configuration sets the number of tones to analyze and the fundamental strategy to use (see Figure 20).

The **Windowing** section sets up the preferred **Window** type to use in the FFT analysis. This section also configures the other parameters to include in the analysis (that is, the **Number of Harmonics**, **Fundamental Bins**, **Harmonic Bins**, **DC Bins**, and **Worst Other Bins**).

The **Single Tone Analysis** and **Two Tone Analysis** sections set up the fundamental frequencies included in the FFT analysis. When analyzing one frequency, use the **Single Tone Analysis section,** and when analyzing two frequencies, use the **Two-Tone Analysis** section.

RESULTS

Click **Export** to export the captured data. The waveform, histogram, and FFT data are stored in .xml files along with the values of the parameters at capture (see Figure 20).

ADAQ7767-1 Board Waveform Tab

The **Waveform Results (Volts)** section displays time domain characteristics of the signal, such as **Sample Frequency**, **Samples**, **Maximum**, **Minimum**, **RMS**, **Average**, and **Peak-to-Peak**.

The waveform graph shows each successive sample of the µModule output. The user can zoom in on and pan across the waveform using the embedded waveform tools.

Within the dropdown menu of the display unit (shown with the **Volts** option selected in Figure 21) select whether the data graph displays in units of hexadecimal, volts, or codes. The axis controls are dynamic.

When selecting either the y-scale dynamic or x-scale dynamic, the corresponding axis width automatically adjusts to show the entire range of the µModule results after each batch of samples.

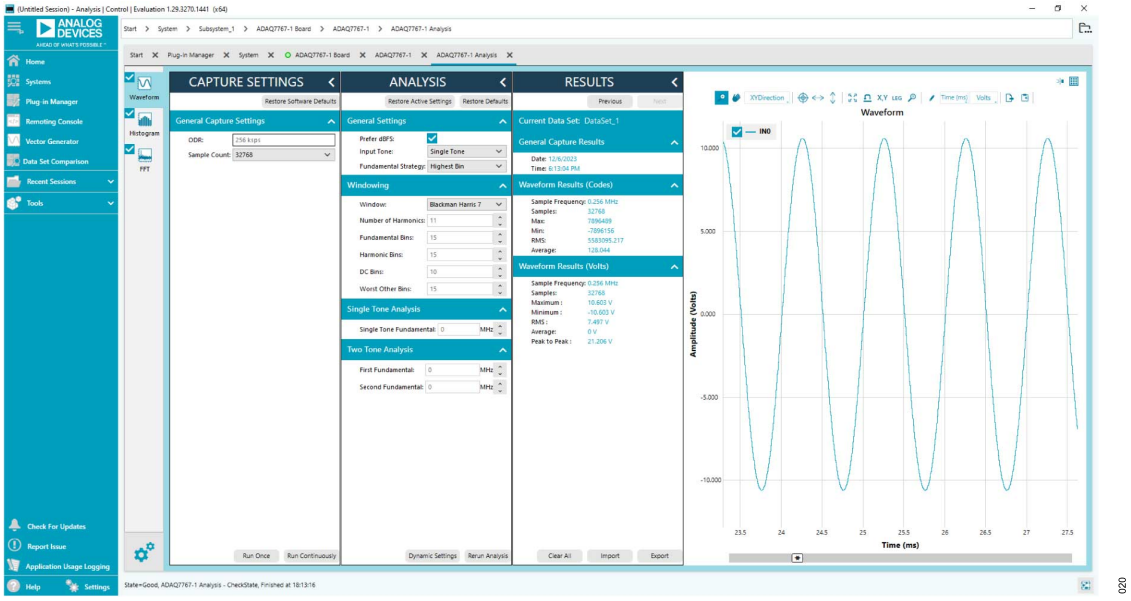


Figure 21. ADAQ7767-1 Board Waveform

EVALUATION BOARD SOFTWARE

ADAQ7767-1 Board Histogram Tab

The **ADAQ7767-1 Board Histogram** tab contains the **Histogram** graph and the **RESULTS** pane, as shown in Figure 22.

The **RESULTS** pane displays the information related to DC performance.

The **Histogram** graph displays the number of hits per code within the sampled data. This graph is useful for DC analysis and indicates the noise performance of the device.

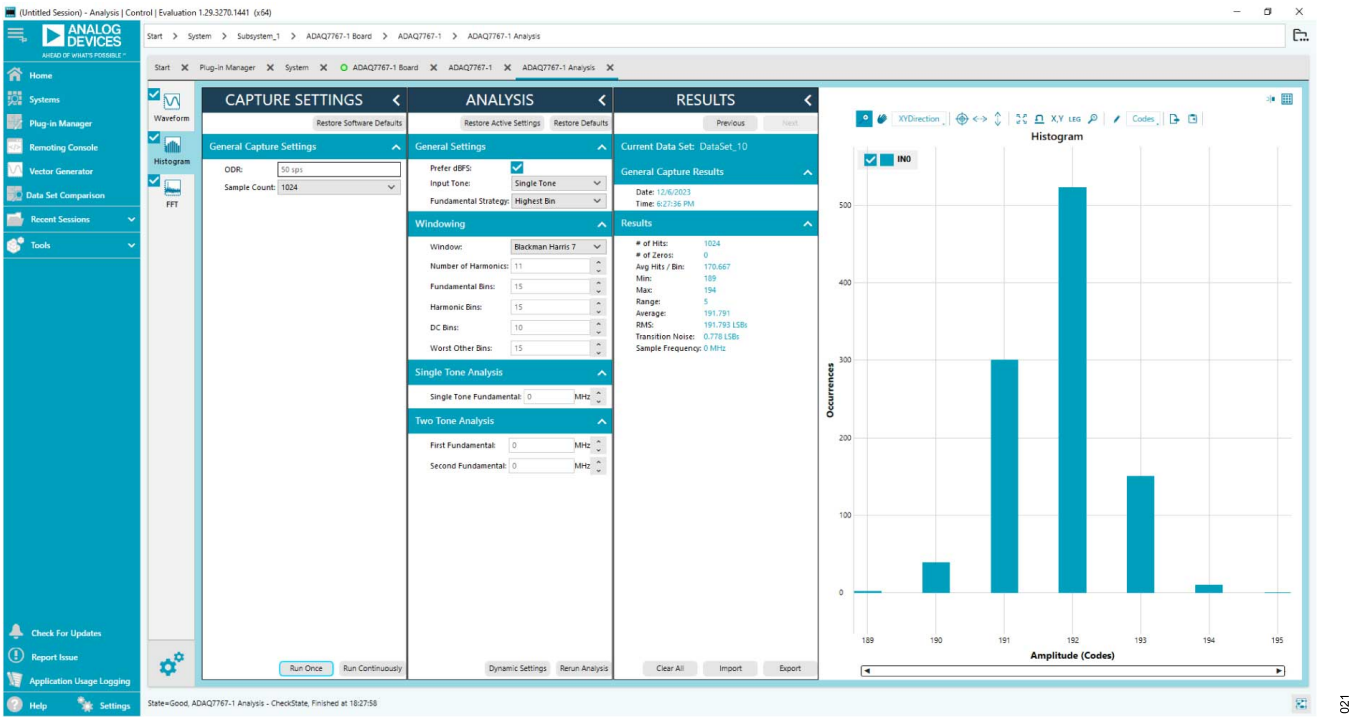


Figure 22. ADAQ7767-1 Board Histogram

EVALUATION BOARD SOFTWARE

ADAQ7767-1 Board FFT Tab

The **ADAQ7767-1 Board FFT** tab displays FFT information for the last batch of samples gathered, as shown in Figure 23 and Figure 24.

The **Signal** section displays the fundamental frequency (**Fund Frequency**) and fundamental power (**Fund Power**). The **Noise** section displays the signal-to-noise ratio (**SNR**) and other noise performance results. The **Distortion** section displays the harmonic content of the sampled signal, and the **DC** section displays the **DC Power** when viewing the FFT analysis.

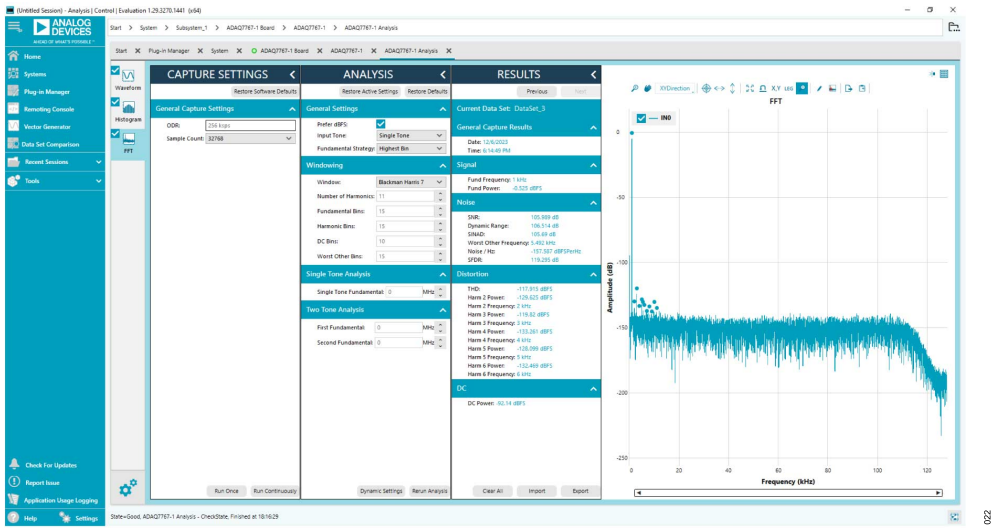


Figure 23. ADAQ7767-1 Board FFT Without Buffers

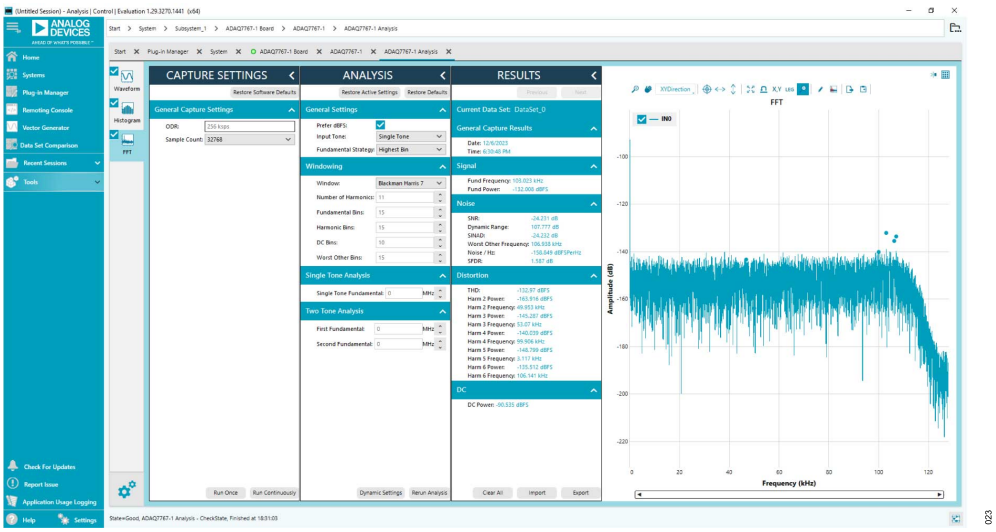


Figure 24. ADAQ7767-1 Board FFT with Shorted Inputs

EVALUATION BOARD SOFTWARE

EXITING THE SOFTWARE

To exit the software, go to **File** in the upper right tab and then click **Close ACE**.

CONFIGURING THE EV-ADAQ7767-1FMC1Z AND THE ADAQ7767-1

Input Range Configuration

To select the input range, take the following steps:

1. Configure the P1 and P2 jumpers on the EV-ADAQ7767-1FMC1Z to either IN1+ and IN1−, IN2+ and IN2−, or IN3+ and IN3−.
2. To properly detect and scale the applied input voltage when displaying results in volts, in the **ADAQ7767-1 Board Chip View** of the **ACE Software**, click on the **ACTIVE LPF** and select the corresponding input range, and then click **Apply Changes** (see Figure 25).

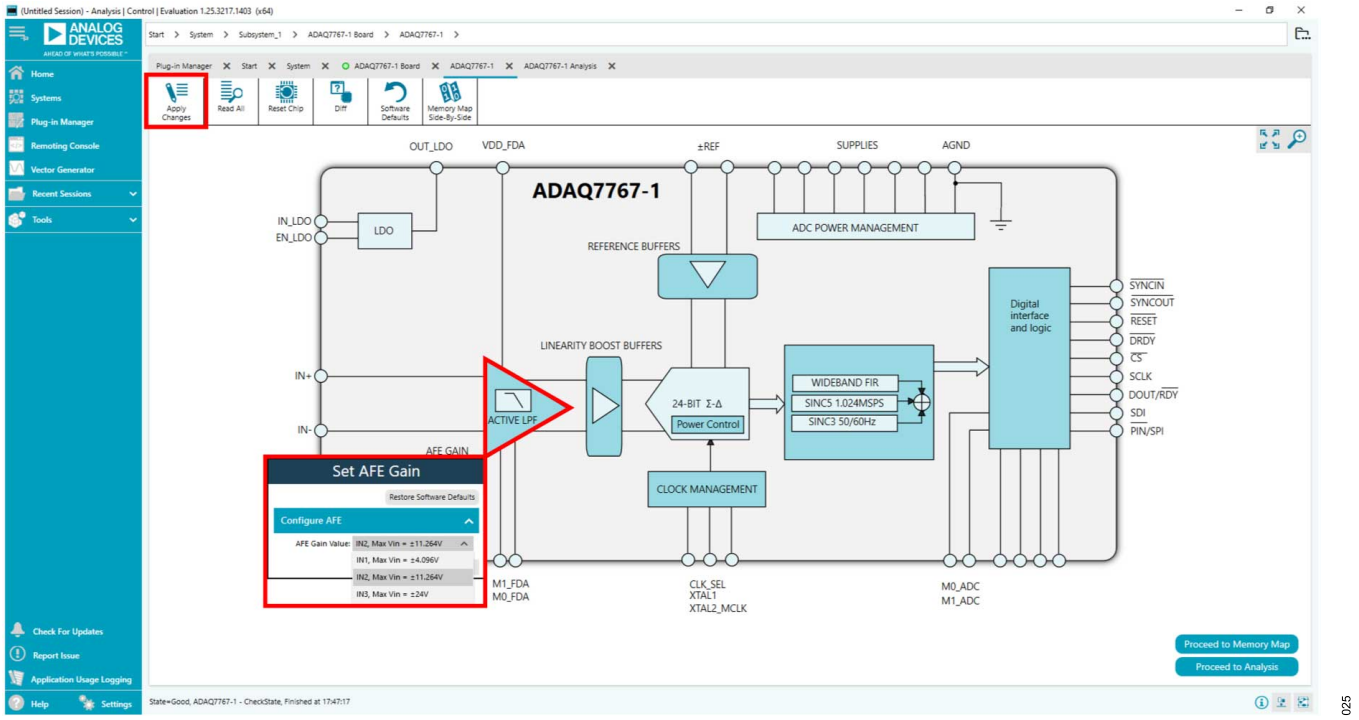


Figure 25. Input Range Selection Menu

EVALUATION BOARD SOFTWARE

ADC Configuration

Apart from the input range, other settings configurable from the **ADAQ7767-1 Board Chip View** pertain to the core ADC settings (see Figure 19). Applied changes to the core ADC through the **ADAQ7767-1 Board Chip View** are automatically reflected in their respective registers, which can also be read or written through the **ADAQ7767-1 Board Memory Map** (see Figure 26). The **ADAQ7767-1 Board Memory Map** contains the complete list of registers.

The following are the core ADC settings configurable in **ADAQ7767-1 Board Chip View**:

- **LINEARITY BOOST BUFFERS**
- **REFERENCE BUFFERS**
- **Power Control**
- **CLOCK MANAGEMENT**
- Filter configuration (see **WIDEBAND FIR** box in Figure 19)
- **Digital interface and logic**

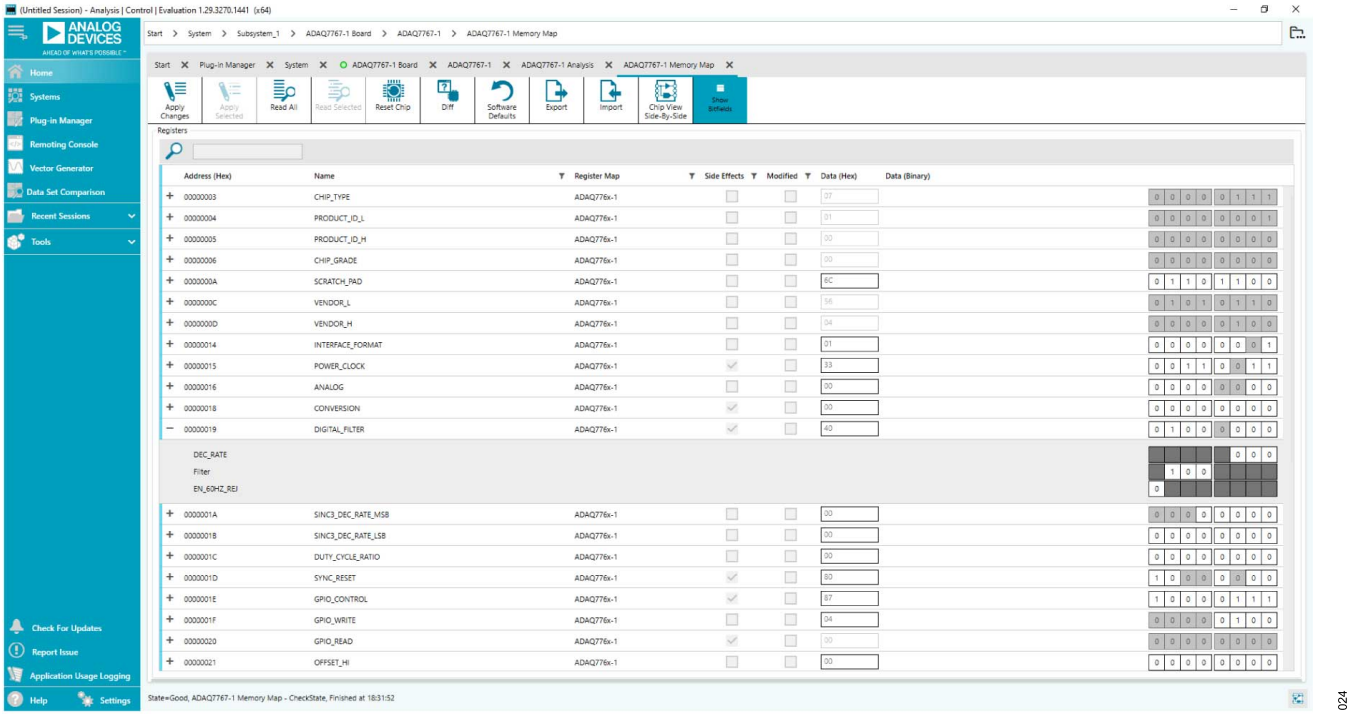


Figure 26. ADAQ7767-1 Board Memory Map

EVALUATION BOARD SOFTWARE

Reset Switches

Press the S1 switch to reset the DUT. Resetting the DUT resets all register settings to their default values.

A reset switch is also available on the SDP-H1 to reset the controller board. Note that resetting the controller board results in losing communication with the DUT.

The user can restart the software tool to re-initialize the EV-ADAQ7767-1FMC1Z.

EXAMPLE DATA CAPTURE

For an example data capture, see the Quick Start Guide section.

NOTES

ESD Caution
ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

Legal Terms and Conditions
By using the evaluation board discussed herein (together with any tools, components documentation or support materials, the "Evaluation Board"), you are agreeing to be bound by the terms and conditions set forth below ("Agreement") unless you have purchased the Evaluation Board, in which case the Analog Devices Standard Terms and Conditions of Sale shall govern. Do not use the Evaluation Board until you have read and agreed to the Agreement. Your use of the Evaluation Board shall signify your acceptance of the Agreement. This Agreement is made by and between you ("Customer") and Analog Devices, Inc. ("ADI"), with its principal place of business at Subject to the terms and conditions of the Agreement, ADI hereby grants to Customer a free, limited, personal, temporary, non-exclusive, non-sublicensable, non-transferable license to use the Evaluation Board FOR EVALUATION PURPOSES ONLY. Customer understands and agrees that the Evaluation Board is provided for the sole and exclusive purpose referenced above, and agrees not to use the Evaluation Board for any other purpose. Furthermore, the license granted is expressly made subject to the following additional limitations: Customer shall not (i) rent, lease, display, sell, transfer, assign, sublicense, or distribute the Evaluation Board; and (ii) permit any Third Party to access the Evaluation Board. As used herein, the term "Third Party" includes any entity other than ADI, Customer, their employees, affiliates and in-house consultants. The Evaluation Board is NOT sold to Customer; all rights not expressly granted herein, including ownership of the Evaluation Board, are reserved by ADI. CONFIDENTIALITY. This Agreement and the Evaluation Board shall all be considered the confidential and proprietary information of ADI. Customer may not disclose or transfer any portion of the Evaluation Board to any other party for any reason. Upon discontinuation of use of the Evaluation Board or termination of this Agreement, Customer agrees to promptly return the Evaluation Board to ADI. ADDITIONAL RESTRICTIONS. Customer may not disassemble, decompile or reverse engineer chips on the Evaluation Board. Customer shall inform ADI of any occurred damages or any modifications or alterations it makes to the Evaluation Board, including but not limited to soldering or any other activity that affects the material content of the Evaluation Board. Modifications to the Evaluation Board must comply with applicable law, including but not limited to the RoHS Directive. TERMINATION. ADI may terminate this Agreement at any time upon giving written notice to Customer. Customer agrees to return to ADI the Evaluation Board at that time. LIMITATION OF LIABILITY. THE EVALUATION BOARD PROVIDED HEREUNDER IS PROVIDED "AS IS" AND ADI MAKES NO WARRANTIES OR REPRESENTATIONS OF ANY KIND WITH RESPECT TO IT. ADI SPECIFICALLY DISCLAIMS ANY REPRESENTATIONS, ENDORSEMENTS, GUARANTEES, OR WARRANTIES, EXPRESS OR IMPLIED, RELATED TO THE EVALUATION BOARD INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTY OF MERCHANTABILITY, TITLE, FITNESS FOR A PARTICULAR PURPOSE OR NONINFRINGEMENT OF INTELLECTUAL PROPERTY RIGHTS. IN NO EVENT WILL ADI AND ITS LICENSORS BE LIABLE FOR ANY INCIDENTAL, SPECIAL, INDIRECT, OR CONSEQUENTIAL DAMAGES RESULTING FROM CUSTOMER'S POSSESSION OR USE OF THE EVALUATION BOARD, INCLUDING BUT NOT LIMITED TO LOST PROFITS, DELAY COSTS, LABOR COSTS OR LOSS OF GOODWILL. ADI'S TOTAL LIABILITY FROM ANY AND ALL CAUSES SHALL BE LIMITED TO THE AMOUNT OF ONE HUNDRED US DOLLARS ($100.00). EXPORT. Customer agrees that it will not directly or indirectly export the Evaluation Board to another country, and that it will comply with all applicable United States federal laws and regulations relating to exports. GOVERNING LAW. This Agreement shall be governed by and construed in accordance with the substantive laws of the Commonwealth of Massachusetts (excluding conflict of law rules). Any legal action regarding this Agreement will be heard in the state or federal courts having jurisdiction in Suffolk County, Massachusetts, and Customer hereby submits to the personal jurisdiction and venue of such courts. The United Nations Convention on Contracts for the International Sale of Goods shall not apply to this Agreement and is expressly disclaimed.

©2024 Analog Devices, Inc. All rights reserved. Trademarks and registered trademarks are the property of their respective owners.
One Analog Way, Wilmington, MA 01887-2356, U.S.A.