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AK7604

Audio DSP with 2chADC + 6chDAC + 8chSRC

1. General Description

The AK7604 is a highly integrated digital signal processor, including a 24-bit stereo ADC with input selector, three 24-bit stereo DACs, four stereo sampling rate convertors supporting the sampling frequency up to 192kHz and an Audio DSP. The Audio DSP has 2560step/fs (when fs=48kHz) parallel processing power and freely programmable for user requirements. The AK7604 is available in a 48-pin LQFP package.

2. Features

□ **Audio DSP:**
- **Word length:** 28-bit (Simple floating point supported)
- **Instruction cycle:** Max. 8.1ns (2560fs at fs=48kHz)
- **Multiplier:** 24 x 24 → 48-bit (Double precision arithmetic available)
- **Divider:** 24 / 24 → 24-bit (Floating point normalization function)
- **ALU:** 64-bit Arithmetic Operation (with 16bits overflow margin)
- **Program RAM:** 1024-word x 36-bit
- **Coefficient RAM:** 1024-word x 24-bit
- **Data RAM:** 6144-word x 28-bit

□ **ADC: 24-bit Stereo ADC with Input Selector**
- **Sampling Frequency: fs = 8kHz ~ 96kHz**
- **Input Selector:** Differential Stereo Input or Single-end Input or Pseudo Differential Input with Analog Gain Amplifiers x 1, Single-ended Stereo Input x 2
- **Channel Independent Analog Gain Amplifiers (0~18dB(2dB Step), 18~36dB(3dB Step))**
- **ADC Characteristics** S/N: 106dB (fs=48kHz, Differential Input, Analog Gain=0dB)
- **Channel Independent Digital Volume Control (24dB ~ -103dB, 0.5dB Step, Mute)**
- **Digital HPF for DC Offset Cancelling**
- **1Vrms Input Full Scale**
- **Low Noise MIC Power Output x 2**

□ **DAC: 24-bit DAC**
- **2ch x 3**
- **Sampling Frequency: fs = 8kHz ~ 96kHz**
- **Single-ended Output**
- **1Vrms Output**
- **DAC Characteristics** S/N: 108dB (fs=48kHz)
- **Channel Independent Digital Volume Control (12dB ~ -115dB, 0.5dB Step, Mute)**

□ **SRC:**
- **2ch x 4**
- **FSI = 8kHz ~ 192kHz, FSO = 8kHz ~ 192kHz (FSO/FSI = 0.167 ~ 6.0)**

□ **Digital Interfaces**
- **Digital Input Port x 4 (TDM Support: 1 Port)**
- **Digital Output Port x 3 (TDM Support: 1 Port)**
- **Independent LRCK/BICK port x 3**
- **Data Format: MSB 32, 24bit / LSB 24, 20, 16bit / I²S / PCM Short Frame / PCM Long Frame**
- **TDM Input/Output Mode (Max: 8ch/256fs, fs=96kHz)**

□ PLL Circuit
□ µP Interface: SPI(Max.6MHz) / I²C(400kHz Fast Mode)
□ Power Supply:

Analog:	**AVDD:**	**3.0V ~ 3.6V (Typ. 3.3V)**
Digital:	**LVDD:**	**3.0V ~ 3.6V (Typ. 3.3V) (3.3V → 1.2V Internal Regulator)**
I/F	**VDD33:**	**3.0V ~ 3.6V (Typ. 3.3V)**
	TVDD:	**1.7V ~ 3.6V (Typ. 3.3V)**

□Operating Temperature Range: -40 ~ 85°C
□Package: 48-pin LQFP (7mm x 7mm, 0.5mm pitch)

3. Table of Contents

4. Block Diagrams

■ Block Diagram

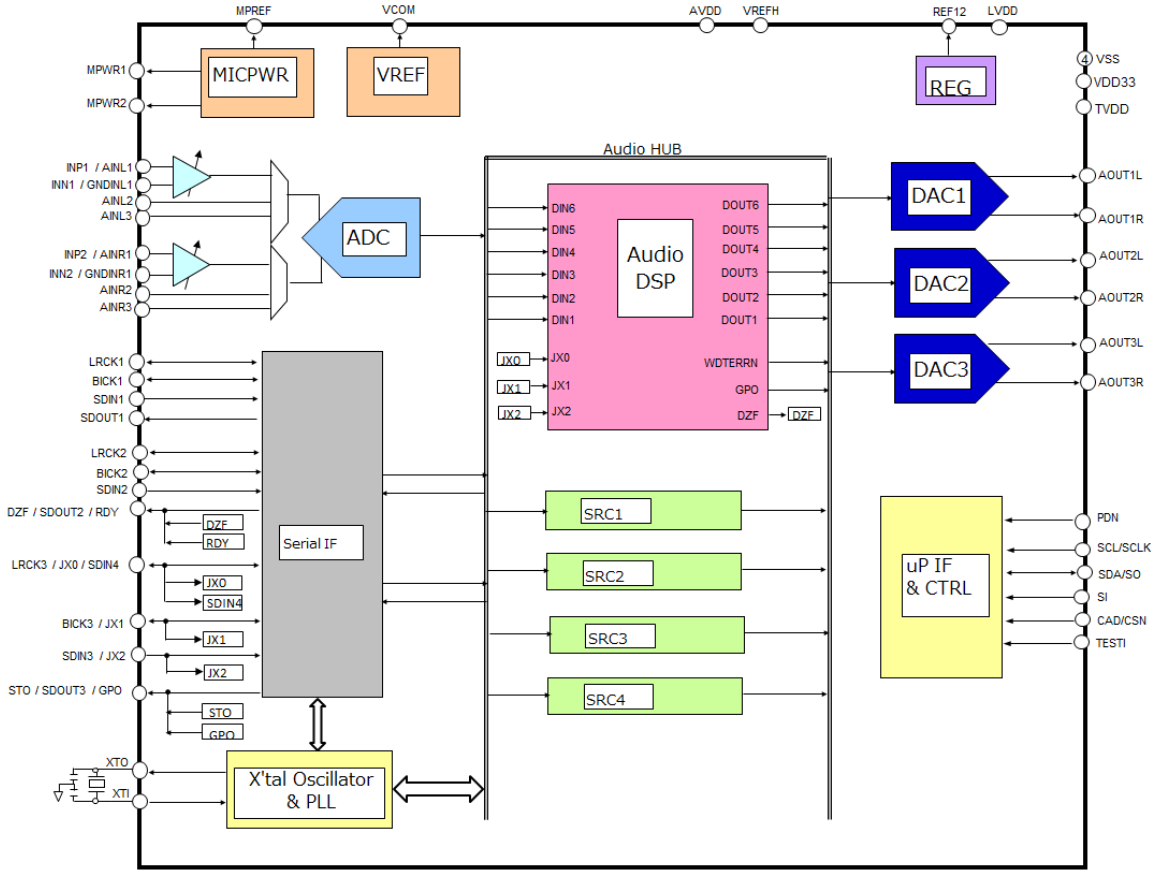
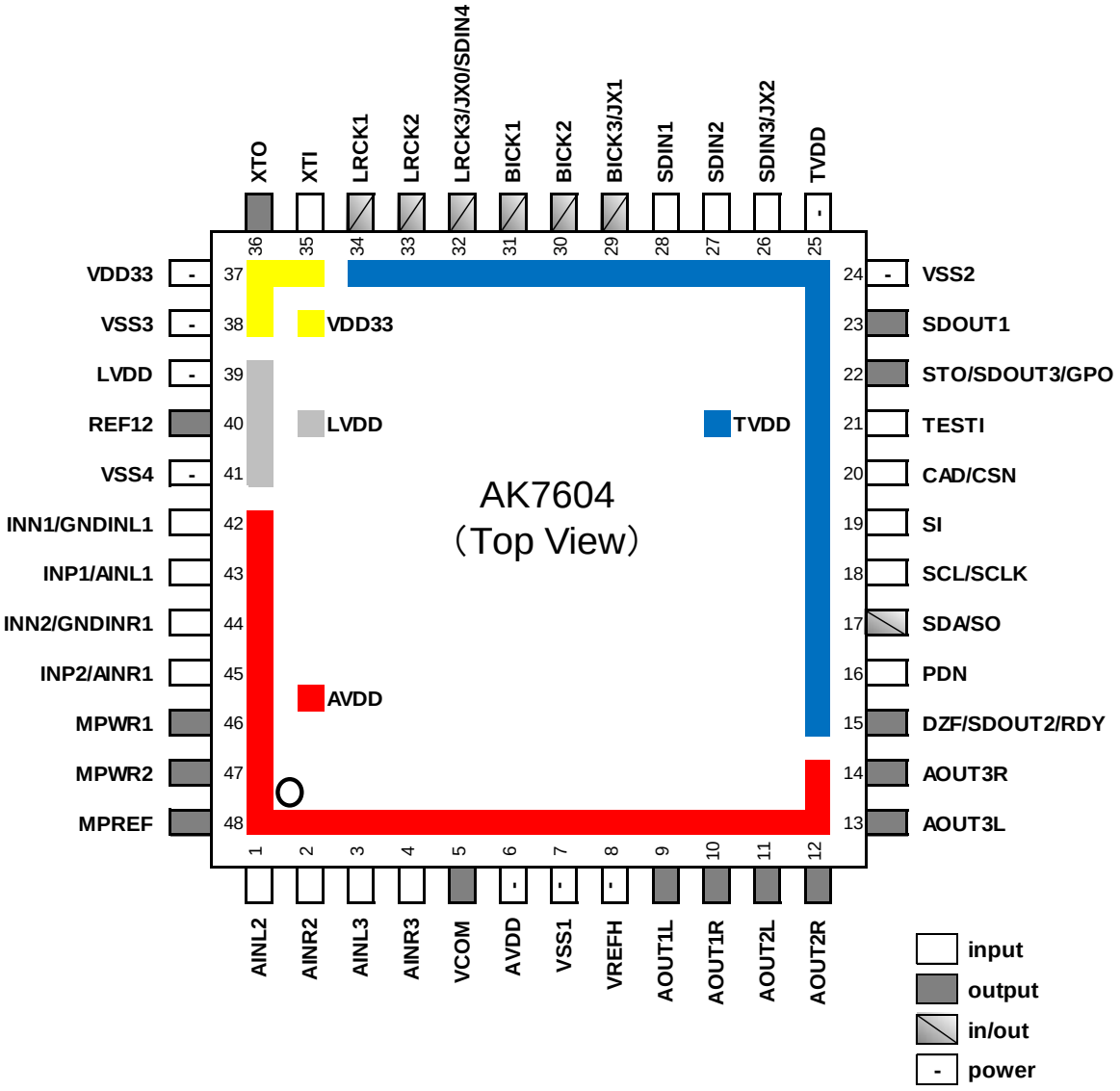


Figure 1. Block Diagram

5. Pin Configurations and Functions

■ Pin Configurations



■ **Pin Functions**

No.	Pin Name	I/O	Function	Power Supply
1	AINL2	I	Lch Single-ended Input 2 Pin	AVDD
2	AINR2	I	Rch Single-ended Input 2 Pin	AVDD
3	AINL3	I	Lch Single-ended Input 3 Pin	AVDD
4	AINR3	I	Rch Single-ended Input 3 Pin	AVDD
5	VCOM	O	Analog Common Voltage Output Pin Connect a 2.2μF ceramic capacitor between this pin and VSS1. This pin outputs "L" during power-down state. Do not connect this pin to an external circuit.	AVDD
6	AVDD	-	Analog Power Supply Pin 3.0~3.6V (typ.3.3V)	-
7	VSS1	-	Ground Pin, 0V	-
8	VREFH	-	Analog High-level Reference Voltage Input Pin Connect this pin to AVDD.	AVDD
9	AOUT1L	O	DAC1 Lch Analog Output Pin This pin outputs "Hi-Z" during power-down state.	AVDD
10	AOUT1R	O	DAC1 Rch Analog Output Pin This pin outputs "Hi-Z" during power-down state.	AVDD
11	AOUT2L	O	DAC2 Lch Analog Output Pin This pin outputs "Hi-Z" during power-down state.	AVDD
12	AOUT2R	O	DAC2 Rch Analog Output Pin This pin outputs "Hi-Z" during power-down state.	AVDD
13	AOUT3L	O	DAC3 Lch Analog Output Pin This pin outputs "Hi-Z" during power-down state.	AVDD
14	AOUT3R	O	DAC3 Rch Analog Output Pin This pin outputs "Hi-Z" during power-down state.	AVDD
15	DZF	O	Soft Defined Zero Detect Pin (GPO0 Output of DSP)	TVDD
	SDOUT2	O	Serial Data Output 2 Pin	
	RDY	O	RDY Signal Output Pin	
16	PDN	I	Power-Down & Reset Pin When "L", the AK7604 is powered-down and the control registers are reset to default state. The PDN pin should be "L" until all power supplies are ON, then put the PDN pin to "H".	TVDD
17	SDA	I/O	Serial Data In/Output Pin for I^2C I/F This pin outputs "Hi-Z" during power-down state.	TVDD
	SO	O	Serial Data Output Pin for SPI I/F This pin outputs "Hi-Z" during power-down state. This pin must be pulled up or pulled down.	TVDD
18	SCL	I	Serial Data Clock Input Pin for I^2C I/F	TVDD
	SCLK	I	Serial Data Clock Input Pin for SPI I/F	
19	SI	I	Serial Data Input Pin for SPI I/F	TVDD
20	CAD	I	I^2C I/F Chip Address Pin This pin must be pulled up or pulled down.	TVDD
	CSN	I	SPI I/F Chip Select Pin During power-down state or when SPI I/F is not in use, leave this pin "H" level.	
21	TESTI	I	Test Input Pin It must be tied "L".	TVDD
22	STO	O	Status Output Pin This pin outputs "L" during power-down state.	TVDD
	SDOUT3	O	Serial Data Output 3 Pin	
	GPO	O	DSP GPO Output Pin (GPO1 Output of DSP)	

No.	Pin Name	I/O	Function	Power Supply
23	SDOUT1	O	Serial Data Output 1 Pin	TVDD
24	VSS2	-	Ground Pin, 0V	-
25	TVDD	-	Digital I/F Power Supply Pin 1.7~3.6V (typ.3.3V)	-
26	SDIN3	I	Serial Data Input 3 Pin	TVDD
	JX2	I	External Conditional Jump Input 2 Pin	TVDD
27	SDIN2	I	Serial Data Input 2 Pin	TVDD
28	SDIN1	I	Serial Data Input 1 Pin	TVDD
29	BICK3	I/O	Serial Bit Clock 3 Pin	TVDD
	JX1	I	External Conditional Jump Input 1 Pin	TVDD
30	BICK2	I/O	Serial Bit Clock 2 Pin	TVDD
31	BICK1	I/O	Serial Bit Clock 1 Pin	TVDD
32	LRCK3	I/O	LR Channel Select Clock 3 Pin	TVDD
	JX0	I	External Conditional Jump Input 0 Pin	
	SDIN4	I	Serial Data Input 4 Pin	
33	LRCK2	I/O	LR Channel Select Clock 2 Pin	TVDD
34	LRCK1	I/O	LR Channel Select Clock 1 Pin	TVDD
35	XTI	I	Crystal Oscillator Input Pin When using a X'tal oscillator, connect it between the XTI and XTO pin. When not using XTI pin, leave this pin open.	VDD33
36	XTO	O	Crystal Oscillator Output Pin When using a X'tal oscillator, connect it between the XTI and XTO pin. When not using XTO pin, leave this pin open.	VDD33
37	VDD33	-	Digital Power Supply Pin 3.0~3.6V (typ.3.3V)	-
38	VSS3	-	Ground Pin 0V	-
39	LVDD	-	Digital Power Supply Pin 3.0~3.6V (typ.3.3V)	-
40	REF12	O	Internal regulator 1.2V Output pin Connect a 2.2μF(±30%) ceramic capacitor between this pin and VSS4. Do not connect this pin to an external circuit.	LVDD
41	VSS4	-	Ground Pin, 0V	-
42	INN1	I	ADC Lch Inverted Differential Input 1 Pin	AVDD
	GNDINL1	I	ADC Lch Pseudo Differential Ground Input 1 Pin	
43	INP1	I	ADC Lch Non-inverted Differential Input 1 Pin	AVDD
	AINL1	I	ADC Lch Single-ended Input 1 Pin	
44	INN2	I	ADC Rch Inverted Differential Input 2 Pin	AVDD
	GNDINR1	I	ADC Rch Pseudo Differential Ground Input 1 Pin	
45	INP2	I	ADC Rch Non-inverted Differential Input 2 Pin	AVDD
	AINR1	I	ADC Rch Single-ended Input 1 Pin	
46	MPWR1	O	Power Supply Output 1 Pin for Microphone This pin outputs "Hi-Z" during power-down state.	AVDD
47	MPWR2	O	Power Supply Output 2 Pin for Microphone This pin outputs "Hi-Z" during power-down state.	AVDD
48	MPREF	O	Ripple Filter Pin for Microphone Power Supply Connect a 1μF ceramic capacitor between this pin and VSS1. Do not connect this pin to an external circuit.	AVDD

■ Handling of Unused Pins

Unused I/O pins must be connected appropriately.

Table 1. Handling of Unused Pins

Classification	Pin Name	Setting
Analog	MPREF, MPWR1, MPWR2, INP1/AINL1, INN1/GNDINL1, INP2/AINR1, INN2/GNDINR1, AINL2, AINR2, AINL3, AINR3, AOUT1L, AOUT1R, AOUT2L, AOUT2R, AOUT3L, AOUT3R	Open
Digital	XTI, XTO, SDOUT1, DZF/SDOUT2/RDY, STO/SDOUT3/GPO	Open
	SDIN3/JX2, SDIN2, SDIN1, LRCK3/JX0/SDIN4, LRCK2, LRCK1, BICK3/JX1, BICK2, BICK1, TESTI	Connect to VSS2/VSS3

■ Internal Pulled-down Pins Status

Table 2. Internal Pulled-down Pins Status

No.	Pin Name	Power Down Status PDN pin = “L”	Power Down Release PDN pin = “H” (Slave mode)	Power Down Release PDN pin = “H” (Master mode)
21	TESTI	Pulled-down (25kΩ)	Pulled-down (25kΩ)	Pulled-down (25kΩ)
34	LRCK1	Pulled-down (50kΩ)	Input (Pulled-down) (46 kΩ)	Output
31	BICK1	Pulled-down (50kΩ)	Input (Pulled-down) (46 kΩ)	Output
33	LRCK2	Pulled-down (50kΩ)	Input (Pulled-down) (46 kΩ)	Output
30	BICK2	Pulled-down (50kΩ)	Input (Pulled-down) (46 kΩ)	Output
32	LRCK3/JX0/SDIN4	Pulled-down (50kΩ)	Input (Pulled-down) (46 kΩ)	Output
29	BICK3/JX1	Pulled-down (50kΩ)	Input (Pulled-down) (46 kΩ)	Output
23	SDOUT1	Pulled-down (50kΩ)	Output	Output
15	DZF/SDOUT2/RDY	Pulled-down (50kΩ)	Output	Output
22	STO/SDOUT3/GPO	Pulled-down (50kΩ)	Output	Output
40	REF12	Pulled-down (70Ω)	Output	Output

Note

* 1. Typical resistance value when LVDD=TVDD=VDD33=3.3V.

■ Power-down Status of Output Pins

Table 3. Power-down Status of Output Pins

No	Pin Name	I/O	Power-down Status	No	Pin Name	I/O	Power-down Status
5	VCOM	O	“L” Output	31	BICK1	I/O	Input
48	MPREF	O	“L” Output	33	LRCK2	I/O	Input
46	MPWR1	O	“Hi-Z” Output	30	BICK2	I/O	Input
47	MPWR2	O	“Hi-Z” Output	32	LRCK3/JX0/SDIN4	I/O	Input
9	AOUT1L	O	“Hi-Z” Output	29	BICK3/JX1	I/O	Input
10	AOUT1R	O	“Hi-Z” Output	17	SDA/SO	I/O	“Hi-Z” Output
11	AOUT2L	O	“Hi-Z” Output	23	SDOUT1	O	“L” Output (Pulled-down)
12	AOUT2R	O	“Hi-Z” Output	15	DZF/SDOUT2/RDY	O	“L” Output (Pulled-down)
13	AOUT3L	O	“Hi-Z” Output	22	STO/SDOUT3/GPO	O	“L” Output (Pulled-down)
14	AOUT3R	O	“Hi-Z” Output	36	XTO	O	“H” Output
34	LRCK1	I/O	Input	40	REF12	O	“L” Output (Pulled-down)

6. Absolute Maximum Ratings

(VSS1=VSS2=VSS3=VSS4=0V * 2)

Parameter	Symbol	Min.	Max.	Unit
Power Supplies				
Analog	AVDD	-0.3	4.3	V
Digital1(Core)	LVDD	-0.3	4.3	V
Digital2(I/F)	TVDD	-0.3	4.3	V
Digital3(I/F)	VDD33	-0.3	4.3	V
Input Current (except power supply pins)	IIN	—	±10	mA
Analog Input Voltage * 3	VINA	-0.3	(AVDD+0.3) or 4.3	V
Digital Input Voltage * 4	VIND1	-0.3	(TVDD+0.3) or 4.3	V
Digital Input Voltage * 5	VIND2	-0.3	(VDD33+0.3) or 4.3	V
Ambient Temperature	Ta	-40	85	°C
Storage Temperature	Tstg	-65	150	°C

Notes

* 2. All voltages are with respect to ground. VSS1-4 must be connected to the same ground.
* 3. The maximum analog input voltage is smaller value between (AVDD+0.3)V and 4.3V.
* 4. The maximum digital input voltage of SDIN1, SDIN2, SDIN3/JX2, LRCK1, BICK1, LRCK2, BICK2, LRCK3/JX0/SDIN4, BICK3/JX1, PDN, SCL/SCLK, CAD/CSN, SI a、nd TESTI pins is smaller value between (TVDD+0.3)V and 4.3V.
* 5. The maximum digital input voltage of XTI pin is smaller value between (VDD33+0.3)V and 4.3V.

WARNING: Operation at or beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

7. Recommended Operating Conditions

(VSS1=VSS2=VSS3=VSS4=0V * 2)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Power Supplies					
Analog	AVDD	3.0	3.3	3.6	V
Digital1(Core)	LVDD	3.0	3.3	3.6	V
Digital2(I/F)	TVDD	1.7	3.3	3.6	V
Digital3(I/F)	VDD33	3.0	3.3	3.6	V
Difference1	AVDD – LVDD	-0.1	0	0.1	V
Difference2	AVDD – VDD33	-0.1	0	0.1	V
Difference3	LVDD – VDD33	-0.1	0	0.1	V
Difference4	LVDD – TVDD	-0.1	-	-	V

Notes

* 6. The power-up sequence with AVDD, DVDD, TVDD and VDD33 is not critical. The PDN pin should be held “L” when power is supplied. The PDN pin is allowed to be “H” after all power supplies are applied and settled.
* 7. Do not turn off the power supply of the AK7604 with the power supply of the peripheral device turned on. When using the I^2C interface, pull-up resistors of SDA and SCL pins should be connected to TVDD or less voltage.

WARNING: AKM assumes no responsibility for the usage beyond the conditions in the datasheet.

8. Electrical Characteristics

■ Analog Characteristics

1. MIC AMP

(Ta=25°C; AVDD=LVDD=TVDD=VDD33=3.3V; VSS1=VSS2=VSS3=VSS4=0V)

	Parameter		Min.	Typ.	Max.	Unit
MIC AMP	Input Impedance (Full-differential)		17	25	33	kΩ
	Input Impedance (Pseudo, Single)		18	26	34	kΩ
	Gain	MGNL[3:0]bits=0H, MGNR[3:0]bits=0H	-1	0	1	dB
		MGNL[3:0]bits=1H, MGNR[3:0]bits=1H	1	2	3	
		MGNL[3:0]bits=2H, MGNR[3:0]bits=2H	3	4	5	
		MGNL[3:0]bits=3H, MGNR[3:0]bits=3H	5	6	7	
		MGNL[3:0]bits=4H, MGNR[3:0]bits=4H	7	8	9	
		MGNL[3:0]bits=5H, MGNR[3:0]bits=5H	9	10	11	
		MGNL[3:0]bits=6H, MGNR[3:0]bits=6H	11	12	13	
		MGNL[3:0]bits=7H, MGNR[3:0]bits=7H	13	14	15	
		MGNL[3:0]bits=8H, MGNR[3:0]bits=8H	15	16	17	
		MGNL[3:0]bits=9H, MGNR[3:0]bits=9H	17	18	19	
		MGNL[3:0]bits=AH, MGNR[3:0]bits=AH	20	21	22	
		MGNL[3:0]bits=BH, MGNR[3:0]bits=BH	23	24	25	
		MGNL[3:0]bits=CH, MGNR[3:0]bits=CH	26	27	28	
		MGNL[3:0]bits=DH, MGNR[3:0]bits=DH	29	30	31	
		MGNL[3:0]bits=EH, MGNR[3:0]bits=EH	32	33	34	
		MGNL[3:0]bits=FH, MGNR[3:0]bits=FH	35	36	37	

2. MIC Bias Output

(Ta=25°C; AVDD=LVDD=TVDD=VDD33=3.3V; VSS1=VSS2=VSS3=VSS4=0V;
Measurement Frequency =20Hz~20kHz)

	Parameter	Min.	Typ.	Max.	Unit
MIC Bias	Output Voltage	2.3	2.5	2.7	V
	Load Resistance	2			kΩ
	Load Capacitance			30	pF
	Output Noise (A-weighted)		-114	-108	dBV

3. MIC AMP + ADC

(Ta=25°C; AVDD=LVDD=TVDD=VDD33=3.3V; VSS1=VSS2=VSS3=VSS4=0V; Signal Frequency =1kHz; 24bit Data; BICK=64fs; @fs=48kHz, Measurement Frequency BW=20Hz ~ 20kHz; @fs=96kHz, BW=20Hz ~ 40kHz; MGNL/R[3:0] bits=0h (0dB); Differential Input, Unless otherwise specified.)

	Parameter		Min.	Typ.	Max.	Unit
MIC AMP + ADC	Resolution				24	Bit
	Input Full Scale Voltage * 8	Differential Input * 12	±2.55	±2.83	±3.11	Vpp
		Differential Input * 13	±0.321	±0.356	±0.391	
	Input Full Scale Voltage * 9	Single-ended / Pseudo Input * 12	2.55	2.83	3.11	Vpp
		Single-ended / Pseudo Input * 13	0.321	0.356	0.391	
	Input Full Scale Voltage * 10	Single-ended Input	2.55	2.83	3.11	Vpp
	S/(N+D) (-1dBFS)	fs=48kHz * 12	85	95		dB
		fs=48kHz * 13		87		
		fs=96kHz * 12		92		
		fs=96kHz * 13		84		
	Dynamic Range (-60dBFS)	fs=48kHz (A-weighted) * 12	98	106		dB
		fs=48kHz (A-weighted) * 13		95		
		fs=96kHz * 12		99		
		fs=96kHz * 13		89		
	S/N	fs=48kHz (A-weighted) * 12	98	106		dB
		fs=48kHz (A-weighted) * 13		95		
		fs=96kHz * 12		99		
		fs=96kHz * 13		89		
	Inter-Channel Isolation * 11		90	105		dB
	Channel Gain Mismatch			0.0	0.3	dB
	CMRR * 14		60	80		dB

Notes

* 8. INP1, INN1, INP2 and INN2 pins
* 9. AIN1L and AIN1R pins
* 10. AINL2, AINR2, AINL3, AINR3 pins.
* 11. Inter-channel Isolation with -1dBFS signal input.
* 12. Input full-scale voltage is proportional to AVDD (0.86 x AVDD) when MIC AMP Gain = 0dB.
* 13. Input full-scale voltage is proportional to AVDD (0.108 x AVDD) when MIC AMP Gain = +18dB.
* 14. Common mode rejection ratio when inputting 1kHz, 100mVpp sine wave to both differential inputs. The value refers to the case when input a 1kHz, ±100mVpp sine wave as differential input.

4. DAC

(Ta=25°C; AVDD=LVDD=TVDD=VDD33=3.3V; VSS1=VSS2=VSS3=VSS4=0V; Signal Frequency =1kHz; 24bit Data; BICK=64fs; @fs=48kHz, Measurement Frequency BW=20Hz ~ 20kHz; @fs=96kHz, Measurement Frequency BW=20Hz ~ 40kHz)

	Parameter		Min.	Typ.	Max.	Unit
DAC1 DAC2 DAC3	Resolution				24	bit
	Output Voltage * 15		2.55	2.83	3.11	Vpp
	S/(N+D) (0dBFS)	fs=48kHz	80	91		dB
		fs=96kHz		89		
	Dynamic Range (-60dBFS)	fs=48kHz (A-weighted)	100	108		dB
		fs=96kHz		101		
	S/N	fs=48kHz (A-weighted)	100	108		dB
		fs=96kHz		101		
	Inter-Channel Isolation (fin=1kHz) * 16		90	110		dB
	Channel Gain Mismatch			0.0	0.7	dB
	Load Resistance * 17		10			kΩ
	Load Capacitance				30	pF

Notes

* 15. The output voltage when 0dBFS signal input. The output voltage is proportional to AVDD (0.86 x AVDD).
* 16. Inter-channel isolation between Lch and Rch of each DAC when 0dBFS signal input. (AOUT1L and AOUT1R, AOUT2L and AOUT2R, and AOUT3L and AOUT3R)
* 17. to AC load

5. SRC

(Ta=25°C; AVDD=LVDD=TVDD=VDD33=3.3V; VSS1=VSS2=VSS3=VSS4=0V; Signal Frequency =1kHz; 24bit Data; Measurement Frequency BW=20Hz ~ FSO/2)

	Parameter	Symbol	Min.	Typ.	Max.	Unit
SRC	Resolution				24	bit
	Input Sample Rate	FSI	8		192 (* 18)	kHz
	Output Sample Rate	FSO	8		192	kHz
	THD+N (Input=1kHz, 0dBFS)					
	Audio Mode (SRCAUDx bit = "1", x=1~4)					
	FSO/FSI=192kHz/48kHz			-122		dB
	FSO/FSI=44.1kHz/48kHz			-125		dB
	FSO/FSI=48kHz/88.2kHz			-122		dB
	FSO/FSI=48kHz/96kHz			-133		dB
	FSO/FSI=44.1kHz/96kHz			-116		dB
	FSO/FSI=48kHz/192kHz			-133		dB
	FSO/FSI=8kHz/48kHz			-130		dB
	Voice Mode (SRCAUDx bit = "0", x=1~4)					
	FSO/FSI=24kHz/32kHz			-95		dB
	FSO/FSI=16kHz/24kHz			-98		dB
	FSO/FSI=24kHz/44.1kHz			-78		dB
	FSO/FSI=16kHz/44.1kHz			-69		dB
	FSO/FSI=8kHz/32kHz			-130		dB
	Dynamic Range (Input=1kHz, -60dBFS)					
	Audio Mode (SRCAUDx bit = "1" , x=1~4)					
	FSO/FSI=192kHz/48kHz			132		dB
	FSO/FSI=44.1kHz/48kHz			136		dB
	FSO/FSI=48kHz/88.2kHz			135		dB
	FSO/FSI=48kHz/96kHz			136		dB
	FSO/FSI=44.1kHz/96kHz			136		dB
	FSO/FSI=48kHz/192kHz			136		dB
	FSO/FSI=8kHz/48kHz			130		dB
	Voice Mode (SRCAUDx bit = "0" , x=1~4)					
	FSO/FSI=24kHz/32kHz			134		dB
	FSO/FSI=16kHz/24kHz			137		dB
	FSO/FSI=24kHz/44.1kHz			132		dB
	FSO/FSI=16kHz/44.1kHz			128		dB
	FSO/FSI=8kHz/32kHz			130		dB
	Dynamic Range (Input=1kHz, -60dBFS, A-weighted)					
	FSO/FSI=44.1kHz/48kHz		-	137	-	dB
	Ratio between Input and Output Sample Rate	FSO/FSI	0.167		6	-

Note

* 18. Set FSI Frequency of each operating SRC as the sum of the frequencies is below 384kHz. For example, if the frequency of FSI is 96kHz, four SRCs can operate at the same time, if the frequency of FSI is 192kHz, only two SRCs are allowed to operate at the same time.

■ Power Consumption

(Ta=25°C; AVDD=LVDD=VDD33=3.0~3.6V (Typ=3.3V, Max=3.6V); TVDD=1.7~3.6V (Typ=3.3V, Max=3.6V); VSS1=VSS2=VSS3=VSS4=0V; fs=96kHz; BICK=64fs; Master Mode; SDOUT1~3/LRCK1~3/BICK1~3=Output; C_L=20pF)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Power-Up * 19 (PDN pin = "H")	AVDD		28	42	mA
	LVDD		14.6	68	mA
	TVDD		4.5	7	mA
	VDD33		2	4	mA
Power-Down (PDN pin = "L")	AVDD		1		uA
	LVDD		10		uA
	TVDD		1		uA
	VDD33		1		uA

Note

* 19. The current of LVDD changes depending on the system frequency and contents of DSP program.

9. Digital Filter Characteristics

■ ADC Block

(Ta=-40 ~ 85°C; AVDD=3.0~3.6V; LVDD=3.0~3.6V; TVDD=1.7~3.6V; VDD33=3.0~3.6V; VSS1=VSS2=VSS3=VSS4=0V)

fs=48kHz

Parameter		Symbol	Min.	Typ.	Max.	Unit
SHARP ROLL-OFF						
Passband * 20	0dB ~ -0.06dB	PB	0		22.1	kHz
	-3.0dB	PB		23.7		kHz
Stopband * 20		SB	27.8			kHz
Stopband Attenuation		SA	85.0			dB
Group Delay Distortion : 0Hz~20kHz		ΔGD		0		1/fs
Group Delay * 21		GD		20.0		1/fs
ADC Digital Filter(HPF)						
Frequency Response	-3.0dB	FR		0.9		Hz

fs=96kHz

Parameter		Symbol	Min.	Typ.	Max.	Unit
SHARP ROLL-OFF						
Passband * 20	0dB ~ -0.06dB	PB	0		44.2	kHz
	-3.0dB	PB		47.5		kHz
Stopband * 20		SB	55.6			kHz
Stopband Attenuation		SA	85.0			dB
Group Delay Distortion : 0Hz~40kHz		ΔGD		0		1/fs
Group Delay * 21		GD		20.0		1/fs
ADC Digital Filter(HPF)						
Frequency Response	-3.0dB	FR		1.9		Hz

Notes

* 20. The passband and stopband frequencies are proportional to fs (sampling rate). High-pass filter characteristics are not included. A reference value of each gain amplitude is the maximum value of frequency response.
* 21. Delay time caused by the digital filter calculation. This time is measured from an analog signal input until 24-bit data of both channels are set into the output register. It includes group delay by HPF.

■ DAC Block

(Ta=-40 ~ 85°C; AVDD=3.0~3.6V; LVDD=3.0~3.6V; TVDD=1.7~3.6V; VDD33=3.0~3.6V; VSS1=VSS2=VSS3=VSS4=0V)

1. Sharp Roll-Off Filter (DASD bit = "0", DASL bit = "0")

fs=48kHz

Parameter		Symbol	Min.	Typ.	Max.	Unit
SHARP ROLL-OFF						
Passband * 22	±0.05dB	PB	0		21.7	kHz
	−3.0dB	PB		23.4		kHz
Passband Ripple * 23		PR	-0.0032		0.0032	dB
Stopband * 22		SB	26.3			kHz
Stopband Attenuation * 25, * 26		SA	80.0			dB
Group Delay * 24		GD		27.3		1/fs
Digital Filter + SCF + SMF * 25						
Frequency Response : 0 ~ 20.0kHz			-0.3		0.1	dB

fs=96kHz

Parameter		Symbol	Min.	Typ.	Max.	Unit
SHARP ROLL-OFF						
Passband * 22	±0.05dB	PB	0		43.5	kHz
	−3.0dB	PB		46.8		kHz
Passband Ripple * 23		PR	-0.0032		0.0032	dB
Stopband * 22		SB	52.5			kHz
Stopband Attenuation * 25, * 26		SA	80.0			dB
Group Delay * 24		GD		27.3		1/fs
Digital Filter + SCF + SMF * 25						
Frequency Response : 0 ~ 40.0kHz			-0.5		0.1	dB

Notes

* 22. The passband and stopband frequencies are proportional to fs (sampling rate).
"PB = 0.4535 × fs, SB = 0.546 × fs"
* 23. Pass-band gain amplitude of double over sampling filter at the first step of Interpolator.
* 24. Delay time caused by the digital filter calculation. This time is measured from setting of the 16/20/24 impulse data to the input registers to output of the analog peak signal.
* 25. The output level with a 1kHz, 0dB sine wave input is defined as 0dB.
* 26. Band width of Stopband Attenuation ranges from 0Hz to fs.

2. Slow Roll-Off Filter (DASD bit = “0”, DASL bit = “1”)

fs=48kHz

Parameter		Symbol	Min.	Typ.	Max.	Unit
SLOW ROLL-OFF						
Passband * 27	±0.05dB	PB	0		8.8	kHz
	−3.0dB	PB		19.8		kHz
Passband Ripple * 23		PR	-0.043		0.043	dB
Stopband * 27		SB	42.7			kHz
Stopband Attenuation * 25, * 26		SA	73.0			dB
Group Delay * 24		GD		6.8		1/fs
Digital Filter + SCF + SMF * 25						
Frequency Response : 0 ~ 20.0kHz			-5.0		0.1	dB

fs=96kHz

Parameter		Symbol	Min.	Typ.	Max.	Unit
SLOW ROLL-OFF						
Passband * 27	±0.05dB	PB	0		17.7	kHz
	−3.0dB	PB		39.5		kHz
Passband Ripple * 23		PR	-0.043		0.043	dB
Stopband * 27		SB	85.3			kHz
Stopband Attenuation * 25, * 26		SA	73.0			dB
Group Delay * 24		GD		6.8		1/fs
Digital Filter + SCF + SMF * 25						
Frequency Response : 0 ~ 40.0kHz			-5.2		0.1	dB

Note

* 27. The passband and stopband frequencies are proportional to fs (sampling rate).
“PB = 0.185 × fs, SB = 0.888 × fs”

3. Short Delay Sharp Roll-Off Filter (DASD bit = “1”, DASL bit = “0”)

fs=48kHz

Parameter		Symbol	Min.	Typ.	Max.	Unit
SHORT DELAY SHARP ROLL-OFF						
Passband * 22	±0.05dB	PB	0		21.7	kHz
	−3.0dB	PB		23.4		kHz
Passband Ripple * 23		PR	-0.0031		0.0031	dB
Stopband * 22		SB	26.3			kHz
Stopband Attenuation * 25, * 26		SA	80.0			dB
Group Delay * 24		GD		6.3		1/fs
Digital Filter + SCF + SMF * 25						
Frequency Response : 0 ~ 20.0kHz			-0.3		0.1	dB

fs=96kHz

Parameter		Symbol	Min.	Typ.	Max.	Unit
SHORT DELAY SHARP ROLL-OFF						
Passband * 22	±0.05dB	PB	0		43.5	kHz
	−3.0dB	PB		46.8		kHz
Passband Ripple * 23		PR	-0.0031		0.0031	dB
Stopband * 22		SB	52.5			kHz
Stopband Attenuation * 25, * 26		SA	80.0			dB
Group Delay * 24		GD		6.3		1/fs
Digital Filter + SCF + SMF * 25						
Frequency Response : 0 ~ 40.0kHz			-0.5		0.1	dB

4. Short Delay Slow Roll-Off Filter (DASD bit = "1", DASL bit = "1")

fs=48kHz

Parameter		Symbol	Min.	Typ.	Max.	Unit
SHORT DELAY SLOW ROLL-OFF						
Passband * 28	±0.05dB	PB	0		12.0	kHz
	−3.0dB	PB		21.1		kHz
Passband Ripple * 23		PR	-0.05		0.05	dB
Stopband * 28		SB	41.5			kHz
Stopband Attenuation * 25, * 26		SA	82.0			dB
Group Delay * 24		GD		5.3		1/fs
Digital Filter + SCF + SMF * 25						
Frequency Response : 0 ~ 20.0kHz			-4.8		0.1	dB

fs=96kHz

Parameter		Symbol	Min.	Typ.	Max.	Unit
SHORT DELAY SLOW ROLL-OFF						
Passband * 28	±0.05dB	PB	0		24.2	kHz
	−3.0dB	PB		42.1		kHz
Passband Ripple * 23		PR	-0.05		0.05	dB
Stopband * 28		SB	83.0			kHz
Stopband Attenuation * 25, * 26		SA	82.0			dB
Group Delay * 24		GD		5.3		1/fs
Digital Filter + SCF + SMF * 25						
Frequency Response : 0 ~ 40.0kHz			-5.0		0.1	dB

Note

* 28. The passband and stopband frequencies are proportional to fs (sampling rate).
"PB = 0.252 × fs, SB = 0.864 × fs"

■ SRC Block

(Ta=-40 ~ 85°C; AVDD=3.0~3.6V; LVDD=3.0~3.6V; TVDD=1.7~3.6V; VDD33=3.0~3.6V; VSS1=VSS2=VSS3=VSS4=0V)

1. Audio Mode (SRCFAUDx bit = "1", x=1~4)

Parameter			Symbol	Min.	Typ.	Max.	Unit
Passband	-0.01dB	0.980 ≤ FSO/FSI ≤ 6.000	PB	0		0.4583FSI	kHz
	-0.01dB	0.900 ≤ FSO/FSI < 0.990	PB	0		0.4167FSI	kHz
	-0.01dB	0.533 ≤ FSO/FSI < 0.909	PB	0		0.2182FSI	kHz
	-0.01dB	0.490 ≤ FSO/FSI < 0.539	PB	0		0.2177FSI	kHz
	-0.01dB	0.450 ≤ FSO/FSI < 0.495	PB	0		0.1948FSI	kHz
	-0.01dB	0.225 ≤ FSO/FSI < 0.455	PB	0		0.1312FSI	kHz
	-0.50dB	0.167 ≤ FSO/FSI < 0.227	PB	0		0.0658FSI	kHz
Stopband		0.980 ≤ FSO/FSI ≤ 6.000	SB	0.5417FSI			kHz
		0.900 ≤ FSO/FSI < 0.990	SB	0.5021FSI			kHz
		0.533 ≤ FSO/FSI < 0.909	SB	0.2974FSI			kHz
		0.490 ≤ FSO/FSI < 0.539	SB	0.2812FSI			kHz
		0.450 ≤ FSO/FSI < 0.495	SB	0.2604FSI			kHz
		0.225 ≤ FSO/FSI < 0.455	SB	0.1802FSI			kHz
		0.167 ≤ FSO/FSI < 0.227	SB	0.0970FSI			kHz
Passband Ripple		0.225 ≤ FSO/FSI ≤ 6.000	PR			±0.01	dB
		0.167 ≤ FSO/FSI < 0.227	PR			±0.50	dB
Stopband Attenuation		0.450 ≤ FSO/FSI ≤ 6.000	SA	95.2			dB
		0.167 ≤ FSO/FSI < 0.455	SA	85.0			dB
Group Delay * 29 (Ts=1/fs)			GD		67 (55/FSI+12/FSO)		Ts

Note

* 29. This value is SRC block only. It is the time from a rising edge of input LRCK after data is input to a rising edge of output LRCK just before the data is output when there is no phase difference between input and output LRCK.

2. Voice Mode (SRCFAUDx bit = "0", x =1~4)

Parameter			Symbol	Min.	Typ.	Max.	Unit
Passband	-0.01dB	0.980 ≤ FSO/FSI ≤ 6.000	PB	0		0.4583FSI	kHz
	-0.01dB	0.900 ≤ FSO/FSI < 0.990	PB	0		0.4167FSI	kHz
	-0.50dB	0.711 ≤ FSO/FSI < 0.910	PB	0		0.3420FSI	kHz
	-0.50dB	0.653 ≤ FSO/FSI < 0.718	PB	0		0.3007FSI	kHz
	-0.50dB	0.450 ≤ FSO/FSI < 0.660	PB	0		0.2230FSI	kHz
	-0.50dB	0.327 ≤ FSO/FSI < 0.455	PB	0		0.1417FSI	kHz
	-0.50dB	0.225 ≤ FSO/FSI < 0.330	PB	0		0.1018FSI	kHz
	-0.50dB	0.167 ≤ FSO/FSI < 0.227	PB	0		0.0658FSI	kHz
Stopband		0.980 ≤ FSO/FSI ≤ 6.000	SB	0.5417FSI			kHz
		0.900 ≤ FSO/FSI < 0.990	SB	0.5021FSI			kHz
		0.711 ≤ FSO/FSI < 0.910	SB	0.3735FSI			kHz
		0.653 ≤ FSO/FSI < 0.718	SB	0.3320FSI			kHz
		0.450 ≤ FSO/FSI < 0.660	SB	0.2490FSI			kHz
		0.327 ≤ FSO/FSI < 0.455	SB	0.1660FSI			kHz
		0.225 ≤ FSO/FSI < 0.330	SB	0.1248FSI			kHz
		0.167 ≤ FSO/FSI < 0.227	SB	0.0970FSI			kHz
Passband Ripple		0.900 ≤ FSO/FSI ≤ 6.000	PR			±0.01	dB
		0.167 ≤ FSO/FSI ≤ 0.910	PR			±0.50	dB
Stopband Attenuation		0.900 ≤ FSO/FSI ≤ 6.000	SA	95.2			dB
		0.653 ≤ FSO/FSI < 0.909	SA	90.0			dB
		0.450 ≤ FSO/FSI ≤ 0.660	SA	70.0			dB
		0.167 ≤ FSO/FSI < 0.455	SA	60.0			dB
Group Delay * 29 (Ts=1/fs)			GD		67 (55/FSI+12/FSO)		Ts

10. DC Characteristics

(Ta=-40 ~ 85°C; AVDD=3.0~3.6V; LVDD=3.0~3.6V; TVDD=1.7~3.6V; VDD33=3.0~3.6V; VSS1=VSS2=VSS3=VSS4=0V)

Parameter		Symbol	Min.	Typ.	Max.	Unit
High-Level Input Voltage 1 * 30		VIH1	75%TVDD			V
Low-Level Input Voltage 1 * 30		VIL1			25%TVDD	V
High-Level Input Voltage 2 * 31		VIH2	75%VDD33			V
Low-Level Input Voltage 2 * 31		VIL2			25%VDD33	V
SCL, SDA High-Level Input Voltage		VIH3	70%TVDD			V
SCL, SDA Low-Level Input Voltage		VIL3			30%TVDD	V
High-Level Output Voltage Iout= -100μA * 32		VOH1	TVDD-0.3			V
Low-Level Output Voltage Iout=100μA * 32		VOL1			0.3	V
SDA Low-Level Output Voltage	TVDD ≥ 2.0V (Iout=3mA)	VOL2			0.4	V
	TVDD < 2.0V (Iout=3mA)	VOL2			20%TVDD	V
Input Leak Current * 33		Iin			±10	μA
Input Leak Current, Pulled down pins Power Down * 34, * 36		Iid		66		μA
Input Leak Current, Pulled down pins Power Down Release * 35, * 36		Iid		72		μA
Input Leak Current, TESTI pin		Iid		132		μA
Input Leak Current, XTI pin		Iix		17		μA

Notes

* 30. SDIN1, SDIN2, SDIN3/JX2, LRCK1, BICK1, LRCK2, BICK2, LRCK3/JX0/SDIN4, BICK3/JX1, PDN, SCL/SCLK, CAD/CSN, TESTI and SI pins. The SCL pin is not included.
* 31. XTI pin.
* 32. SDOUT1, DZF/SDOUT2/RDY,STO/SDOUT3/GPO and SDA/SO pins. The SDA pin is not included.
* 33. Except internal pulled-down pins and the XTI pin.
* 34. When the AK7604 is powered down (PDN pin = “L”), the pull down resistors of LRCK1, BICK1, LRCK2, BICK2, LRCK3/JX0/SDIN4 and BICK3/JX1 pins is 50kΩ (Typ. @3.3V).
* 35. When the AK7604 is powered up (PDN pin = “H”), the pull down resistors of LRCK1, BICK1, LRCK2, BICK2, LRCK3/JX0/SDIN4 and BICK3/JX1 pins is 46kΩ (Typ. @3.3V).
* 36. Leak current in case of inputting 3.3V when LVDD=TVDD=VDD33=3.3V.

11. Switching Characateristics

■ System Clock

(Ta=-40 ~ 85°C; AVDD=3.0~3.6V; LVDD=3.0~3.6V; TVDD=1.7~3.6V; VDD33=3.0~3.6V; VSS1=VSS2=VSS3=VSS4=0V; C_L=20pF)

Parameter	Symbol	Min.	Typ.	Max.	Unit
XTI Input Timing					
a) X'tal Oscillator					
Input Frequency	fXTI	11.2896		18.432	MHz
b) XTI Clock Input					
Duty Cycle		40	50	60	%
Input Frequency	fXTI	0.256		24.576	MHz
LRCK/BICK Input Timing (Slave Mode)					
LRCK Input Timing					
Frequency	fs	8		192	kHz
BICK Input Timing					
Frequency * 37	fBCLK	0.256		24.576	MHz
Pulse Width Low	tBCLKL	0.4 / fBCLK			ns
Pulse Width High	tBCLKH	0.4 / fBCLK			ns
LRCK/BICK Output Timing (PLL Master Mode)					
LRCK Output Timing					
Frequency	fs	8		192	kHz
Pulse Width High PCM Mode Except PCM Mode	 tLRCKH tLRCKH		 1/fBCLK 50		 ns %
BICK Output Timing					
Frequency * 37	fBCLK	0.256		24.576	MHz
Duty	dBCLK		50		%

Note

* 37. Required to meet the following expression: fBCLK ≥ 2 x fs x (Input/Output Data Length).

■ Power Down

(Ta=-40 ~ 85°C; AVDD=3.0~3.6V; LVDD=3.0~3.6V; TVDD=1.7~3.6V; VDD33=3.0~3.6V; VSS1=VSS2=VSS3=VSS4=0V)

Parameter	Symbol	Min.	Typ.	Max.	Unit
PDN Pulse Width * 38	tRST	600			ns

Note

* 38. The PDN pin must be "L" when power up the AK7604.

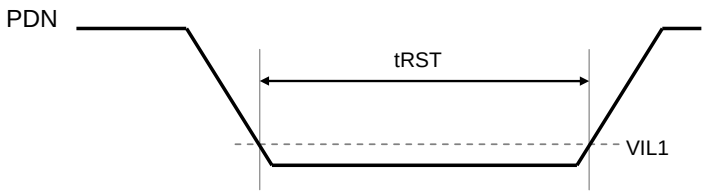


Figure 2. Reset Timing

■ **Serial Data Interface (SDIN1 ~ SDIN4, SDOUT1 ~ SDOUT3)**

(Ta=-40 ~ 85°C; AVDD=3.0~3.6V; LVDD=3.0~3.6V; TVDD=1.7~3.6V; VDD33=3.0~3.6V; VSS1=VSS2=VSS3=VSS4=0V; C_L=20pF)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Slave Mode					
Delay Time from BICK "↑" to LRCK * 39	tBLRD	10			ns
Delay Time from LRCK to BICK "↑" * 39	tLRBD	10			ns
Serial Data Input Latch Setup Time	tBSIDS	10			ns
Serial Data Input Latch Hold Time	tBSIDH	5			ns
Delay Time from BICK "↓" to Serial Data Output * 40	tBSOD1			20	ns
Delay Time from BICK "↑"to Serial Data Output * 39, * 41	tBSOD2	5		30	ns
Master Mode					
BICK Frequency	fBCLK		32, 48, 64, 128, 256		fs
BICK Duty Cycle			50		%
Delay Time from BICK "↓" to LRCK * 40	tMBL	-10		10	ns
Serial Data Input Latch Setup Time	tBSIDS	10			ns
Serial Data Input Latch Hold Time	tBSIDH	10			ns
Delay Time from BICK "↓" to Serial Data Output * 40, * 41	tBSOD			10	ns

Notes

* 39. It is measured from BICK "↓" when the BICK polarity is inverted by setting BCKPx bit = "1".
* 40. It is measured from BICK "↑" when the BICK polarity is inverted by setting BCKPx bit = "1".
* 41. Set SDOPHx bit to "1" and the data from SDOUTx pin is output based on BICK "↑" when BICK speed is more than 12.288MHz such as when using TDM256 mode with 96kHz sampling frequency or TDM128 mode with 192kHz sampling frequency in slave mode. SDOPHx bit must be set to "0" in master mode.

1. Slave Mode

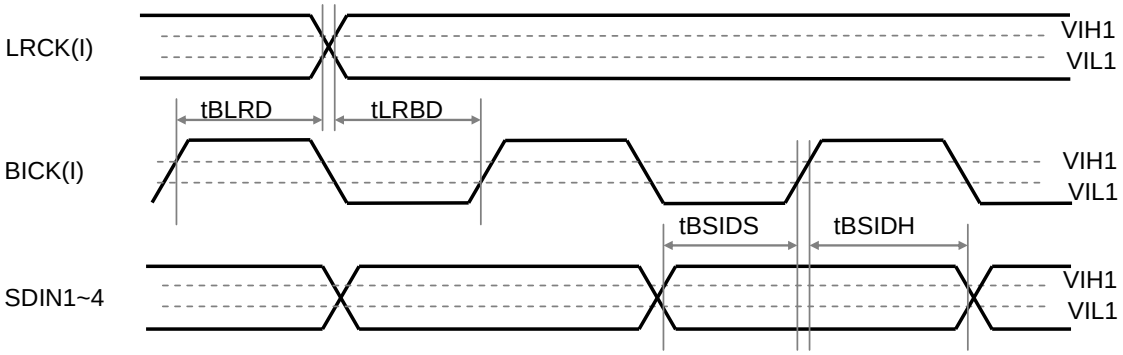


Figure 3. Serial Interface Input Timing in Slave Mode

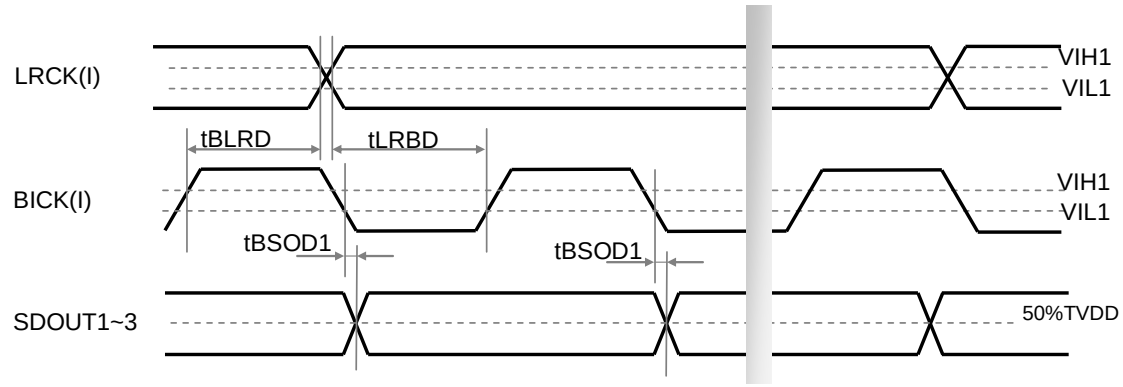


Figure 4. Serial Interface Output Timing in Slave Mode (SDOPHx bit = “0”)

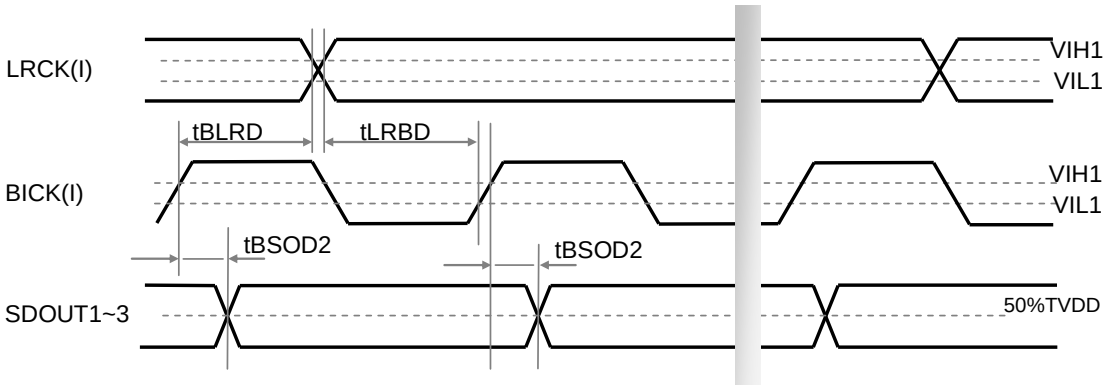


Figure 5. Serial Interface Output Timing in Slave Mode (SDOPHx bit = “1”)

2. Master Mode

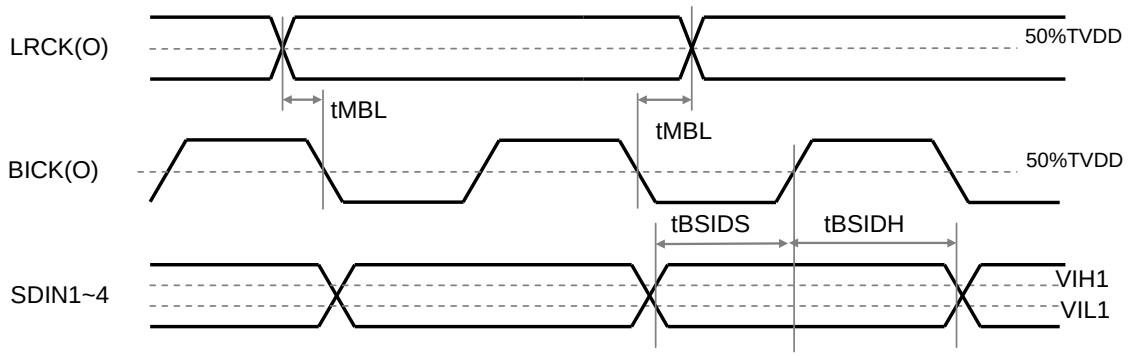


Figure 6. Serial Interface Input Timing in Master Mode

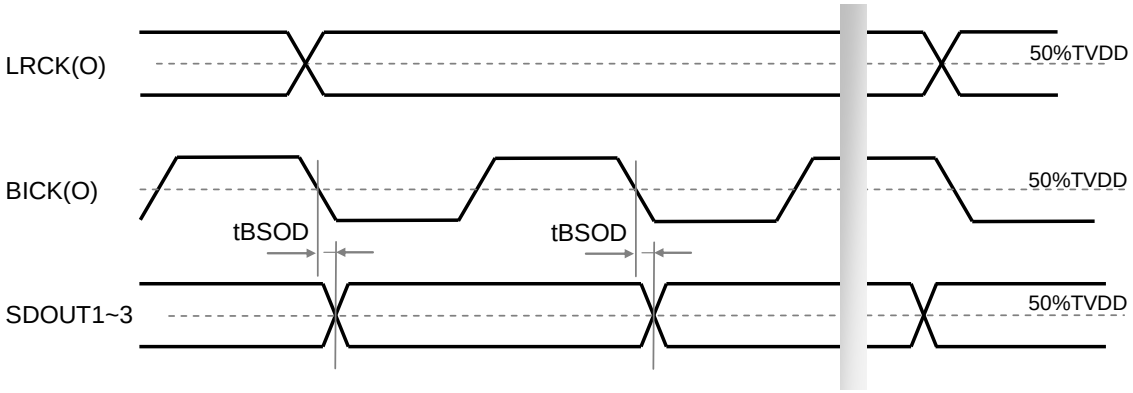


Figure 7. Serial Interface Output Timing in Master Mode (SDOPHx bit = “0”)

■ SPI Interface

(Ta=-40 ~ 85°C; AVDD=3.0~3.6V; LVDD=3.0~3.6V; TVDD=1.7~3.6V; VDD33=3.0~3.6V; VSS1=VSS2=VSS3=VSS4=0V; C_L=20pF)

1. SPI Low Speed Mode

Parameter	Symbol	Min.	Typ.	Max.	Unit
µP Interface Signal					
SCLK Frequency * 43	fSCLK			3.0	MHz
SCLK Low-level Width	tSCLKL	160			ns
SCLK High-level Width	tSCLKH	160			ns
Microcontroller → AK7604					
CSN High-level Width	tWRQH	300			ns
From CSN "↑" to PDN "↑"	tRST	360			ns
From PDN "↑" to CSN "↓"	tIRRQ	1			ms
From CSN "↓" to SCLK "↓"	tWSC	300			ns
From SCLK "↑" to CSN "↑"	tSCW	480			ns
SI Latch Setup Time	tSIS	120			ns
SI Latch Hold Time	tSIH	120			ns
AK7604 → Microcontroller					
Delay Time from SCLK "↓" to SO Output	tSOS			120	ns
SO Output Hold Time from SCLK "↑" * 42	tSOH	120			ns

2. SPI High Speed Mode

Parameter	Symbol	Min.	Typ.	Max.	Unit
µP Interface Signal					
SCLK Frequency * 43	fSCLK			6	MHz
SCLK Low-level Width	tSCLKL	72			ns
SCLK High-level Width	tSCLKH	72			ns
Microcontroller → AK7604					
CSN High-level Width	tWRQH	150			ns
From CSN "↑" to PDN "↑"	tRST	180			ns
From PDN "↑" to CSN "↓"	tIRRQ	1			ms
From CSN "↓" to SCLK "↓"	tWSC	150			ns
From SCLK "↑" to CSN "↑"	tSCW	240			ns
SI Latch Setup Time	tSIS	60			ns
SI Latch Hold Time	tSIH	60			ns
AK7604 → Microcontroller					
Delay Time from SCLK "↓" to SO Output	tSOS			60	ns
SO Output Hold Time from SCLK "↑" * 42	tSOH	60			ns

Notes

* 42. Except when writing the 24th bit (8 bits command + 16 bits address) of the command code. This will be the 8th bit (8 bits command) with "write preparation data read command (24H)".

* 43. Dummy command writing for switching to SPI interface from I^2C interface and control register access can always be made in SPI high speed mode (Max. 6MHz). DSP RAM area can be accessed in SPI low speed mode (Max. 3MHz) in clock reset state (CKRESETN bit = "0") and can also be accessed in SPI high speed mode (Max. 6MHz) when PLL is locked (CKRESETN bit = "1" and PLL is locked). It is necessary to set DLRDY bit to "1" when accessing to the DSP RAM area while PLL is unlocked.

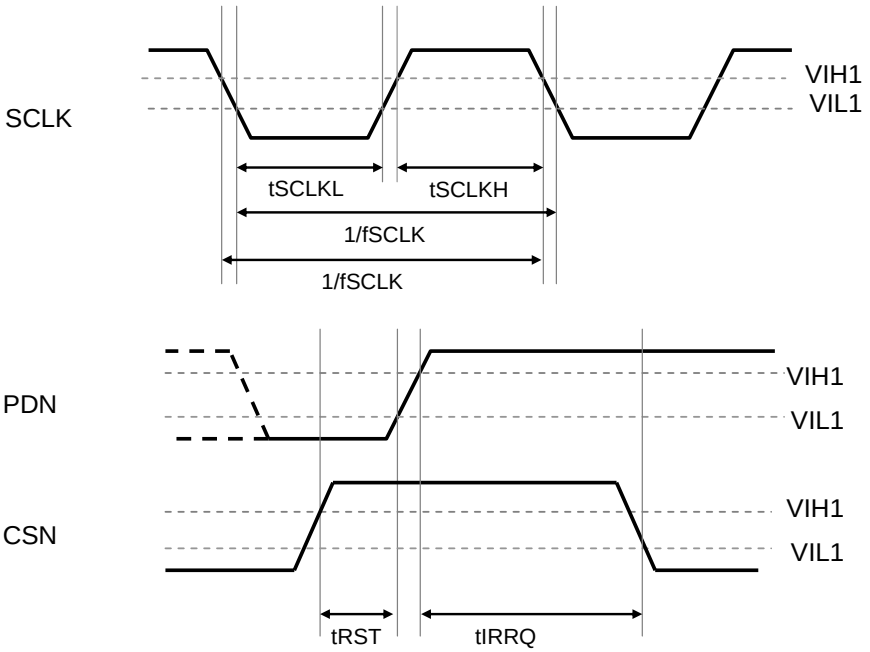


Figure 8. SPI Interface Timing 1

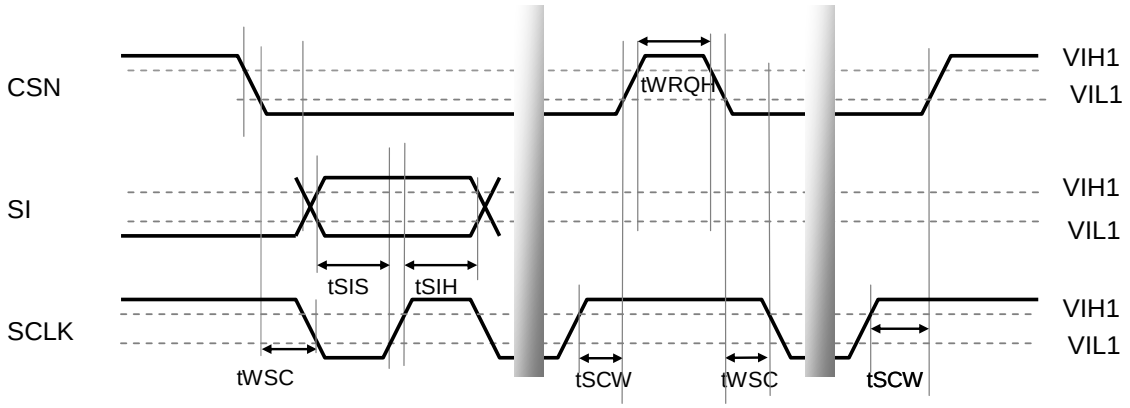


Figure 9. SPI Interface Timing 2 (Microcontroller → AK7604)

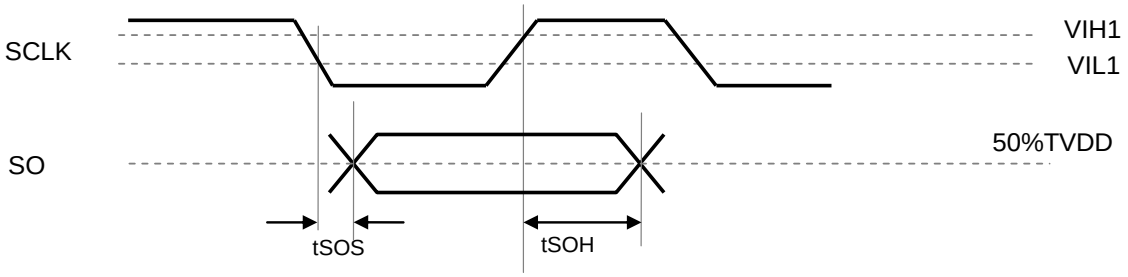


Figure 10. SPI Interface Timing 3 (AK7604 → Microcontroller)

■ I²C Interface

(Ta=-40 ~ 85°C; AVDD=3.0~3.6V; LVDD=3.0~3.6V; TVDD=1.7~3.6V; VDD33=3.0~3.6V; VSS1=VSS2=VSS3=VSS4=0V)

I²C: Fast Mode

Parameter	Symbol	Min.	Typ.	Max.	Unit
I²C Timing					
SCL clock frequency	fSCL	-	-	400	kHz
Bus Free Time Between Transmissions	tBUF	1.3	-	-	μs
Start Condition Hold Time (prior to first Clock pulse)	tHD:STA	0.6	-	-	μs
Clock Low Time	tLOW	1.3	-	-	μs
Clock High Time	tHIGH	0.6	-	-	μs
Setup Time for Repeated Start Condition	tSU:STA	0.6	-	-	μs
SDA Hold Time from SCL Falling	tHD:DAT	0	-	-	μs
SDA Setup Time from SCL Rising	tSU:DAT	0.1	-	-	μs
Rise Time of Both SDA and SCL Lines	tR	-	-	0.3	μs
Fall Time of Both SDA and SCL Lines	tF	-	-	0.3	μs
Setup Time for Stop Condition	tSU:STO	0.6	-	-	μs
Pulse Width of Spike Noise Suppressed By Input Filter	tSP	0	-	50	ns
Capacitive load on bus	Cb	-	-	400	pF

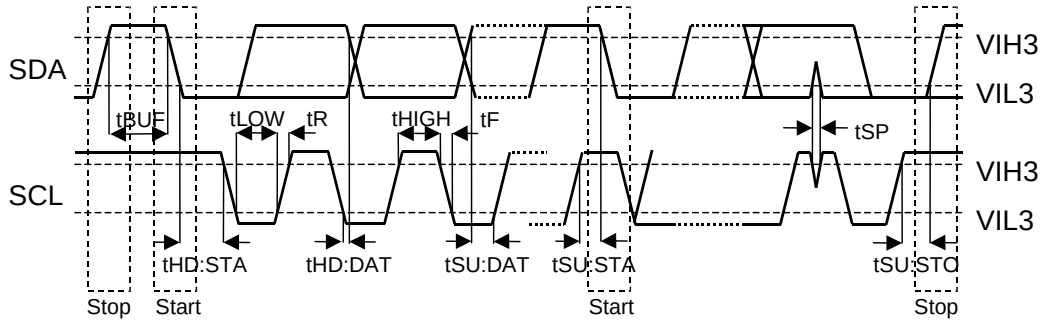


Figure 11. I²C Interface Timing

12. Recommended External Circuits

■ Connection Diagram

I²C Interface

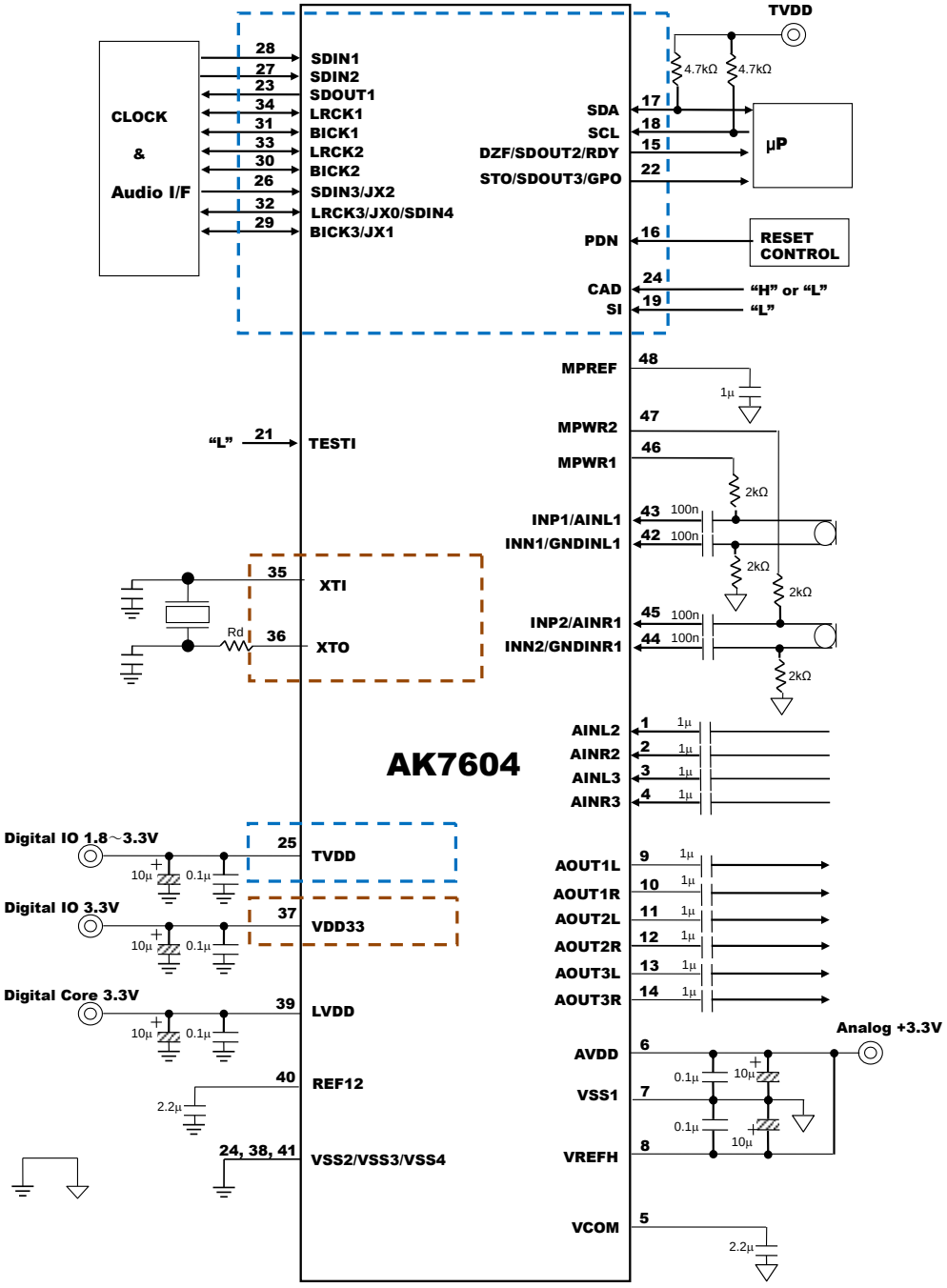


Figure 12. I²C Interface Connection Example

■ Peripheral Circuit

1. Ground

VSS1, VSS2, VSS3 and VSS4 should be connected to the same ground. Decoupling capacitors, particularly ceramic capacitors of small capacity, should be placed at positions as close as possible to the AK7604.

2. Reference Voltage

VCOM is a common voltage of this chip and the VCOM pin outputs AVDD/2. A 2.2μF ceramic capacitor should be connected between the VCOM pin and VSS1.

Do not connect the VCOM pin to any external devices. Digital signal lines, especially clock signal line should be kept away as far as possible from this pin in order to avoid unwanted coupling into the AK7604.

3. Analog Input

The analog input signal is input to the analog modulator of the AK7604. The maximum input voltage at differential input pins is ±2.83Vpp (Typ.). The maximum input voltage at single-ended input pins is 2.83Vpp (Typ.). The output code format is 2's complements. The internal HPF removes the DC offset.

After power-down is released, the internal operating point level AVDD/2 occurs on analog input pins of the AK7604. Concerning the internal operating point formation circuit, each input pin has impedance of 25kΩ (Typ.). The pins that are connected to AC coupling capacitors require start-up time (time constant).

The AK7604 samples the analog inputs at 6.144MHz when fs=48kHz, 96kHz. The AK7604 includes an anti-aliasing filter (RC filter), and no external low-pass filter is necessary in front of the ADC. However, an external low-pass filter should be connected before the ADC for the signal which has large out-of-band noise such as D/A converted signals.

The analog power supply to the AK7604 is +3.3V (Typ.). Voltage of AVDD + 0.3V or larger, voltage of AVSS - 0.3V or smaller, and current of 10mA or larger must not be applied to analog input pins. Excessive current will damage the internal protection circuit and will cause latch-up, damaging the IC. Accordingly, if the external analog circuit voltage is ±15V, the analog input pins must be protected from signals which are equal or larger than absolute maximum ratings.

When using differential input mode, it is prohibited to input signal to only one side like pseudo differential input.

4. Analog Output

The analog output is single-ended and the output signal range is typically 0.86 x AVDD Vpp centered on VCOM. The digital input data format is two’s compliment. Positive full-scale output corresponds to 7FFFFFH (@24bit) input code, Negative full scale is 800000H (@24bit) and VCOM voltage ideally is 000000H (@24bit). The Out-of-Band noise (shaping noise) generated by the internal delta-sigma modulator is attenuated by an integrated switched capacitor filter (SCF) and a continuous time filter (CTF).

5. Crystal Oscillator

The resistor and capacitor values for the oscillator RC circuit are shown blow.

Table 4. Recommended Resistance and Capacitance with Crystal Oscillator

Oscillator	R1 (Max)	C0 (Max)	XTI, XTO pin Capacity
12.288MHz	120Ω	2.5pF	22pF
18.432MHz	80Ω	2.5pF	15pF

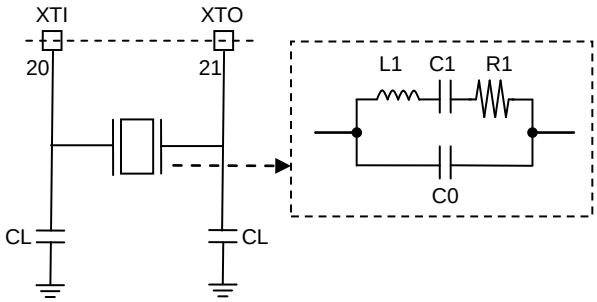
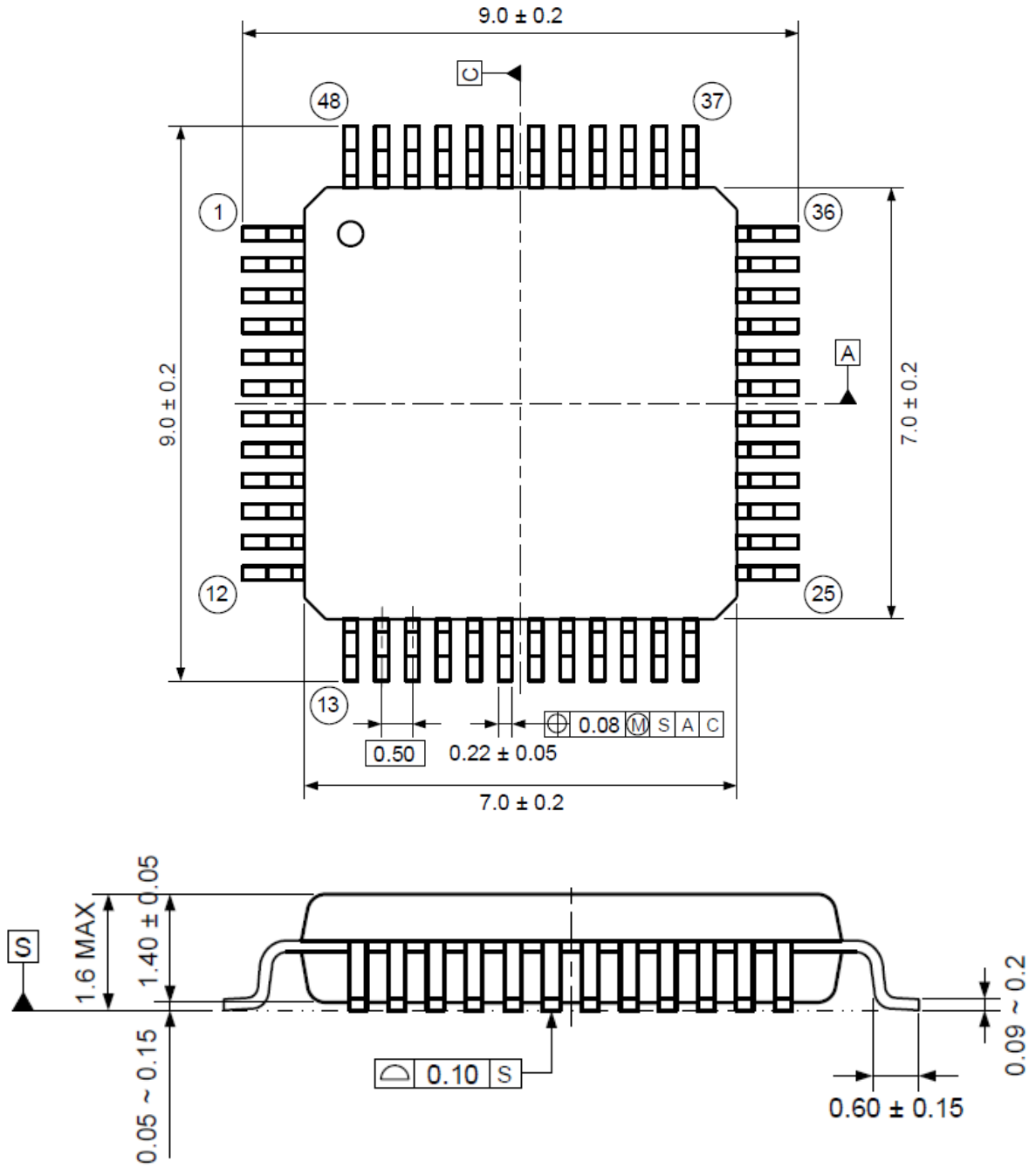


Figure 13. Electric Equivalent Circuit of Crystal Oscillator

13. Package

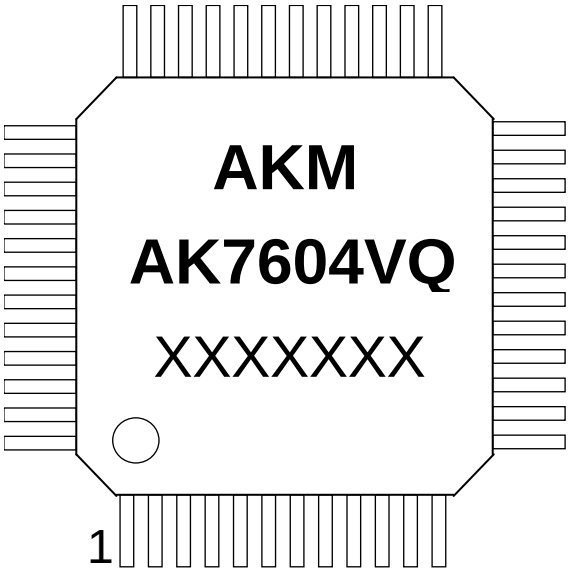
■ Outline Dimensions



■ Material and Lead Finish

Package: Epoxy, Halogen (Br and Cl) free
Lead frame: Copper
Lead-finish: Soldering (Pb free) plate

■ **Marking**



1) Pin #1 indication
2) Date Code: XXXXXXX (7 digits)
3) Marking Code: AK7604VQ
4) Asahi Kasei Logo

14. Ordering Guide

AK7604VQ	-40 ~ +85°C	48-pin LQFP (0.5mm pitch)
AKD7604	Evaluation Board for AK7604	

15. Revision History

Date (Y/M/D)	Revision	Reason	Page	Contents
2018/09/27	0	First Edtion		

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