DATA SHEET
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Motion SPM® 45 Series

FNB41060

General Description

FNB41060 is a Motion SPM45 module providing a fully−featured, high−performance inverter output stage for AC Induction, BLDC, and PMSM motors. These modules integrate optimized gate drive of the built−in IGBTs to minimize EMI and losses, while also providing multiple on−module protection features including under−voltage lockouts, over−current shutdown, thermal monitoring, and fault reporting. The built−in, high−speed HVIC requires only a single supply voltage and translates the incoming logic−level gate inputs to the high−voltage, high−current drive signals required to properly drive the module's robust short−circuit−rated IGBTs. Separate negative IGBT terminals are available for each phase to support the widest variety of control algorithms.

Features

- UL Certified No. E209204 (UL1557)
- 600 V − 10 A 3−Phase IGBT Inverter with Integral Gate Drivers and Protection
- Low Thermal Resistance Using Ceramic Substrate
- Low−Loss, Short−Circuit Rated IGBTs
- Built−In Bootstrap Diodes and Dedicated Vs Pins Simplify PCB Layout
- Built−In NTC Thermistor for Temperature Monitoring
- Separate Open−Emitter Pins from Low−Side IGBTs for Three−Phase Current Sensing
- Single−Grounded Power Supply
- Isolation Rating: 2000 V_{rms} / Min.
- This Device is Pb−Free and Halide Free

Applications

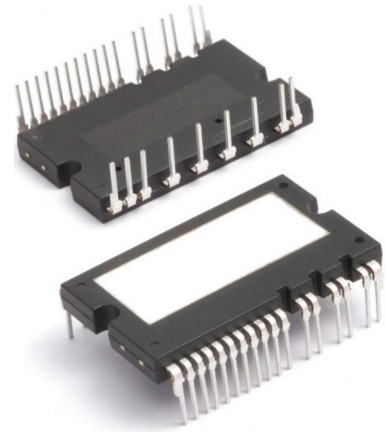
- Motion Control − Home Appliance / Industrial Motor

Integrated Power Functions

- 600 V − 10 A IGBT Inverter for Three−phase DC / AC Power Conversion (Please Refer to Figure 2)

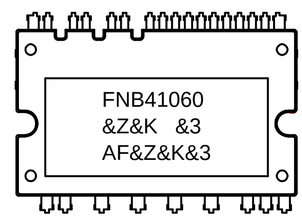
Integrated Drive, Protection, and System Control Functions

- For Inverter High−side IGBTs: Gate Drive Circuit, High−voltage Isolated High−speed Level Shifting Control Circuit Under−Voltage Lock−Out (UVLO) Protection
- For Inverter Low−side IGBTs: Gate Drive Circuit, Short−Circuit Protection (SCP) Control Supply Circuit Under−Voltage Lock−Out (UVLO) Protection
- Fault Signaling: Corresponding to UVLO (Low−side Supply) and SC Faults
- Input Interface: Active−HIGH Interface, Works with 3.3 / 5 V Logic, Schmitt Trigger Input



SPMAA−A26 / 26LD, PDD STD, CERAMIC TYPE, STANDARD DUAL FORM CASE MODFA

MARKING DIAGRAM



FNB41060 = Specific Device Code
&Z = Assembly Plant Code
&K = 2−Digits Lot Run Traceability Code
&3 = 3−Digit Date Code
AF = Specific Product Name

ORDERING INFORMATION

Device	Package	Shipping
FNB41060	SPMAA−A26 (Pb−Free, Halide Free)	12 Units / Rail

Related Resources

- AN−9070 − Motion SPM 45 Series Users Guide
- AN−9071 − Motion SPM 45 Series Thermal Performance Information
- AN−9072 − Motion SPM 45 Series Mounting Guidance
- RD−344 − Reference Design (Three Shunt Solution)
- RD−345 − Reference Design (One Shunt Solution)

PIN CONFIGURATION

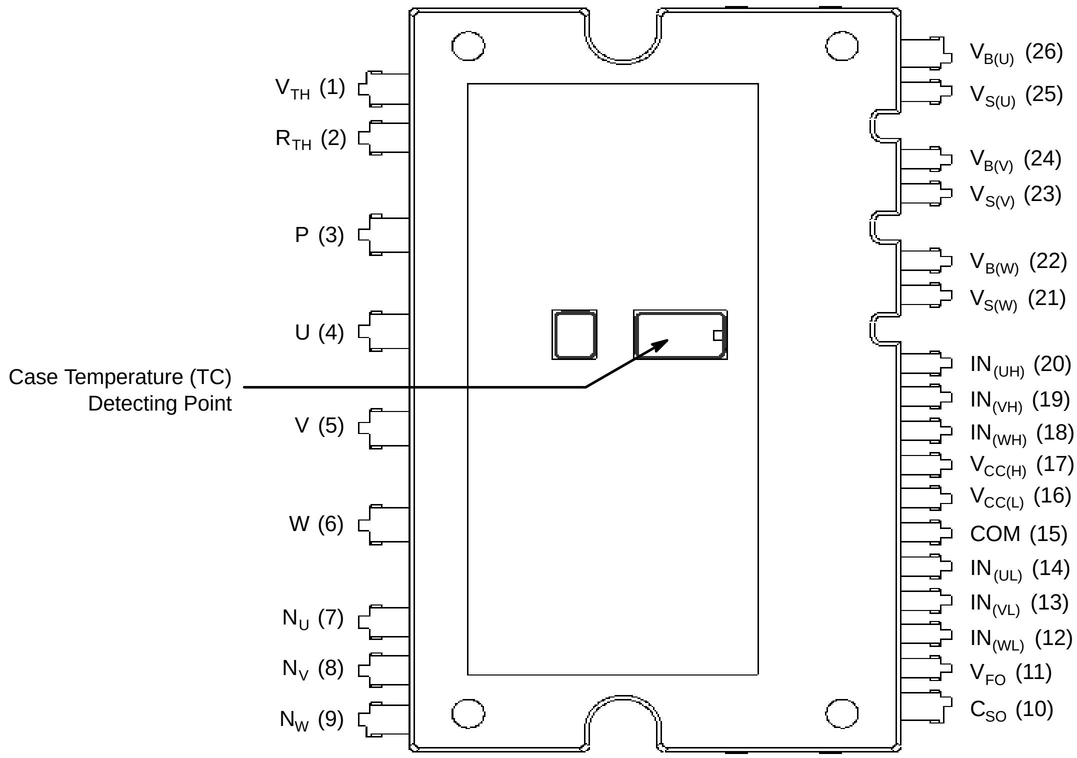


Figure 1. Top View

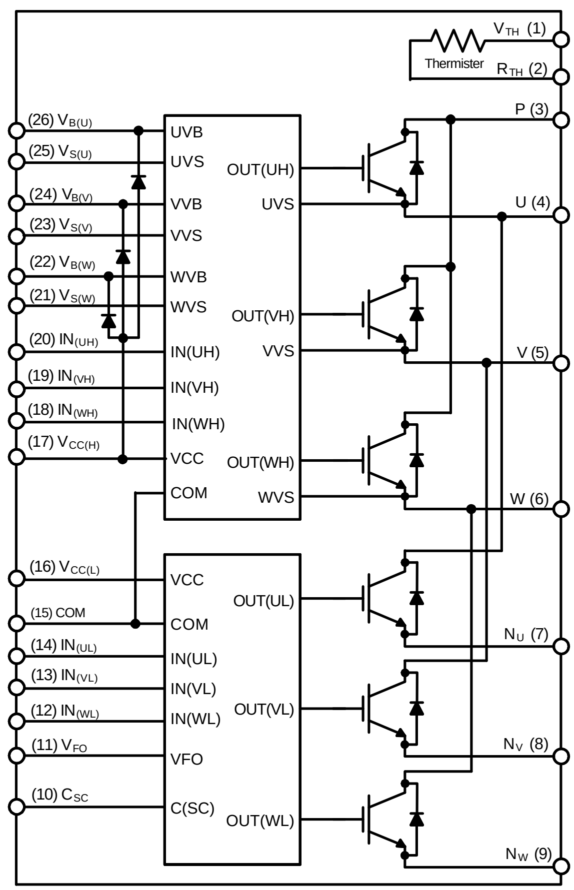
PIN DESCRIPTIONS

Pin Number	Pin Name	Pin Description
1	V_{TH}	Thermistor Bias Voltage
2	R_{TH}	Series Resistor for the Use of Thermistor (Temperature Detection)
3	P	Positive DC−Link Input
4	U	Output for U−Phase
5	V	Output for V−Phase
6	W	Output for W−Phase
7	N_U	Negative DC−Link Input for U−Phase
8	N_V	Negative DC−Link Input for V−Phase
9	N_W	Negative DC−Link Input for W−Phase
10	C_{SC}	Capacitor (Low−Pass Filter) for Short−circuit Current Detection Input
11	V_{FO}	Fault Output
12	$IN_{(WL)}$	Signal Input for Low−Side W−Phase
13	$IN_{(VL)}$	Signal Input for Low−Side V−Phase
14	$IN_{(UL)}$	Signal Input for Low−Side U−Phase
15	COM	Common Supply Ground
16	$V_{CC(L)}$	Low−Side Common Bias Voltage for IC and IGBTs Driving
17	$V_{CC(H)}$	High−Side Common Bias Voltage for IC and IGBTs Driving
18	$IN_{(WH)}$	Signal Input for High−Side W−Phase

PIN DESCRIPTIONS (continued)

Pin Number	Pin Name	Pin Description
19	$IN_{(VH)}$	Signal Input for High−Side V−Phase
20	$IN_{(UH)}$	Signal Input for High−Side U−Phase
21	$V_{S(W)}$	High−Side Bias Voltage Ground for W−Phase IGBT Driving
22	$V_{B(W)}$	High−Side Bias Voltage for W−Phase IGBT Driving
23	$V_{S(V)}$	High−Side Bias Voltage Ground for V−Phase IGBT Driving
24	$V_{B(V)}$	High−Side Bias Voltage for V−Phase IGBT Driving
25	$V_{S(U)}$	High−Side Bias Voltage Ground for U−Phase IGBT Driving
26	$V_{B(U)}$	High−Side Bias Voltage for U−Phase IGBT Driving

INTERNAL EQUIVALENT CIRCUIT AND INPUT/OUTPUT PINS



NOTE:
1. Inverter high−side is composed of three IGBTs, freewheeling diodes, and one control IC for each IGBT.
2. Inverter low−side is composed of three IGBTs, freewheeling diodes, and one control IC for each IGBT. It has gate drive and protection functions.
3. Inverter power side is composed of four inverter DC−link input terminals and three inverter output terminals.

Figure 2. Internal Block Diagram

ABSOLUTE MAXIMUM RATINGS (T_J = 25°C unless otherwise specified)

Symbol	Parameter	Conditions	Rating	Unit
INVERTER PART				
V_{PN}	Supply Voltage	Applied between P − N_U, N_V, N_W	450	V
$V_{PN(Surge)}$	Supply Voltage (Surge)	Applied between P − N_U, N_V, N_W	500	V
V_{CES}	Collector−Emitter Voltage		600	V
$I_{O,25}$	Output Phase Current	T_C = 25°C, T_J < 150°C (Note 4)	10	A
$I_{O,100}$	Output Phase Current	T_C = 100°C, T_J < 150°C (Note 4)	5	A
I_{pk}	Output Peak Phase Current	T_C = 25°C, T_J < 150°C, Under 1 ms Pulse Width	15	A
P_C	Collector Dissipation	T_C = 25°C per Chip	32	W
T_J	Operating Junction Temperature	(Note 5)	− 40~150	°C
CONTROL PART				
V_{CC}	Control Supply Voltage	Applied between $V_{CC(H)}$, $V_{CC(L)}$ − COM	20	V
V_{BS}	High−Side Control Bias Voltage	Applied between $V_{B(U)}$ − $V_{S(U)}$, $V_{B(V)}$ − $V_{S(V)}$, $V_{B(W)}$ − $V_{S(W)}$	20	V
V_{IN}	Input Signal Voltage	Applied between $IN_{(UH)}$, $IN_{(VH)}$, $IN_{(WH)}$, $IN_{(UL)}$, $IN_{(VL)}$, $IN_{(WL)}$ − COM	−0.3~V_{CC} + 0.3	V
V_{FO}	Fault Output Supply Voltage	Applied between V_{FO} − COM	−0.3~V_{CC} + 0.3	V
I_{FO}	Fault Output Current	Sink Current at V_{FO} pin	1	mA
V_{SC}	Current−Sensing Input Voltage	Applied between C_{SC} − COM	−0.3~V_{CC} + 0.3	V
BOOTSTRAP DIODE PART				
V_{RRM}	Maximum Repetitive Reverse Voltage		600	V
I_F	Forward Current	T_C = 25°C, T_J < 150°C	0.50	A
I_{FP}	Forward Current (Peak)	T_C = 25°C, T_J < 150°C, Under 1 ms Pulse Width	1.50	A
T_J	Operating Junction Temperature		−40~150	°C
TOTAL SYSTEM				
$V_{PN(PROT)}$	Self−Protection Supply Voltage Limit (Short−Circuit Protection Capability)	V_{CC} = V_{BS} = 13.5~16.5 V T_J = 150°C, Non−Repetitive, < 2 μs	400	V
T_{STG}	Storage Temperature		−40~125	°C
V_{ISO}	Isolation Voltage	60 Hz, Sinusoidal, AC 1 Minute, Connect Pins to Heat Sink Plate	2000	V_{rms}

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

4. Sinusoidal PWM at V_{PN} = 300 V, V_{CC} = V_{BS} = 15 V, T_J < 150°C, F_{SW} = 20 kHz, MI = 0.9, PF = 0.8.
5. The maximum junction temperature rating of the power chips integrated within the Motion SPM 45 product is 150°C.

THERMAL RESISTANCE

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-c)Q}$	Junction to Case Thermal Resistance	Inverter IGBT part, (Per 1 / 6 Module)	−	−	3.8	°C/W
$R_{th(j-c)F}$		Inverter FWDi part, (Per 1 / 6 Module)	−	−	4.8	°C/W

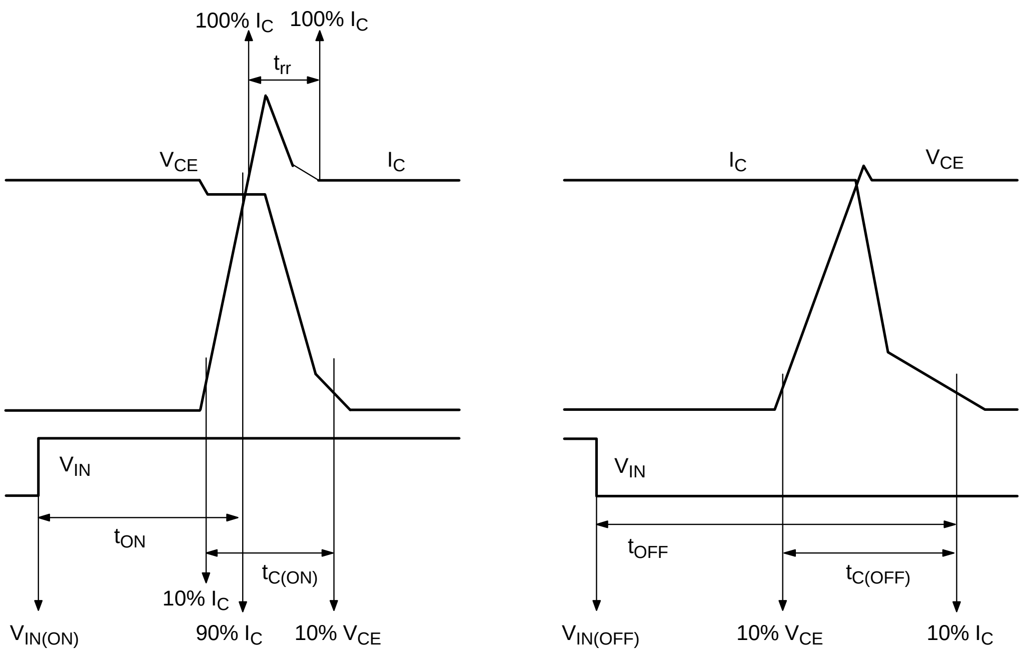
6. For the measurement point of case temperature (T_C), please refer to Figure 1.

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise specified)

Symbol		Parameter	Conditions		Min	Typ	Max	Unit
INVERTER PART								
$V_{CE(SAT)}$		Collector−Emitter Saturation Voltage	V_{CC} = V_{BS} = 15 V V_{IN} = 5 V	I_C = 5 A, T_J = 25°C	−	1.5	2.0	V
V_F		FWDi Forward Voltage	V_{IN} = 0 V	I_F = 5 A, T_J = 25°C	−	1.5	2.0	V
HS	t_{ON}	Switching Times	V_{PN} = 300 V, V_{CC} = V_{BS} = 15 V, I_C = 5 A, T_J = 25°C V_{IN} = 0 V ↔ 5 V, Inductive Load (Note 7)		0.45	0.75	1.25	μs
	$t_{C(ON)}$				−	0.20	0.45	μs
	t_{OFF}				−	0.70	1.20	μs
	$t_{C(OFF)}$				−	0.15	0.40	μs
	t_{rr}				−	0.15	−	μs
LS	t_{ON}		V_{PN} = 300 V, V_{CC} = V_{BS} = 15 V, I_C = 5 A, T_J = 25°C V_{IN} = 0 V ↔ 5 V, Inductive Load (Note 7)		0.35	0.65	1.15	μs
	$t_{C(ON)}$				−	0.15	0.40	μs
	t_{OFF}				−	0.65	1.15	μs
	$t_{C(OFF)}$				−	0.15	0.40	μs
	t_{rr}				−	0.15	−	μs
I_{CES}		Collector − Emitter Leakage Current	V_{CE} = V_{CES}		−	−	1	mA

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

7. t_{ON} and t_{OFF} include the propagation delay time of the internal drive IC. $t_{C(ON)}$ and $t_{C(OFF)}$ are the switching times of IGBT itself under the given gate driving condition internally. For the detailed information, please see Figure 3.



(a) turn−on *(b) turn−off*

Figure 3. Switching Time Definition

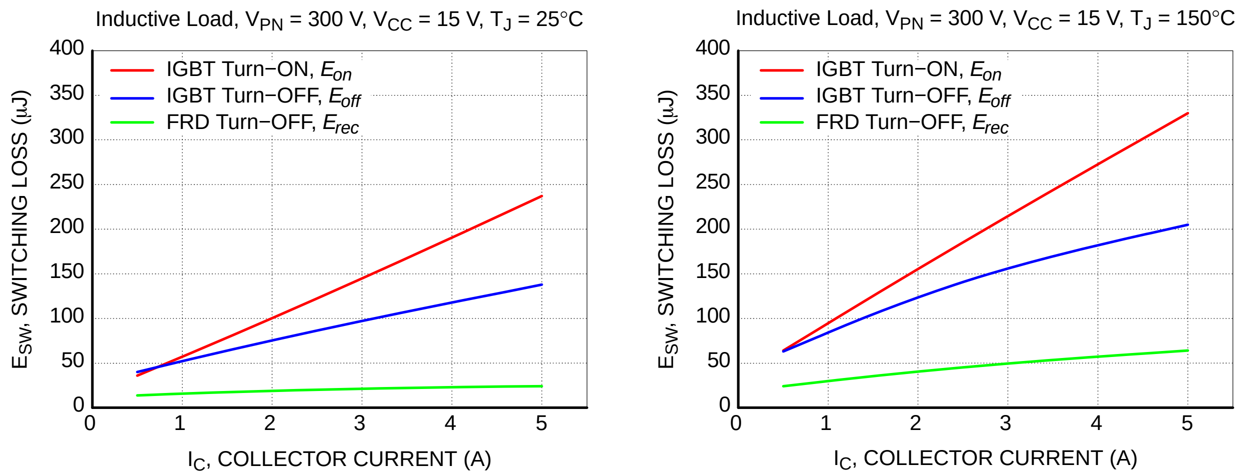


Figure 4. Switching Loss Characteristics (Typical)

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise specified)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
CONTROL PART							
I_{QCCH}	Quiescent V_{CC} Supply Current	$V_{CC(H)}$ = 15 V, $IN_{(UH,VH,WH)}$ = 0 V	$V_{CC(H)}$ − COM	−	−	0.10	mA
I_{QCCL}		$V_{CC(L)}$ = 15 V, $IN_{(UL,VL,\ WL)}$ = 0 V	$V_{CC(L)}$ − COM	−	−	2.65	mA
I_{PCCH}	Operating V_{CC} Supply Current	$V_{CC(L)}$ = 15 V, f_{PWM} = 20 kHz, Duty = 50%, Applied to One PWM Signal Input for High−Side	$V_{CC(H)}$ − COM	−	−	0.15	mA
I_{PCCL}		$V_{CC(L)}$ = 15 V, f_{PWM} = 20 kHz, Duty = 50%, Applied to One PWM Signal Input for Low−Side	$V_{CC(L)}$ − COM	−	−	3.65	mA
I_{QBS}	Quiescent V_{BS} Supply Current	V_{BS} = 15 V, $IN_{(UH,\ VH,\ WH)}$ = 0 V	$V_{B(U)}$ − $V_{S(U)}$, $V_{B(V)}$ − $V_{S(V)}$, $V_{B(W)}$ − $V_{S(W)}$	−	−	0.30	mA
I_{PBS}	Operating V_{BS} Supply Current	V_{CC} = V_{BS} = 15 V, f_{PWM} = 20 kHz, Duty = 50%, Applied to One PWM Signal Input for High−Side	$V_{B(U)}$ − $V_{S(U)}$, $V_{B(V)}$ − $V_{S(V)}$, $V_{B(W)}$ − $V_{S(W)}$	−	−	2.00	mA
V_{FOH}	Fault Output Voltage	V_{SC} = 0 V, V_{FO} Circuit: 10 kΩ to 5 V Pull−up		4.5	−	−	V
V_{FOL}		V_{SC} = 1 V, V_{FO} Circuit: 10 kΩ to 5 V Pull−up		−	−	0.5	V
$V_{SC(ref)}$	Short−Circuit Current Trip Level	V_{CC} = 15 V (Note 8)		0.45	0.50	0.55	V
UV_{CCD}	Supply Circuit Under−Voltage Protection	Detection level		10.5	−	13.0	V
UV_{CCR}		Reset level		11.0	−	13.5	V
UV_{BSD}		Detection level		10.0	−	12.5	V
UV_{BSR}		Reset level		10.5	−	13.0	V
t_{FOD}	Fault−Out Pulse Width			30	−	−	μs
$V_{IN(ON)}$	ON Threshold Voltage	Applied between $IN_{(UH)}$, $IN_{(VH)}$, $IN_{(WH)}$, $IN_{(UL)}$, $IN_{(VL)}$, $IN_{(WL)}$ − COM		−	−	2.6	V
$V_{IN(OFF)}$	OFF Threshold Voltage			0.8	−	−	V
R_{TH}	Resistance of Thermister	@ T_{TH} = 25°C, (Note 9)		−	47	−	kΩ
		@ T_{TH} = 100°C		−	2.9	−	kΩ

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

8. Short−circuit protection is functioning only at the low−sides.
9. T_{TH} is the temperature of thermister itselt. To know case temperature (T_C), please make the experiment considering your application.

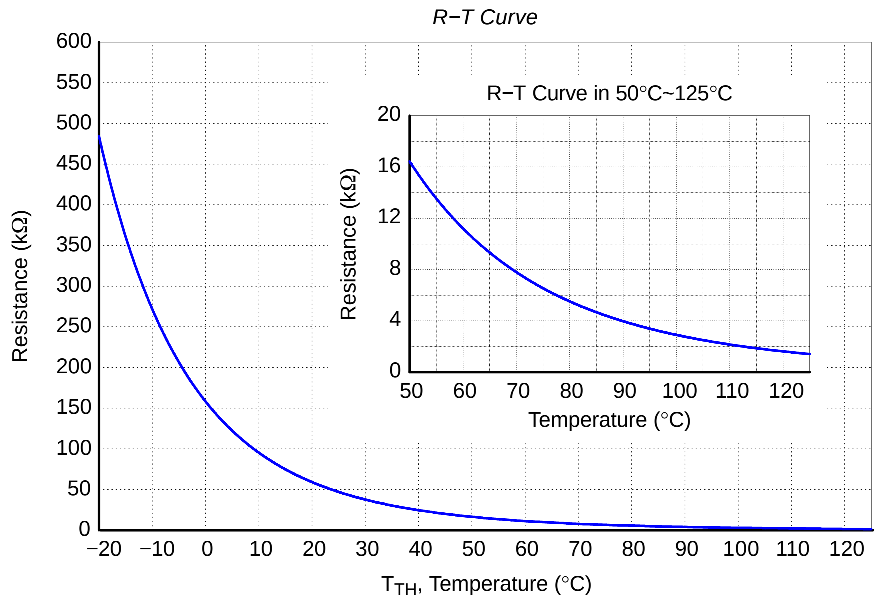
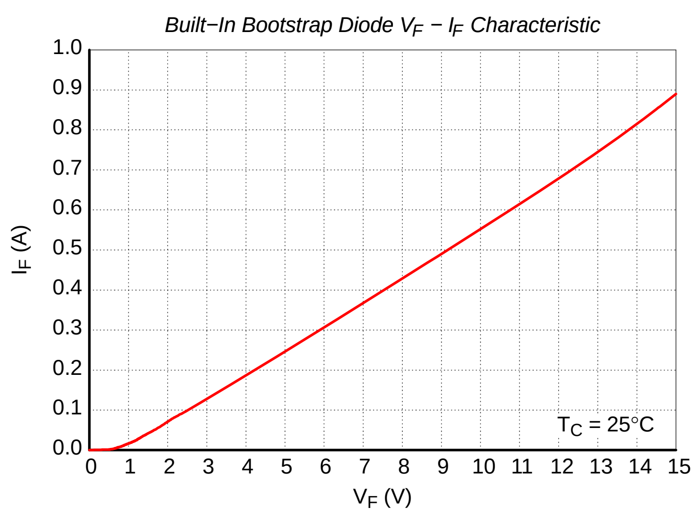


Figure 5. R−T Curve of The Built−In Thermistor

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise specified)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
BOOTSTRAP DIODE PART						
V_F	Forward Voltage	I_F = 0.1 A, T_C = 25°C	−	2.5	−	V
trr	Reverse−Recovery Time	I_F = 0.1 A, T_C = 25°C	−	80	−	ns

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.



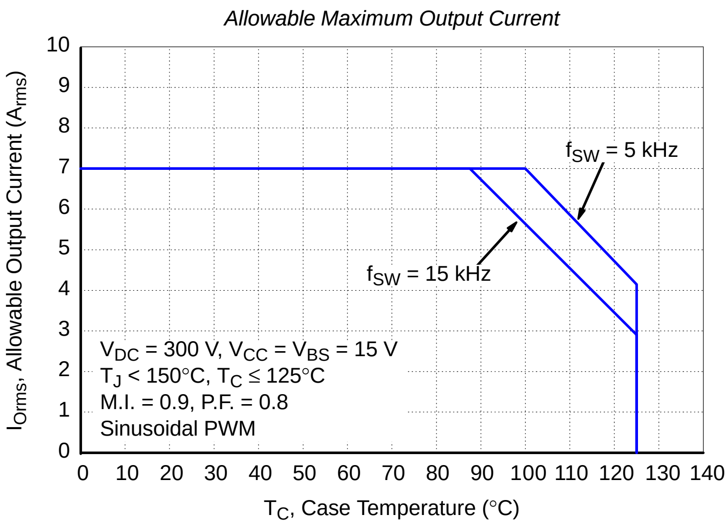
NOTE:
10. Build−in bootstrap diode includes around 15 Ω resistance characteristic.

Figure 6. R−T Curve of The Built−In Thermistor

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{PN}	Supply Voltage	Applied between P − N_U, N_V, N_W	−	300	400	V
V_{CC}	Control Supply Voltage	Applied between $V_{CC(H)}$, $V_{CC(L)}$ − COM	13.5	15	16.5	V
V_{BS}	High−Side Bias Voltage	Applied between $V_{B(U)} - V_{S(U)}$, $V_{B(V)} - V_{S(V)}$, $V_{B(W)} - V_{S(W)}$	13.0	15	18.5	V
dV_{CC} / dt, dV_{BS} / dt	Control Supply Variation		−1	−	1	V / μs
t_{dead}	Blanking Time for Preventing Arm−Short	For each input signal	1.5	−	−	μs
f_{PWM}	PWM Input Signal	−40°C < T_J < 150°C	−	−	20	kHz
V_{SEN}	Voltage for Current Sensing	Applied between N_U, N_V, N_W − COM (Including Surge−Voltage)	−4	−	4	V
$P_{WIN(ON)}$	Minimum Input Pulse Width	(Note 11)	0.5	−	−	μs
$P_{WIN(OFF)}$			0.5	−	−	

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.
11. This product might not make response if input pulse width is less than the recommended value.



NOTE:
12. This allowable output current value is the reference data for the safe operation of this product. This may be different from the actual application and operating condition.

Figure 7. Allowable Maximum Output Current

MECHANICAL CHARACTERISTICS AND RATINGS

Parameter	Conditions		Min	Typ	Max	Unit
Device Flatness	See Figure 8		0	−	+120	μm
Mounting Torque	Mounting Screw: M3 See Figure 9	Recommended 0.7 N • m	0.6	0.7	0.8	N • m
		Recommended 7.1 kg • cm	6.2	7.1	8.1	kg • cm
Weight			−	11	−	g

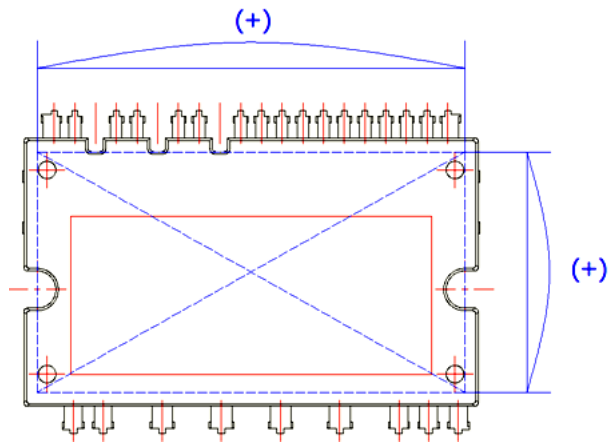
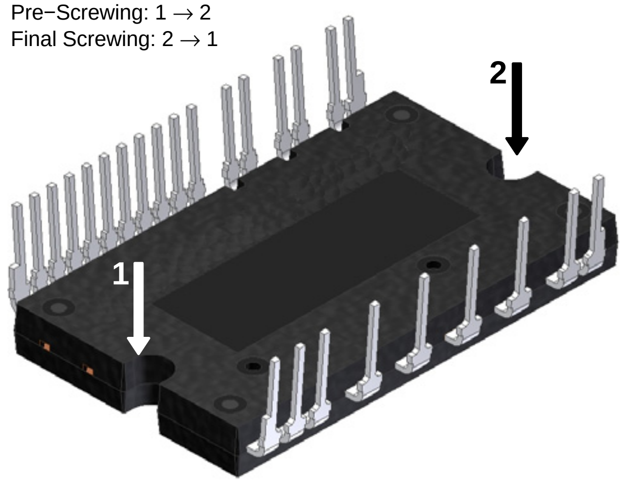


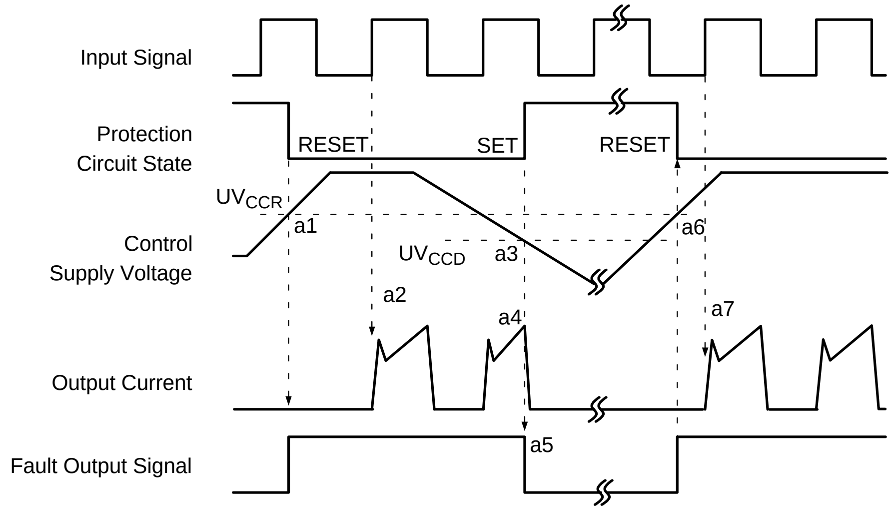
Figure 8. Flatness Measurement Position



NOTES:
13. Do not make over torque when mounting screws. Much mounting torque may cause ceramic cracks, as well as bolts and Al heat−sink destruction.
14. Avoid one side tightening stress. Figure 9 shows the recommended torque order for mounting screws. Uneven mounting can cause the ceramic substrate of the SPM 45 package to be damaged. The pre−screwing torque is set to 20~30% of maximum torque rating.

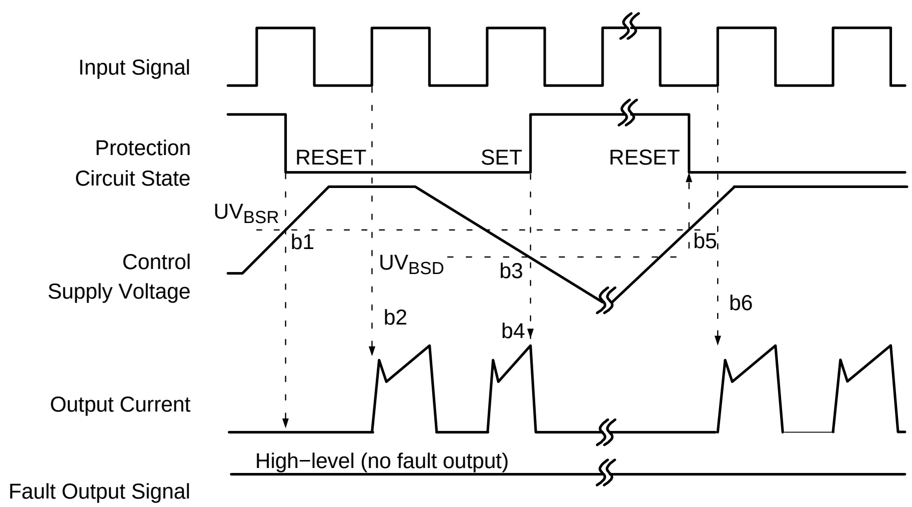
Figure 9. Mounting Screws Torque Order

TIME CHARTS OF PROTECTIVE FUNCTION



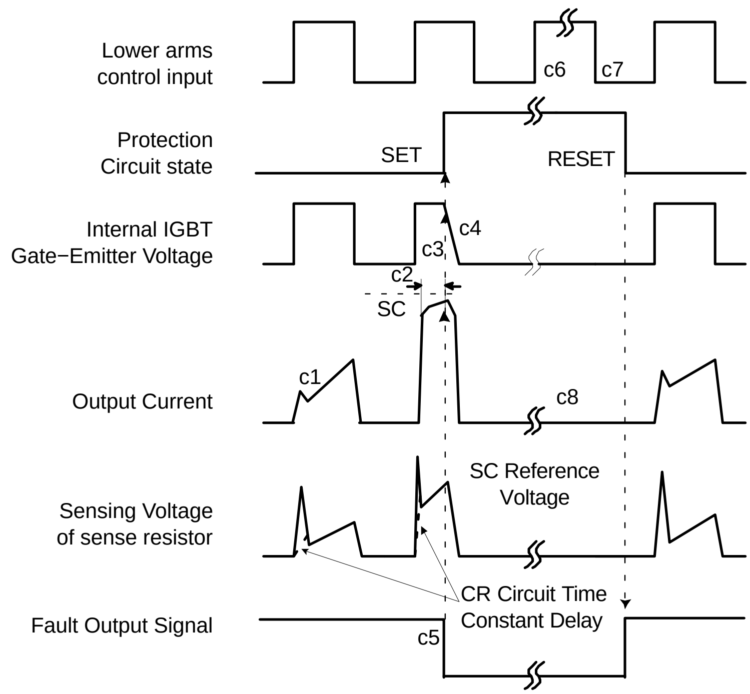
a1: Control supply voltage rises: after the voltage rises UV_{CCR}, the circuits start to operate when next input is applied.
a2: Normal operation: IGBT ON and carrying current.
a3: Under−voltage detection (UV_{CCD}).
a4: IGBT OFF in spite of control input condition.
a5: Fault output operation starts.
a6: Under−voltage reset (UV_{CCR}).
a7: Normal operation: IGBT ON and carrying current.

Figure 10. Under−Voltage Protection (Low−Side)



b1: Control supply voltage rises: after the voltage reaches UV_{BSR}, the circuits start to operate when next input is applied.
b2: Normal operation: IGBT ON and carrying current.
b3: Under−voltage detection (UV_{BSD}).
b4: IGBT OFF in spite of control input condition, but there is no fault output signal.
b5: Under−voltage reset (UV_{BSR}).
b6: Normal operation: IGBT ON and carrying current.

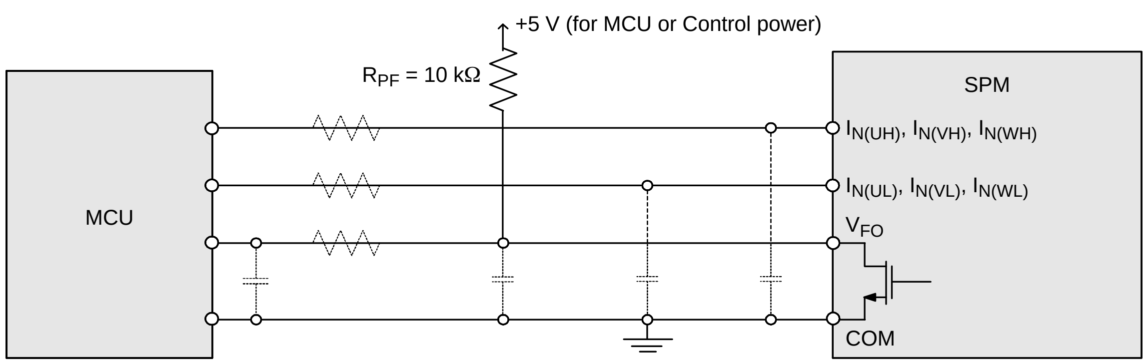
Figure 11. Under−Voltage Protection (High−Side)



(with the external shunt resistance and CR connection)
c1: Normal operation: IGBT ON and carrying current.
c2: Short−circuit current detection (SC trigger).
c3: Hard IGBT gate interrupt.
c4: IGBT turns OFF.
c5: Input "LOW": IGBT OFF state.
c6: Input "HIGH": IGBT ON state, but during the active period of fault output, the IGBT doesn't turn ON.
c7: IGBT OFF state.

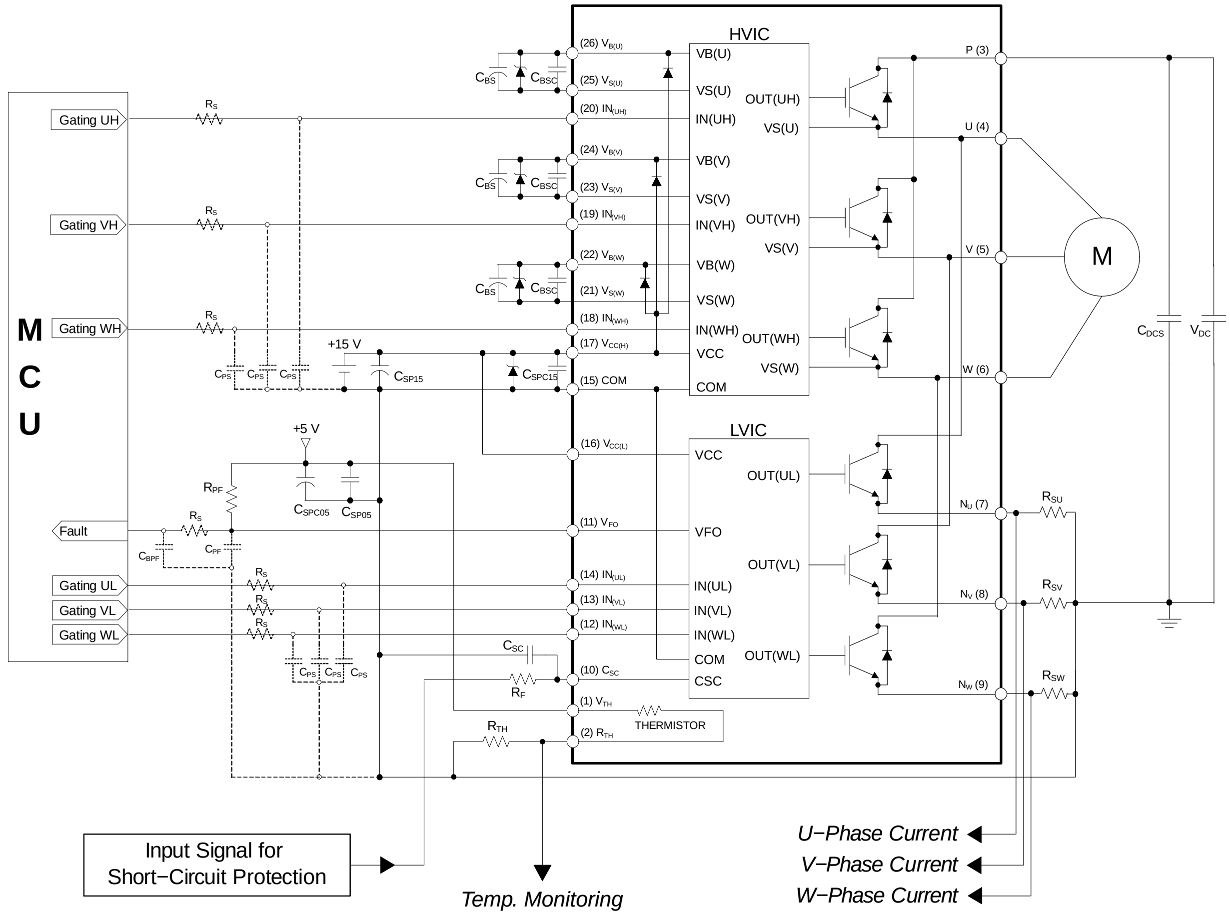
Figure 12. Short−Circuit Protection (Low−Side Operation Only)

INPUT/OUTPUT INTERFACE CIRCUIT



NOTE:
15. RC coupling at each input (parts shown dotted) might change depending on the PWM control scheme in the application and the wiring impedance of the application's printed circuit board. The input signal section of the Motion SPM 45 product integrates a 5 kΩ (typ.) pull−down resistor. Therefore, when using an external filtering resistor, pay attention to the signal voltage drop at input terminal.

Figure 13. Recommended MCU I/O Interface Circuit



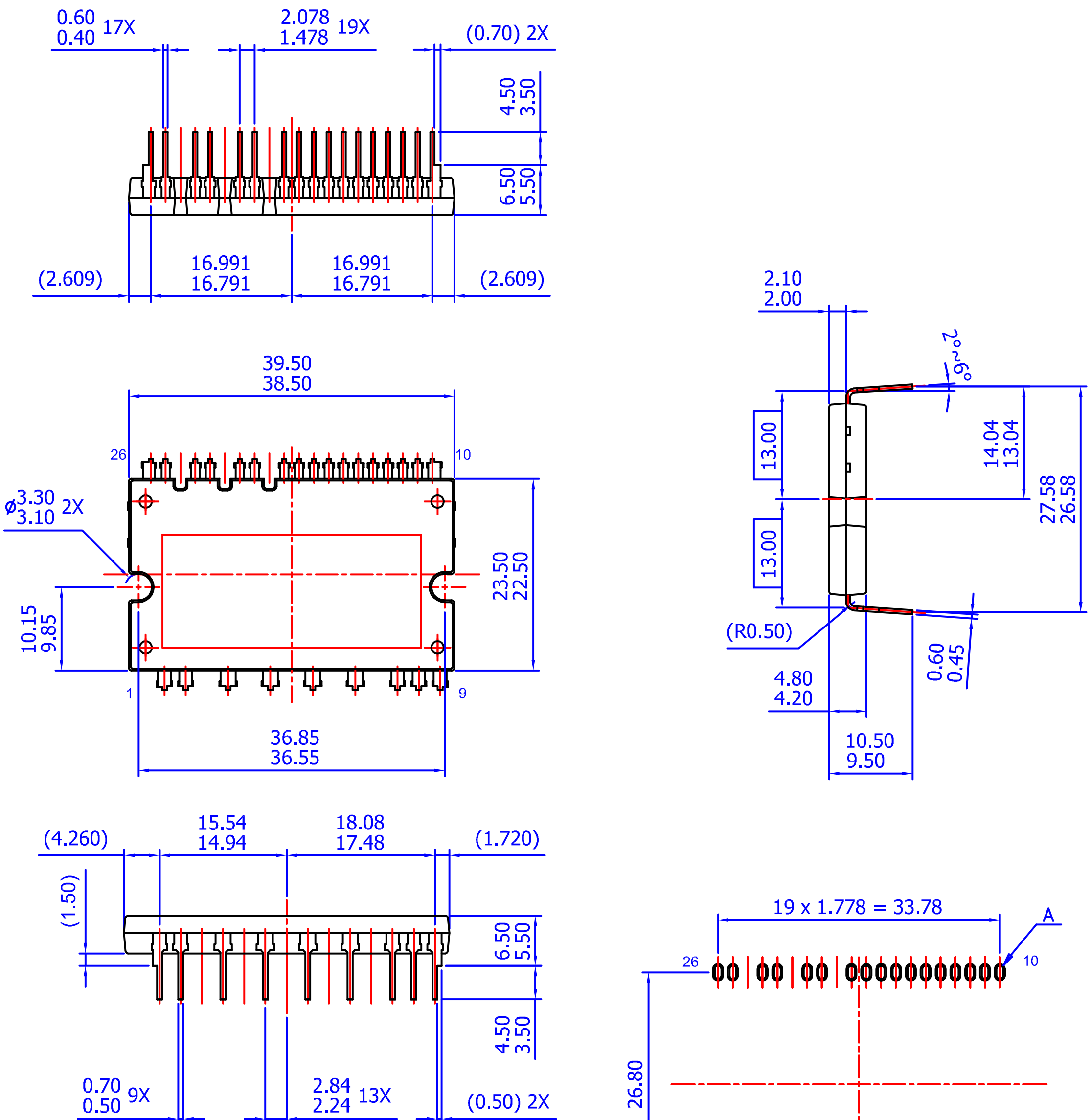
NOTES:

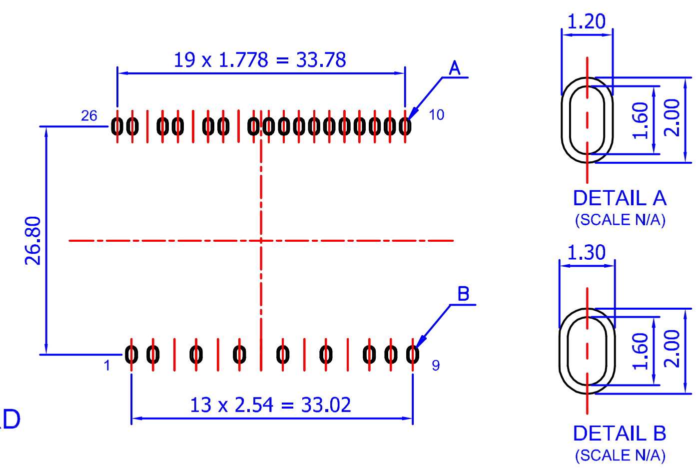
16. To avoid malfunction, the wiring of each input should be as short as possible (less than 2−3 cm).
17. By virtue of integrating an application−specific type of HVIC inside the Motion SPM 45 product, direct coupling to MCU terminals without any optocoupler or transformer isolation is possible.
18. V_{FO} output is open−drain type. This signal line should be pulled up to the positive side of the MCU or control power supply with a resistor that makes I_{FO} up to 1 mA (please refer to Figure 13).
19. C_{SP15} of around seven times larger than bootstrap capacitor C_{BS} is recommended.
20. Input signal is active−HIGH type. There is a 5 kΩ resistor inside the IC to pull down each input signal line to GND. RC coupling circuits is recommended for the prevention of input signal oscillation. R_SC_{PS} time constant should be selected in the range 50~ 50 ns (recommended R_S = 100 Ω, C_{PS} = 1 nF).
21. To prevent errors of the protection function, the wiring around R_F and C_{SC} should be as short as possible.
22. In the short−circuit protection circuit, please select the R_FC_{SC} time constant in the range 1.5~2 μs.
23. The connection between control GND line and power GND line which includes the N_U, N_V, N_W must be connected to only one point. Please do not connect the control GND to the power GND by the broad pattern. Also, the wiring distance between control GND and power GND should be as short as possible.
24. Each capacitor should be mounted as close to the pins of the Motion SPM 45 product as possible.
25. To prevent surge destruction, the wiring between the smoothing capacitor and the P & GND pins should be as short as possible. The use of a high−frequency non−inductive capacitor of around 0.1~0.22 μF between the P and GND pins is recommended.
26. Relays are used in almost every systems of electrical equipment in home appliances. In these cases, there should be sufficient distance between the MCU and the relays.
27. The zener diode or transient voltage suppressor should be adopted for the protection of ICs from the surge destruction between each pair of control supply terminals (recommended zener diode is 22 V / 1 W, which has the lower zener impedance characteristic than about 15 Ω).
28. Please choose the electrolytic capacitor with good temperature characteristic in C_{BS}. Also, choose 0.1~0.2 μF R−category ceramic capacitors with good temperature and frequency characteristics in C_{BSC}.
29. For the detailed information, please refer to the AN−9070, AN−9071, AN−9072, RD−344, and RD−345.

Figure 14. Typical Application Circuit

SPMAA−A26 / 26LD, PDD STD, CERAMIC TYPE, STANDARD DUAL FORM
CASE MODFA
ISSUE O

DATE 31 JAN 2017





LAND PATTERN RECOMMENDATIONS

NOTES: UNLESS OTHERWISE SPECIFIED
A) THIS PACKAGE DOES NOT COMPLY TO ANY CURRENT PACKAGING STANDARD
B) ALL DIMENSIONS ARE IN MILLIMETERS
C) DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS
D) ( ) IS REFERENCE

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DESCRIPTION:	**SPMAA−A26 / 26LD, PDD STD, CERAMIC TYPE, STANDARD DUAL**		**PAGE 1 OF 1**

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