IQS318 DATASHEET

Single channel standalone and I²C proximity or touch sensing controller. It features low power consumption and different adjustable settings such as sensitivity, sampling period, and sensing threshold.

1 Device Overview

The IQS318 ProxFusion® IC is both a standalone and I²C sensing device for single channel proximity or touch sensing requirements. The sensor is configurable via external input pins and on-chip calculations enable the IC to respond effectively in various use cases.

1.1 Main Features

- Multiple user interface options:
  - Single channel I²C / standalone inductive switch (with long term activation: IQS318-0xx)
  - Single channel I²C / standalone inductive button / single level trigger (IQS318-1xx)
  - Single channel I²C / standalone inductive snap button (IQS318-2xx)
  - Single channel I²C / standalone self-capacitive switch (with long term activation: IQS318-5xx)
- 1 (self) / 2 (inductive) external sensor pad connection
- DYCAL™ 2 solution: The IQS318-0xx and IQS318-5xx offers a dynamic calibration UI with intelligent hysteresis for long term detection
- Built-in basic functions:
  - Automatic tuning
  - Noise filtering
  - Debounce & hysteresis
- Built-in signal processing options:
  - Single I²C touch/proximity output
  - Single standalone touch output
- Design simplicity:
  - Configurable channel sensitivity, sample period, threshold, and charge transfer frequency using external input pins
  - One-time programmable settings for custom IC configuration (MOQs apply)
- I²C debugging interface with IRQ/RDY (up to Fast Mode Plus – 1 MHz)
- Supply voltage 1.71 V to 3.5 V
- Package options:
  - WLCSP11 (1.48 × 1.08 × 0.345 mm) – interleaved 0.35 mm × 0.35 mm ball pitch
  - DFN12 (3 × 3 × 0.75 mm) – 0.5 mm pitch
  - QFN20 (3 × 3 × 0.55 mm) – 0.4 mm pitch

Figure 1.1: WLCSP11

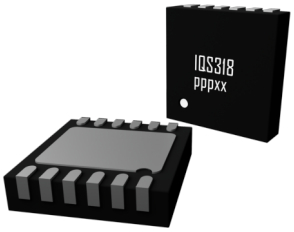

Figure 1.2: DFN12

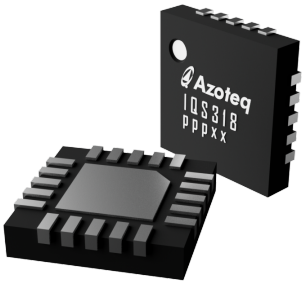

Figure 1.3: QFN20

1.2 Applications

- General-use button/switch
- Wear detection
- Backlight activation
- Tamper switch (release detection)

- Snap button

1.3 Block Diagram

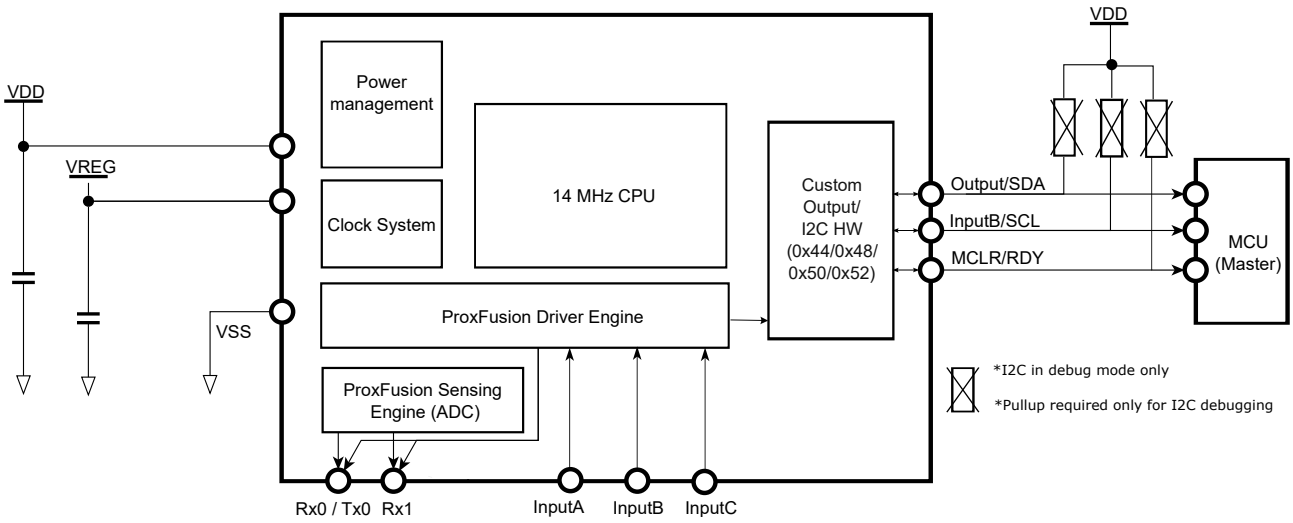

Figure 1.4: Functional Block Diagram

1.4 Order Code Description

1.4.1 IQS318-0xx

The IQS318-0xx is a single channel I²C (IQS318-000) / standalone (IQS318-001) inductive switch application that integrates the DYCAL™ 2 UI, suitable for long-term activations. See AZD137 for more information on the user interface.

Applications of the IQS318-0xx order codes include general-use inductive switches and tamper switches (release detection).

1.4.2 IQS318-1xx

The IQS318-1xx is a single channel I²C (IQS318-100) / standalone (IQS318-101) inductive button application without the DYCAL™ 2 UI.

Applications of the IQS318-1xx order codes include general-use inductive buttons that will recover automatically even if a harsh environment causes them to become latched accidentally.

1.4.3 IQS318-2xx

The IQS318-2xx is a single channel I²C (IQS318-200) / standalone (IQS318-202) inductive button application without the DYCAL™ 2 UI.

Applications of the IQS318-2xx order codes include inductive snap buttons. The IQS318-2xx also covers a wide range of snap domes and PCB overlays. The algorithm of this solution is tuned for the snap button profile rather than just a threshold crossing. A single sensitivity setting applies to various different snap-dome and overlay combinations. An alternate excitation frequency option exists for applications where multiple inductive coils are placed next to each other. This prevents interference

between coils. Alternating coil frequencies are recommended when placing multiple coils next to each other.

1.4.4 IQS318-5xx

The IQS318-5xx is a single channel I^2C (IQS318-510) / standalone (IQS318-512) capacitive switch application that integrates the DYCAL™ 2 UI, suitable for long-term activations. See AZD137 for more information on the user interface.

Applications of the IQS318-5xx order codes include capacitive wear detection, lid open-close switches, and backlight activation.

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2 Hardware Connection

2.1 WLCSP11 Pin Diagram

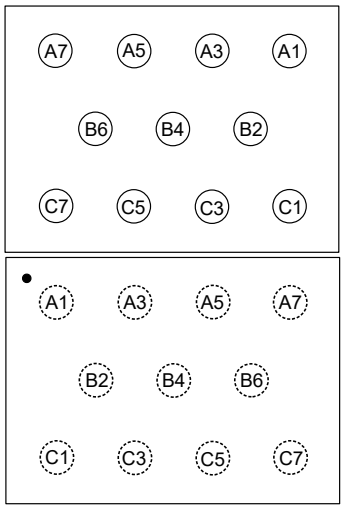


Table 2.1: 11-pin WLCSP11 Package

Pin no.	Signal
A7	VSS
A5	Output/SDA
A3	VREG
A1	Rx1
B6	InputA
B4	Unused
B2	Rx0/Tx0
C7	MCLR/RDY
C5	VDD
C3	InputB/SCL
C1	InputC

2.2 DFN12 Pin Diagram

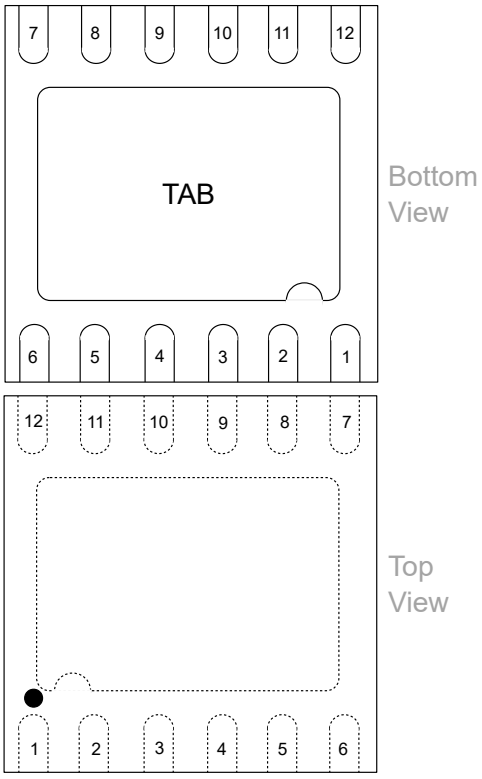
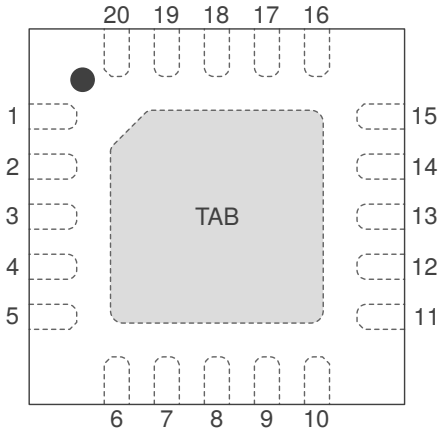


Table 2.2: 12-pin DFN Package

Pin no.	Signal
1	InputA
2	Output/SDA
3	VDD
4	VREG
5	InputB/SCL
6	InputC
7	Rx0/Tx0
8	NC
9	Rx1
10	Unused
11	MCLR/RDY
12	VSS

2.3 QFN20 Pin Diagram



Top View

Table 2.3: 20-pin QFN Package (Top View)

Pin no.	Signal	Pin no.	Signal
1	InputC	11	NC
2	Rx0/Tx0	12	NC
3	Rx1	13	NC
4	NC	14	NC
5	NC	15	NC
6	VREG	16	NC
7	Unused	17	MCLR/RDY
8	VDD	18	InputA
9	VSS	19	Output/SDA
10	NC	20	InputB/SCL

Area name	Signal
TAB[i]	Thermal pad (floating)

[i] It is recommended to connect the thermal pad (TAB) to VSS.

2.4 Signal Descriptions

Table 2.4: Signal Descriptions

Function	Signal Name	Signal Type	Pin Type[ii]	Description
ProxFusion®	Rx0/Tx0	Analog	IO	ProxFusion® channel
	Rx1	Analog	IO	
	InputC	Digital	IO	
	InputA	Digital	IO	InputA pad
	Unused	N/A	IO	Unused pad
GPIO	MCLR/RDY	Digital	IO	Active pull-up, 200k resistor to VDD. Pulled low during Power-on Reset (POR[iii]), and MCLR function enabled by default. VPP input for OTP
Digital Out/I²C	Output/SDA	Digital	IO	Digital Output / I²C Data (Debugging)
	InputB/SCL	Digital	IO	Digital Output / I²C Clock (Debugging)
Power	VDD	Power	P	Power supply input voltage
	VREG	Power	P	Internal regulated supply output
	VSS	Power	P	Analog/Digital Ground

[ii] Pin Types: I = Input, O = Output, I/O = Input or Output, P = Power
[iii] POR is used to reference a clean reset state after power-on.

2.5 Reference Schematic

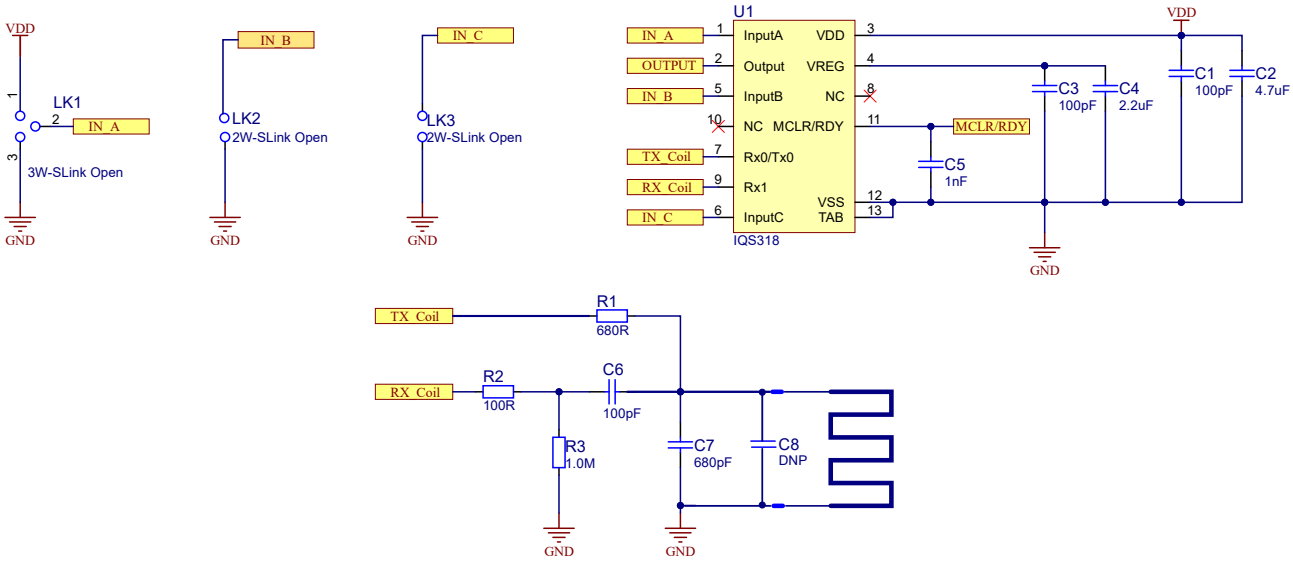


Figure 2.1: DFN12 Inductive Reference Schematic (IQS318-0xx, IQS318-1xx, and IQS318-2xx)[i]

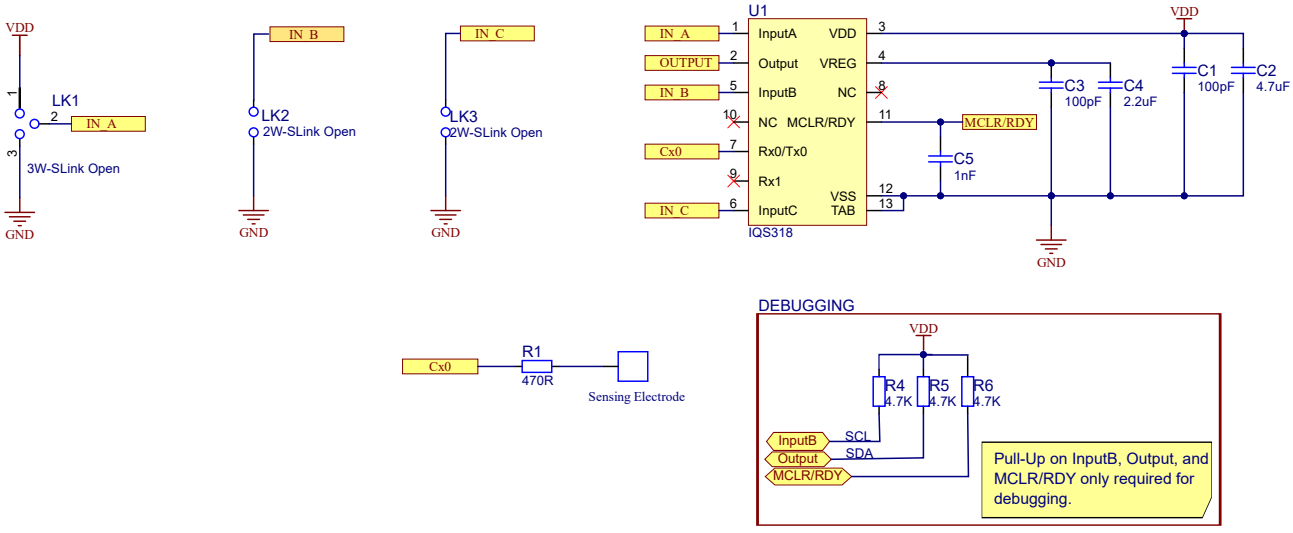


Figure 2.2: DFN12 Self-Capacitive Reference Schematic (IQS318-5xx)[i]

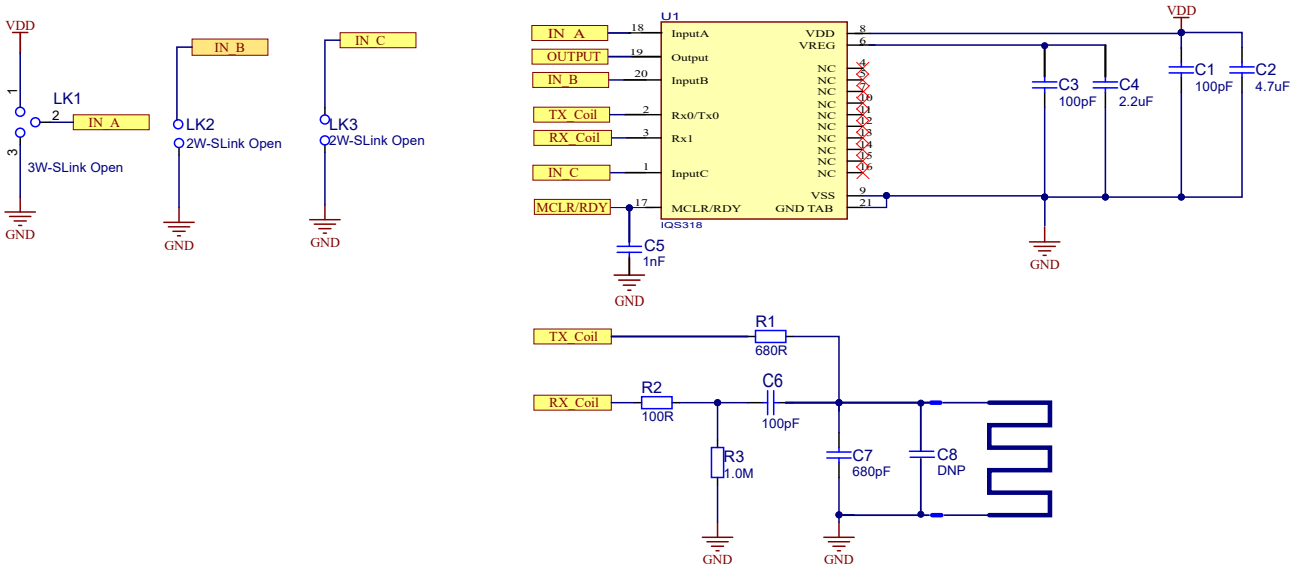


Figure 2.3: QFN20 Inductive Reference Schematic (IQS318-0xx, IQS318-1xx, and IQS318-2xx)[i]

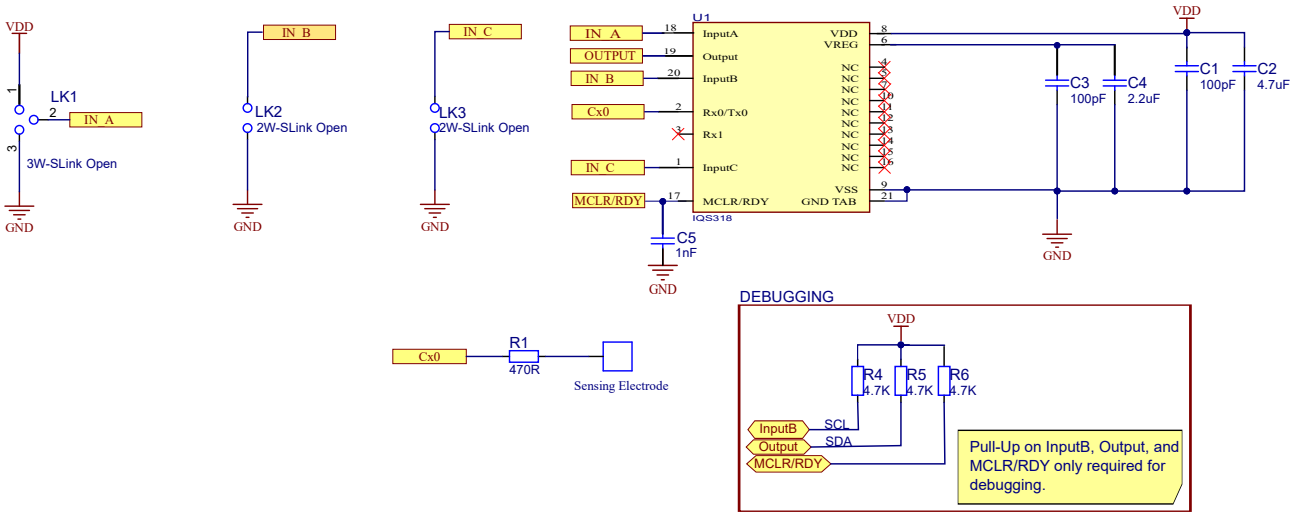


Figure 2.4: QFN20 Self-Capacitive Reference Schematic (IQS318-5xx)[i]

[i] For I²C debugging, 4.7 kΩ pull-ups are required on Output/SDA, InputB/SCL and MCLR/RDY.

3 Electrical Characteristics

3.1 Absolute Maximum Ratings

	Min	Max	Unit
Voltage applied at VDD pin to VSS	1.71	3.6	V
Voltage applied to any ProxFusion® pin	-0.3	VREG	V
Voltage applied to any other pin (referenced to VSS)	-0.3	VDD + 0.3 (3.6 V max)	V
Storage temperature, T_{stg}	-40	85	°C

3.2 Recommended Operating Conditions

Recommended operating conditions		Min	Nom	Max	Unit
VDD	Supply voltage applied at VDD pin	1.71		3.6	V
VREG	Internal regulated supply output for analog domain		1.53		V
VSS	Supply voltage applied at VSS pin	0	0	0	V
T_A	Operating free-air temperature	–40	25	85	°C
C_{VDD}	Recommended capacitor at VDD	$2\times C_{VREG}$	$3\times C_{VREG}$		µF
C_{VREG}	Recommended external buffer capacitor at VREG, ESR≤ 200 mΩ	2[i]	5	13	µF
Cm_{Tx-Rx}	Capacitance of all external electrodes on all ProxFusion® blocks (mutual-capacitance mode)	0.1	-	9	pF
Cp_{Rx-VSS}	Maximum capacitance of all external electrodes on all ProxFusion® blocks Mutual-capacitance mode, F_{xfer} = 1 MHz Mutual-capacitance mode, F_{xfer} = 4 MHz			 100 25	pF
$\frac{Cx_{RX-VSS}}{Cm_{TX-RX}}$	Capacitance ratio for optimal SNR in mutual capacitance mode	10		20	n/a
$RCx_{Rx/Tx}$	Series (in-line) resistance of all mutual-capacitance pins (Tx & Rx pins) in mutual-capacitance mode	0[ii]	0.47	10[iii]	kΩ

3.3 ESD Rating

		Value	Unit
$V_{(ESD)}$ Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[iv]	± 2000	V

[i] Absolute minimum allowed capacitance value is 1 µF, after taking derating, temperature, and worst-case tolerance into account. Please refer to the AZD004 application note for more information regarding capacitor derating.

[ii] Nominal series resistance of 470 Ω is recommended to prevent received and emitted EMI effects. Typical resistance also adds additional ESD protection.

[iii] Series resistance limit is a function of F_{xfer} and the circuit time constant, RC. $R_{max} \times C_{max} = \frac{1}{(6\times F_{xfer})}$ where C is the pin capacitance to VSS.

[iv] JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Pins listed as ±2000 V may actually have higher performance.

3.4 Current Consumption

3.4.1 IQS318-000: I²C Inductive Switch (DYCAL™ 2 UI)

Configuration	Sampling period [ms]	Active channels	Typical Power Consumption [µA] 3.3V[v]
InputC floating	200	Inductive (1 channel)	4.5
InputC to VSS	43	Inductive (1 channel)	25.6

3.4.2 IQS318-001: Standalone Inductive Switch (DYCAL™ 2 UI)

Configuration	Sampling period [ms]	Active channels	Typical Power Consumption [µA] 3.3V[v]
InputC floating	200	Inductive (1 channel)	4.3
InputC to VSS	43	Inductive (1 channel)	24.4

3.4.3 IQS318-100: I²C Inductive Button

Configuration	Sampling period [ms]	Active channels	Typical Power Consumption [µA] 3.3V[v]
InputC floating	200	Inductive (1 channel)	4.6
InputC to VSS	43	Inductive (1 channel)	15.2

3.4.4 IQS318-101: Standalone Inductive Button

Configuration	Sampling period [ms]	Active channels	Typical Power Consumption [µA] 3.3V[v]
InputC floating	200	Inductive (1 channel)	4.3
InputC to VSS	43	Inductive (1 channel)	17.3

3.4.5 IQS318-200: I²C Inductive Snap Button

Configuration	Sampling period [ms]	Active channels	Typical Power Consumption [µA] 3.3V[v]
InputC floating	200	Inductive (1 channel)	4.7
InputC to VSS	43	Inductive (1 channel)	24.8

3.4.6 IQS318-202: Standalone Inductive Snap Button

Configuration	Sampling period [ms]	Active channels	Typical Power Consumption [µA] 3.3V[v]
InputC floating	200	Inductive (1 channel)	4.3
InputC to VSS	43	Inductive (1 channel)	14.6

3.4.7 IQS318-510: I²C Self-Capacitive Switch (DYCAL™ 2 UI)

Configuration	Sampling period [ms]	Active channels	Typical Power Consumption [µA] 3.3V[v]
InputC floating	200	Self-capacitance (1 channel)	3.6
InputC to VSS	43	Self-capacitance (1 channel)	9.6

3.4.8 IQS318-512: Standalone Self-Capacitive Switch (DYCAL™ 2 UI)

Configuration	Sampling period [ms]	Active channels	Typical Power Consumption [µA] 3.3V[v]
InputC floating	200	Self-capacitance (1 channel)	3.1
InputC to VSS	43	Self-capacitance (1 channel)	8.3

[v] Long term averages - higher power consumption expected momentarily during activated states.

4 Timing and Switching Characteristics

4.1 Reset Levels

Table 4.1: Reset Levels

Parameter		Min	Max	Unit
V_{VDD}	Power-up (Reset trigger) – slope > 100 V/s		1.65	V
	Power-down (Reset trigger) – slope < –100 V/s	0.9		

4.2 MCLR Pin Levels and Characteristics

Table 4.2: MCLR Pin Characteristics

Parameter		Test Conditions	Min	Typ	Max	Unit
$V_{IL(MCLR)}$	MCLR Input low level voltage	VDD = 3.3 V	VSS – 0.3	-	1.05	V
		VDD = 1.7 V			0.75	
$V_{IH(MCLR)}$	MCLR Input high level voltage	VDD = 3.3 V	2.25	-	VDD + 0.3	V
		VDD = 1.7 V	1.05			
$R_{PU(MCLR)}$	MCLR pull-up equivalent resistor		180	210	240	kΩ
$t_{PULSE(MCLR)}$	MCLR input pulse width – no trigger	VDD = 3.3 V	-	-	15	ns
		VDD = 1.7 V			10	
$t_{TRIG(MCLR)}$	MCLR input pulse width – ensure trigger		250	-	-	ns

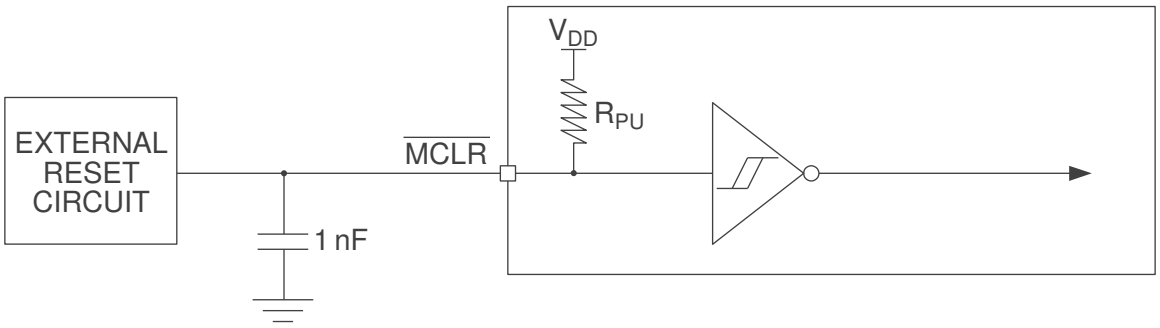


Figure 4.1: MCLR Pin Diagram

4.3 Digital I/O Characteristics

Table 4.3: Digital I/O Characteristics

Parameter		Test Conditions	Min	Max	Unit
V_{OL}	Output/SDA & InputB/SCL Output low voltage	I_{sink} = 20 mA		0.3	V
V_{OH}	Output high voltage	I_{source} = 20 mA	VDD – 0.2		V
V_{IL}	Input low voltage			VDD × 0.3	V
V_{IH}	Input high voltage		VDD × 0.7		V
C_{b_max}	SDA & SCL maximum bus capacitance			550	pF

4.4 I²C Characteristics

Table 4.4: I²C Characteristics

Parameter		VDD	Min	Max	Unit
f_{SCL}	SCL clock frequency	1.8 V, 3.3 V		1000	kHz
$t_{HD,STA}$	Hold time (repeated) START	1.8 V, 3.3 V	0.26		µs
$t_{SU,STA}$	Setup time for a repeated START	1.8 V, 3.3 V	0.26		µs
$t_{HD,DAT}$	Data hold time	1.8 V, 3.3 V	0		ns
$t_{SU,DAT}$	Data setup time	1.8 V, 3.3 V	50		ns
$t_{SU,STO}$	Setup time for STOP	1.8 V, 3.3 V	0.26		µs
t_{SP}	Pulse duration of spikes suppressed by input filter	1.8 V, 3.3 V	0	50	ns

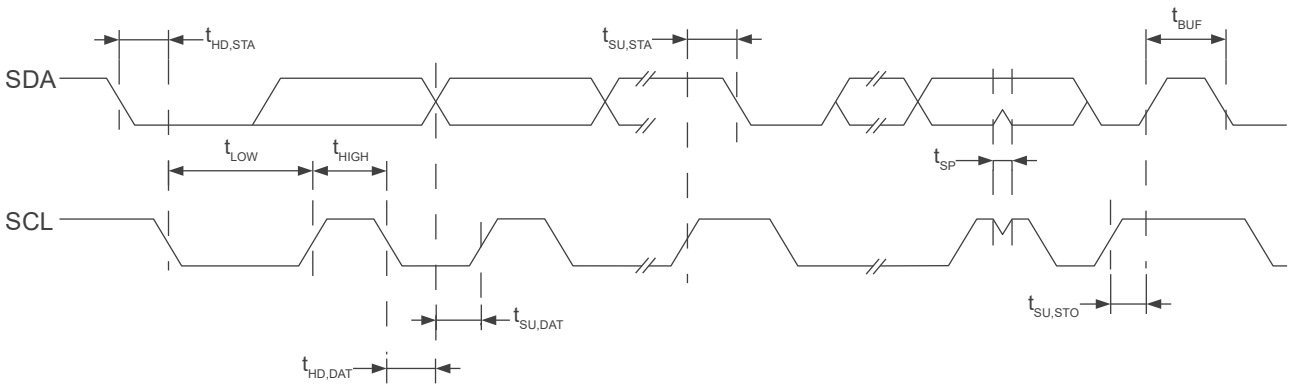


Figure 4.2: I²C Mode Timing Diagram

5 Basic Standalone Functionality

5.1 Input Pin Functionality

The IQS318 offers three input pins that can be used to adjust the threshold, sensitivity, sampling period, and charge transfer frequency. Table 5.1 shows the different input pin configurations.

Table 5.1: IQS318 input pin description

Input pin	Floating	VDD[i]	VSS[ii]
InputA[iii]	N/A	**InputA IQS318-2xx order code:** 14MHz charge transfer frequency	**InputA IQS318-2xx order code:** 7MHz charge transfer frequency
		InputA other order codes: High threshold (less sensitive)	**InputA other order codes:** Low threshold (more sensitive)
InputB[iv]	High sensitivity	N/A	Low sensitivity
InputC[v]	Low sampling period	N/A	High sampling period

Note: Debugging is not possible when InputB/SCL is shorted to VSS. Both InputB/SCL and Output/SDA must have pull-up resistors connected.

5.2 Output Pin Functionality

The Output pin is used to indicate when a touch event has occurred. This pin is configured as a push-pull active low pin and is set to VSS when a touch is detected, and to VDD when a release event is detected. The IQS318 power-on state description is shown in Table 5.2.

Table 5.2: IQS318 power-on state description

IC order option (all output active low)	POR state of the Output pin	Output pin state description
IQS318-000	High	Not in touch
IQS318-001	High	Not in touch
IQS318-100	High	Not in touch
IQS318-101	High	Not in touch
IQS318-200	High	Not in touch
IQS318-202	High	Not in touch
IQS318-510	Low	In touch / In wear / Lid closed
IQS318-512	Low	In touch / In wear / Lid closed

[i] Pins are shorted to VDD.
[ii] Pins are shorted to VSS.
[iii] InputA should never be left floating. The IQS318-2xx use InputA to set the charge transfer frequency (f_{xfer}) while all the remaining order codes use InputA to set the threshold.
[iv] When InputB is left floating, the internal pull-up is enabled and InputB is pulled high. InputB must not be pulled high externally to VDD.
[v] InputC must not be pulled high to VDD.

5.3 Standalone Power On Sequence of the IQS318-512

On startup, the output of the IQS318-512 will follow the sequence shown in Figures 5.1 and 5.2. The time interval, t_{init}, is typically less than 12 ms and t_{start_up}, is typically less than 250 ms.

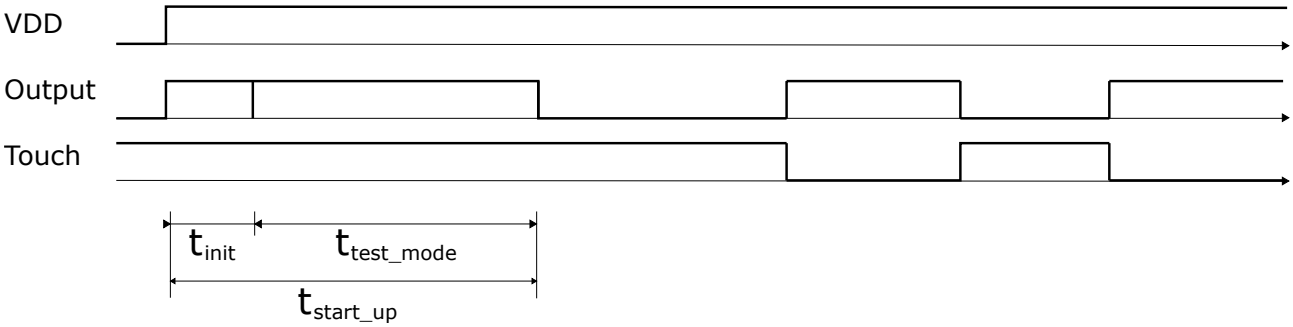


Figure 5.1: IQS318-512 output timing diagram (touch at POR)

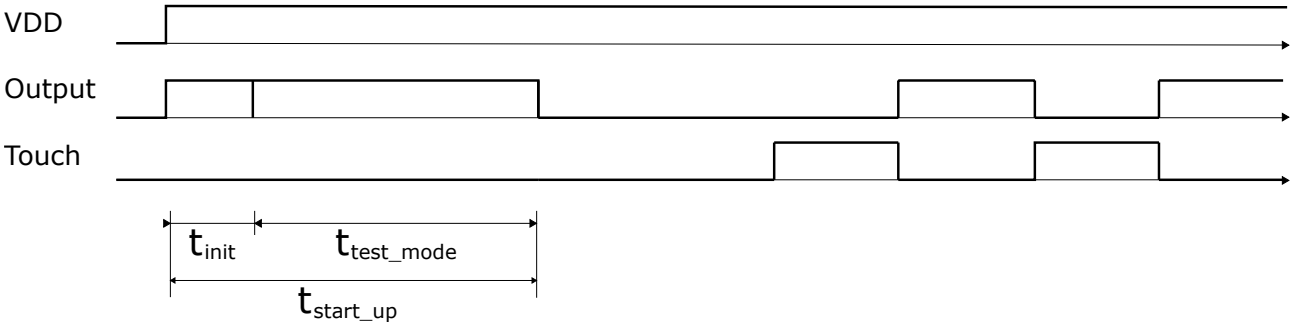


Figure 5.2: IQS318-512 output timing diagram (no touch at POR)

5.4 Standalone Power On Sequence of the IQS318-001, IQS318-101, and IQS318-202

For the IQS318-001, IQS318-101, and IQS318-202 order codes, the output on startup will follow the sequence shown in Figures 5.3 and 5.4. The time interval, t_{init}, is typically less than 12 ms and t_{start_up}, is typically less than 250 ms.

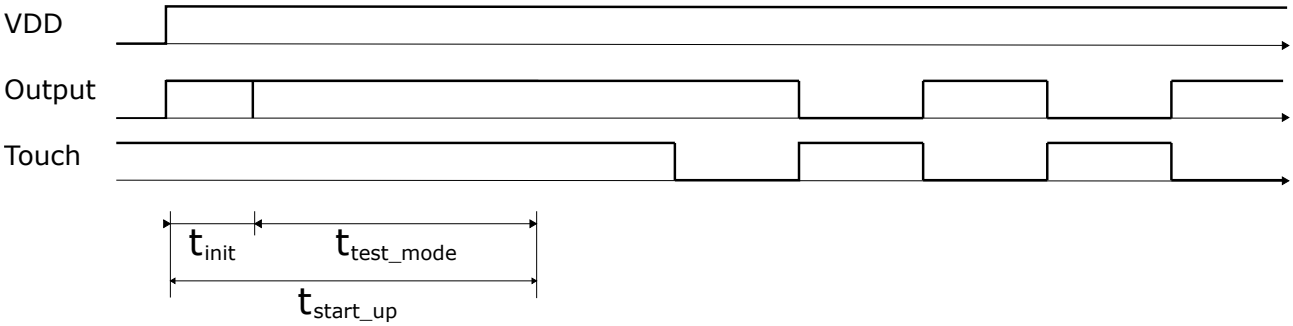


Figure 5.3: IQS318-001, IQS318-101, and IQS318-202 output timing diagram (touch at POR)

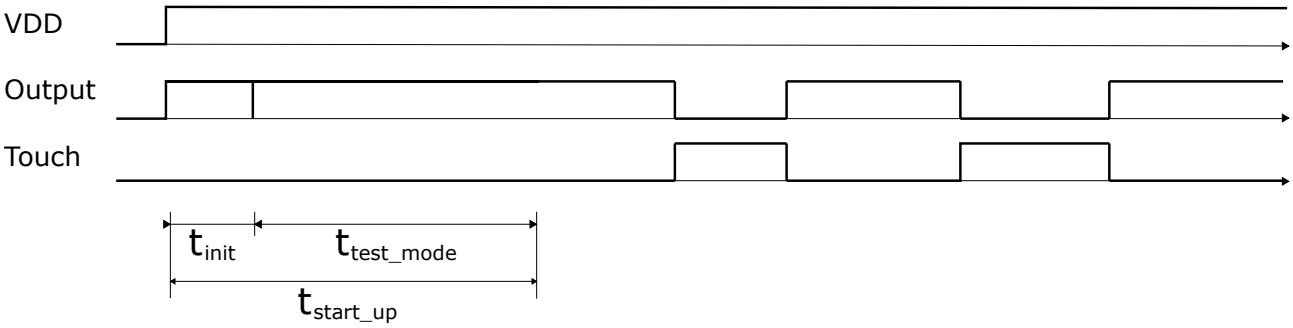


Figure 5.4: IQS318-001, IQS318-101, and IQS318-202 output timing diagram (no touch at POR)

6 ProxFusion® Module

The IQS318 contains a single ProxFusion® module that uses patented technology to measure and process the sensor data.

6.1 Channel Options

The single channel inductive sensors (IQS318-0xx, IQS318-1xx, and IQS318-2xx), and the single channel self-capacitive sensor (IQS318-5xx), are intended for basic standalone and I^2C inductive and capacitive applications.

- AZD125: Capacitive Sensing Design Guide
- AZD115: Inductive Sensing Application Note

6.2 Low Power Options

The standalone options for the IQS318 offer two sampling period configurations. The low sampling period (low SP) is used for applications that do not require a highly responsive output and have lower power consumption. On the other hand, the high sampling period (high SP) is suitable for applications that require a more immediate response, such as repetitive button taps.

6.3 Count Value

The sensing measurement determines a *count value* for the sensing channel. Count values are inversely proportional to the actual analog change in capacitance or inductance, and all outputs are derived from this.

6.3.1 Max Counts

Each channel is limited to having a count value smaller than the *maximum counts*. If the ATI setting or hardware causes a measured count value higher than this, the conversion will be stopped, and the counts will be limited to the maximum value.

6.4 Long-Term Average (LTA)

User interaction is detected by comparing the measured count values to a reference value known as the *LTA*. The LTA of the sensor is slowly updated to track changes in the environment and is not updated during user interaction.

6.4.1 Reseed

When a reseed event occurs the LTA is seeded with the current counts value. Therefore, a reseed event will exit any touch or proximity conditions. The IQS318 automatically handles reseed events and a reseed command can be given by setting the *Reseed* bit in the *System Control* register.

6.5 Automatic Tuning Implementation (ATI)

The ATI is an advanced technological feature implemented in ProxFusion® devices to allow optimal performance of the devices for a wide range of sensing electrode capacitances and inductances without modification to external components. The ATI settings allows the tuning of various parameters. For a detailed description of the ATI see AZD004.

6.6 Automatic Re-ATI

6.6.1 Description

Re-ATI will be triggered if certain conditions are met. One of the most important features of the Re-ATI is that it allows easy and fast recovery from an incorrect ATI, such as when performing ATI during user interaction with the sensor. This could cause the wrong ATI compensation to be configured, since the user affects the capacitance or inductance of the sensor. A Re-ATI would correct this. Automatic re-ATI is always enabled on the IQS318. For debugging, when a Re-ATI is performed on the IQS318, a status bit will be set momentarily to indicate that this has occurred.

6.6.2 Conditions for Re-ATI to Activate

A Re-ATI is performed when the reference of a channel drifts outside the acceptable range from the ATI Target. The boundary where Re-ATI occur for a given channel can be adjusted in the registers listed in Appendix A.9.

$$\text{Re-ATI Boundary= ATI target} \pm \left(\frac{1}{8} \times \text{ATI Target}\right) \tag{1}$$

For example, assume that the ATI target is configured to 800 and the boundary value is $\frac{1}{8} \times 800 = 100$. If Re-ATI is enabled, the ATI algorithm will be repeated under the following conditions:

$$\text{LTA} > 900 \text{ or } \text{LTA} < 700$$

The ATI algorithm executes in a short time, so it goes unnoticed by the user.

6.6.3 ATI Error

After the ATI algorithm is performed, a check is done to see if there was any error with the algorithm. An ATI error is reported if one of the following conditions is true for the sensing channel after the ATI is completed:

- ATI Compensation = 0 (min value)
- ATI Compensation = 1023 (max value)
- Count is already outside the Re-ATI range upon completion of the ATI algorithm

If any of these conditions are met, the corresponding error flag will be set (*ATI Error*). The flag status is only updated again when a new ATI algorithm is performed.

Note: Re-ATI will not be repeated immediately if an ATI Error occurs. This is to prevent the Re-ATI repeating indefinitely. An ATI error should however not occur under normal circumstances.

6.7 Channel Outputs

6.7.1 Channel Proximity

A channel proximity event occurs when the channel proximity threshold has been reached and this happens when a target comes into close proximity with the sensing electrode. A channel proximity output is debounced (see Appendix A.12), and the proximity threshold configured is a delta value (see Appendix A.12) measuring how much a channel's count value has deviated from the reference/LTA value.

6.7.2 Channel Touch

A channel touch event occurs when the touch threshold has been reached. The touch threshold can be calculated as:

$$\text{Threshold} = \text{value} \times \frac{\text{LTA}}{256} \tag{2}$$

The touch hysteresis value determines the corresponding touch release threshold. The release threshold can be calculated as:

$$\text{Release threshold} = \frac{\text{LTA}}{256} \times (\text{Threshold value - Hysteresis value}) \tag{3}$$

6.7.3 Channel Touch Direction

When a channel touch event occurs, the touch direction flag indicates whether the touch is positive or negative. This is only applicable to the IQS318-0xx and IQS318-5xx order codes that make use of the DYCAL™ 2 UI and the dual direction setting.

6.8 Power Mode Timeout

In order to optimise the power consumption and the performance, the power modes are "stepped" by default in order to move to power efficient modes when no interaction has been detected for a certain (configurable) time, known as the "power mode timeout".

6.9 Sensor Setup

6.9.1 Channel Setup

The channel sensitivity, threshold, sampling period, and charge transfer frequency can be adjusted using three input pins on the IQS318. For more information see Section 5.1.

6.9.2 Channel Default Settings

The default settings for the channel sensitivity, sampling period, proximity and touch event timeout are shown below.

Table 6.1: Default Channel Settings

Order Codes	Prox Timeout [s]	Touch Timeout [s]	Sampling Period [ms]		Sensitivity	
			Slow	Fast	Low	High
IQS318-0xx	20	20	200	43	Base: 200 Target: 300	Base: 150 Target: 750
IQS318-1xx						
IQS318-2xx						
IQS318-5xx						

6.9.3 Charge Transfer Frequency

The charge transfer frequency (f_{xfer}) is set to a default of 14 MHz for the IQS318-0xx, IQS318-1xx, and IQS318-2xx order codes, and 1 MHz for the IQS318-5xx order code unless otherwise indicated. F_{OSC} can be used as the Tx frequency by setting the *F_{OSC} Tx Frequency* bit in the *Sensor Setup* register.

Note: f_{xfer} is configurable and for more information about the usage of f_{xfer} for an inductive resonant tank design, see Appendix B.

6.9.4 Filter Betas

An Infinite Impulse Response (IIR) filter is applied to the digitised raw input for both the counts value and the LTA. There are two sets of filter settings for the IQS318-0xx, IQS318-1xx, and IQS318-5xx of which one must be selected at startup depending on the configured sampling period (SP). Normal power low SP and ULP low SP filter settings are used for a low sampling period, while normal power high SP and ULP high SP filter settings are used for a high sampling period. For the IQS318-2xx the same filter settings are used for the two power modes.
The damping factor can be calculated as:

$$\text{Damping factor} = \frac{\text{Beta}}{256} \tag{4}$$

6.10 Watchdog Timer

The IQS318 implements a hardware watchdog timer. The watchdog timer is set to expire after 255 ms if not reset and it will trigger a software reset upon expiration.

During I^2C communication the watchdog timer will reset whenever a read or write occurs. If the master initiates communication by sending an I^2C START condition and does not complete the I^2C transaction within 255 ms, the IQS318 device will reset.

The I^2C transaction is completed either when an I^2C STOP notification is sent by the master or when the master ends the communication as described in Section 7.13.

6.11 Hardware Reset

The MCLR pin (active low) can be used to hard reset the device. For more details see Section 4.2.

7 I²C Interface

7.1 Debug Mode

The IQS318 provides a debug mode or I²C streaming mode for all standalone versions of the product. The debug window enables the user to test different settings and the functionalities of the three input selections described in Section 5.1.

7.2 Conditions for Debugging

The debug window is made available on the standalone devices on startup if the following conditions are met:

- The states of Output/SDA and InputB/SCL pins must be high
- There must be a pull-up on RDY

Note: The debug window is only available for a brief period of time (based on the *I²C Transaction Timeout*). If no I²C communication request has been received during this period of time, the device goes into standalone mode.

7.3 Debug Mode to Standalone Mode

In debug mode, the user can test different settings, change register values, and then switch back to standalone mode with the updated settings. In standalone mode the I²C functionality is terminated until the next power cycle.

In addition to the three input selections described in Section 5.1, other engineering settings that can be configured by the user are given in this section and in Section 6.

Note: When you switch from debug to standalone mode, the input pin selections are ignored.

7.4 I²C Streaming Mode

For all I²C versions of the product, the IQS318 device goes directly into streaming mode after power on reset.

7.5 I²C Module Specification

The device supports a standard two wire I²C interface with the addition of a RDY (ready interrupt) line. The RDY pin also serves as a Master Clear (MCLR) and can be used to hard reset the device (see Section 6.11). The communications interface of the IQS318 supports the following:

- *Fast-Mode-Plus* standard I²C up to 1MHz.
- Streaming data as well as event mode.
- The provided interrupt line (RDY) is an open-drain active-low implementation and indicates a communication window.

The IQS318 implements 8-bit addressing with 2 bytes at each address.

7.6 I²C Address

The 7-bit device address for the IQS318-5xx order code is 0x44 (‘01000100’). Thus, the full address byte for address 0x44 will be 0x89 (read) or 0x88 (write).

The 7-bit device address for the IQS318-0xx order code is 0x48 (‘01001000’). Thus, the full address byte for address 0x48 will be 0x91 (read) or 0x90 (write).

The 7-bit device address for the IQS318-1xx order code is 0x50 (‘01010000’). Thus, the full address byte for address 0x50 will be 0xA1 (read) or 0xA0 (write).

The 7-bit device address for the IQS318-2xx order code is 0x52 (‘01010010’). Thus, the full address byte for address 0x52 will be 0xA5 (read) or 0xA4 (write).

7.7 I³C Compatibility

This device is not compatible with an I³C bus due to clock stretching allowed for data retrieval.

7.8 Communication During ATI

If an ATI event is triggered then I²C communications are disabled for the duration of the ATI process.

7.9 Memory Map Addressing and Data

The memory map implements 8-bit addressing. Data is formatted as 16-bit words meaning that two bytes are stored at each address. For example, address 0x10 will provide two bytes. The next two bytes read will be from address 0x11.

The 16-bit data is sent in little endian byte order (least significant byte first).

7.10 RDY/IRQ

The communication has an open-drain active-low RDY signal to inform the master that updated data is available. It is optimal for the master to use this as an interrupt input and initiate I²C reads accordingly.

The RDY line allows the master MCU to be woken from low-power/sleep when user presence is detected by the touch device. It is recommended that the RDY be placed on an interrupt-on-pin-change input on the master. On the IQS318 the RDY line also serves as an MCLR pin. MCLR functionality is described in Section 6.11.

7.11 Communications Window

When the device has data for the master, it will pull the RDY line low. This indicates that the device has opened its communications window and it is expecting the master to address it. When the communication window is closed the RDY line is released. For information on when the communications window is closed see Section 7.13.

Transfer of data between the master and slave must occur during the communications window (RDY is low). If the master wishes to initiate communication, a *Force Communications Request* must be made, after which the master should wait for the slave to pull RDY low before attempting to read or write. Section 7.16.2 describes the *Force Communications Request* sequence.

7.12 I²C Communication Timeout

If the communication window is not serviced within the *I²C Timeout* period (in milliseconds), the session is ended (RDY goes high) and processing continues as normal. This allows the system to continue and keep reference values up to date even if the master is not responsive. However, the corresponding data will be missed/lost. The default I²C timeout period is set to 200 ms and can be set to a maximum of 250 ms. The *I²C Communication Timeout* is measured from the start of the communications window (RDY goes low).

Once communication between the master and the IQS318 has begun (START condition on I²C lines), the I²C communication timeout is disabled leaving the watchdog timer in control. For more information on the behaviour of the device under these conditions see Section 6.10.

7.13 Terminate Communication

A standard I²C STOP will close the current communication window.

If the stop bit disable is set, the device will not respond to a standard I²C STOP. The communication window must be terminated using the end communications command (0xFF) shown in Figure 7.1.

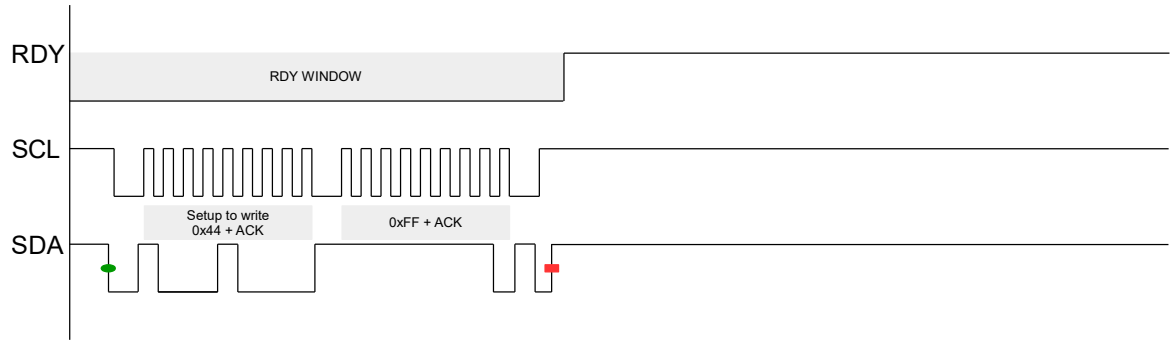


Figure 7.1: Force Stop Communication Sequence

7.14 Invalid Communications Return

The device will give an invalid communication response (0xEE) under the following conditions:

- The host is trying to read from a memory map register that does not exist.
- The host is trying to read from the device outside of a communication window (i.e. while RDY is high)

7.15 I²C Interface Types

The IQS318 has two *I²C Interface Types*, as described in the sections below.

7.15.1 I²C Streaming

I²C Streaming mode refers to constant data reporting at the relevant power mode sampling period specified in *Normal Power Mode Sampling Period*, and *Ultra Low Power Sampling Period*.

7.15.2 I²C Event Mode

The device can be set up to bypass the communication window when no activity is sensed (event mode). This is enabled to optimise communication and power consumption by only interrupting the master when activity on the sensor occurs. The communication will resume (RDY will indicate available data) if an enabled event occurs.

7.16 Event Mode Communication

Event mode can only be entered if the following requirements are met:

- *Reset Event* bit must be cleared by acknowledging the device reset condition by writing the *ACK Reset* bit to clear the System status flag.
- Events must be serviced by reading from the *System Status* to ensure all events flags are cleared otherwise continuous reporting (RDY interrupts) will persist after every conversion cycle similar to streaming mode

7.16.1 Events

Events can be individually enabled to trigger communication, bit definitions can be found in *System Status*.

Using the *Events Mask* register the following events can be enabled:

- ATI error
- ATI event
- Power event
- Touch event
- Proximity event

7.16.2 Force Communication

In streaming mode, the IQS318 I²C will provide Ready (RDY) windows at intervals specified by the power mode sampling period. Ideally, communication with the IQS318 should only be initiated in a RDY window. A communication request described in the figure below will force a RDY window to open. In event mode, RDY windows are only provided when an event is reported. A RDY window must be requested to write or read settings outside of this provided window. The minimum and maximum time between the communication request and the opening of a RDY window (t_{wait}) is typically less than 1.5 ms[i]. The communication request sequence is shown in Figure 7.2.

[i] Please contact Azoteq for an application specific value of t_{wait}

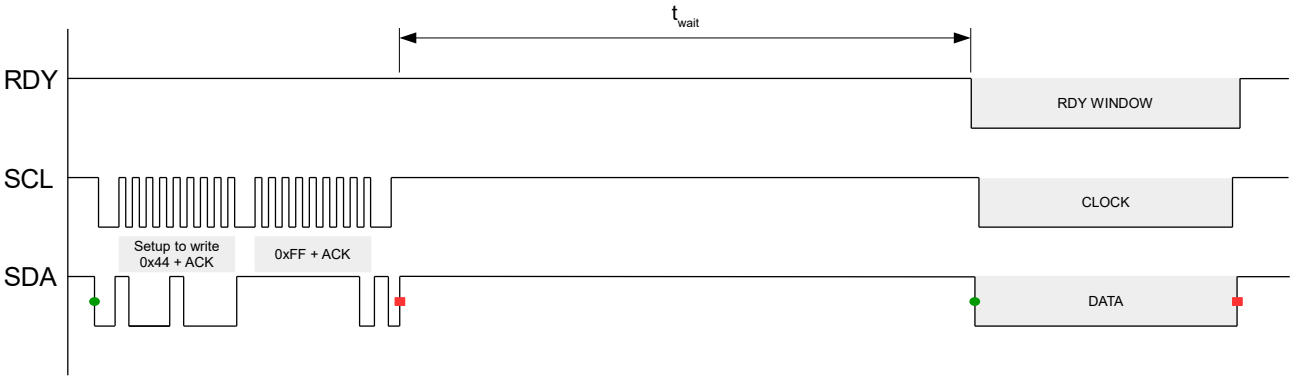


Figure 7.2: Force Communication Sequence

8 Memory Map Register Descriptions

Address	Data (16bit)	Notes
0x00 - 0x09	Version Details	See Appendix A.1
Read Only	**System Information**	
0x10	Reserved	
0x11	System Status	See Appendix A.2
0x12	Channel 0 Filtered Counts	16-bit value
0x13	Channel 0 LTA	
0x14	Channel 0 Delta	
Read/Write	**Sensor 0 Setup**	
0x20	Sensor Setup 0	See Appendix A.3
0x21	Sampling Setup	See Appendix A.4
0x22	Prox Control	See Appendix A.5
0x23	Sensor Setup 1	See Appendix A.6
0x24		See Appendix A.7
0x25		See Appendix A.8
0x26	ATI Setup	See Appendix A.9
0x27	ATI Base	16-bit value
0x28	ATI Multipliers Selection	See Appendix A.10
0x29	Compensation	See Appendix A.11
Read/Write	**Channel 0 Setup**	
0x40	Prox Settings	See Appendix A.12
0x41	Touch Settings	See Appendix A.13
Read/Write	**Normal Power Filter Betas**	
0x50	Normal Power Counts Filter Betas	16-bit value
0x51	Normal Power LTA Filter Betas	
0x52	Normal Power LTA Fast Filter Betas	
0x53	Normal Power Fast Filter Band	
Read/Write	**ULP Filter Betas**	
0x60	ULP Counts Filter Betas	16-bit value
0x61	ULP LTA Filter Betas	
0x62	ULP LTA Fast Filter Betas	
0x63	ULP Fast Filter Band	
Read/Write	**System Control**	
0x70	System Control	See Appendix A.14
0x71	Normal Power Mode Sampling Period	16-bit value (ms)
0x72	Ultra Low Power Sampling Period	
0x73	Power Mode Timeout	
Read/Write	**I²C Settings**	
0x80	I²C Transaction Timeout	Range: 2 - 250 (ms)
0x81	Event Timeouts	See Appendix A.15
0x82	Events Mask	See Appendix A.16

9 Ordering Information

9.1 Ordering Code

IQS318 zzz ppb

Table 9.1: Order Code Description

IC NAME			IQS318
CONFIGURATION	zzz	=	000 — I^2C inductive proximity/touch switch (DYCAL™ 2 UI)
			001 — Standalone inductive proximity/touch switch (DYCAL™ 2 UI)
			100 — I^2C inductive proximity/touch button
			101 — Standalone inductive proximity/touch button
			200 — I^2C inductive touch snap button
			201 — Reserved
			202 — Standalone inductive touch snap button
			510 — I^2C capacitive proximity/touch switch (DYCAL™ 2 UI)
			511 — Reserved
			512 — Standalone capacitive proximity/touch switch (DYCAL™ 2 UI)
			501 — Reserved
PACKAGE TYPE	pp	=	CS — WLCSP-11 package
			QF — QFN-20 package
			DN — DFN-12 package (On special order only[i])
BULK PACKAGING	b	=	R — WLCSP-11 Reel (3000pcs/reel)
			QFN-20 Reel (2000pcs/reel)
			DFN-12 Reel (6000pcs/reel)

9.2 Top Marking

9.2.1 WLCSP11 Package Marking

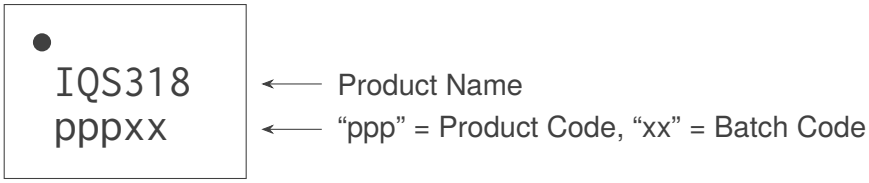


Figure 9.1: IQS318-WLCSP11 Package Top Marking

[i] Special order codes are subject to larger minimum order quantities, longer lead times and are non-cancelable, non-returnable.

9.2.2 DFN12 Package Marking Options

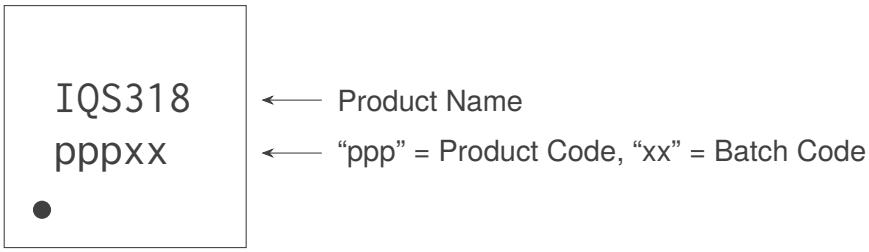


Figure 9.2: IQS318-DFN12 Package Top Marking

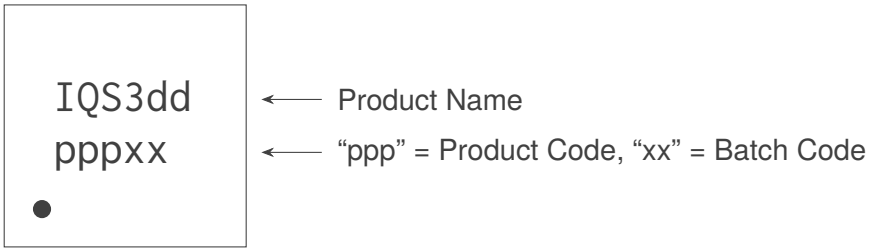


Figure 9.3: IQS3dd-DFN12 Package Top Marking

9.2.3 QFN20 Package Marking Options

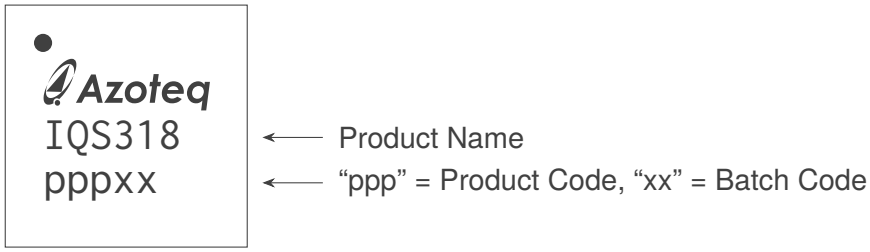


Figure 9.4: IQS318-QFN20 Package Top Marking

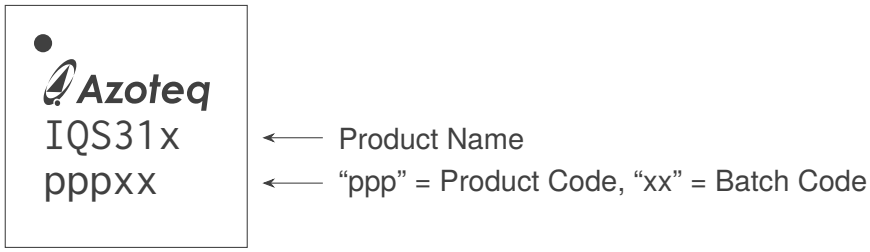


Figure 9.5: IQS31x-QFN20 Package Top Marking

10 Package Specification

10.1 Package Outline Description – WLCSP11

This package outline is specific to order codes ending in WLCSP.

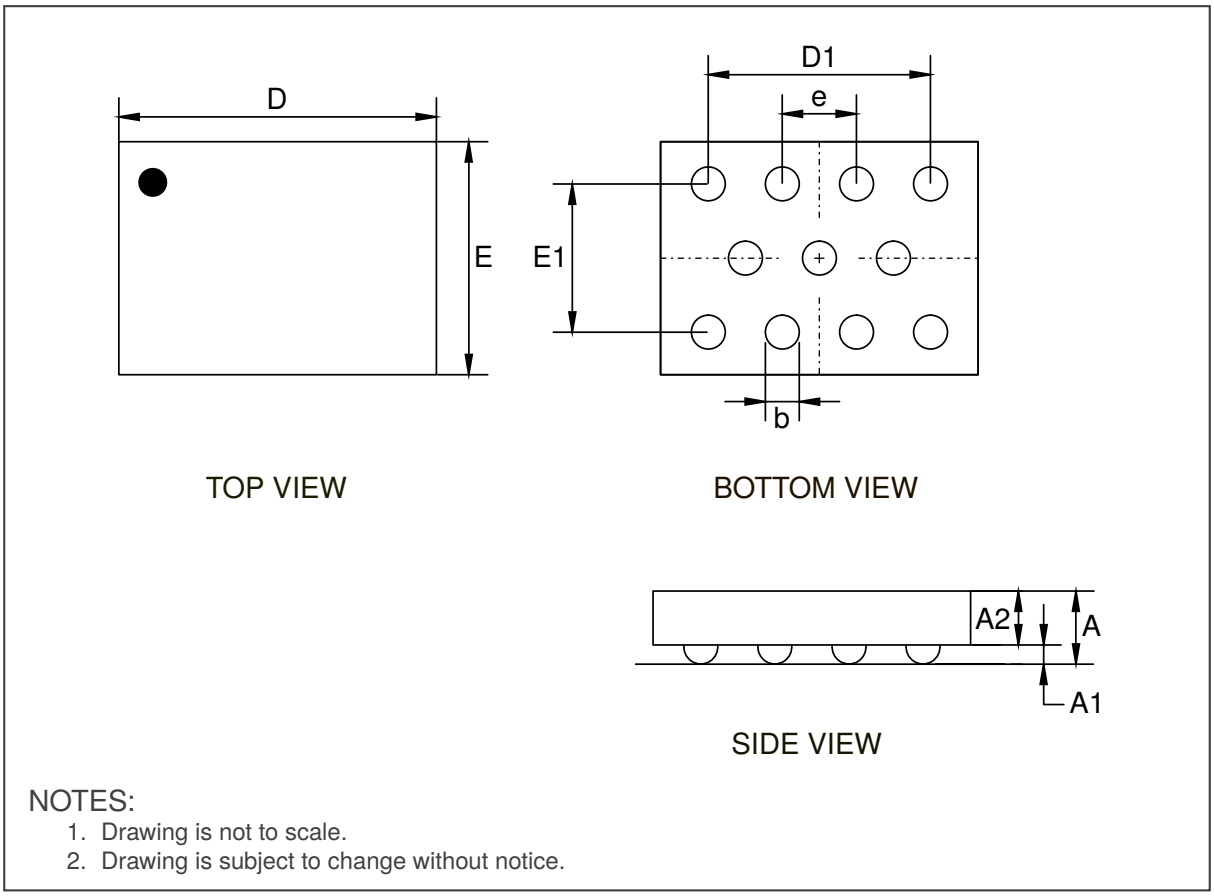
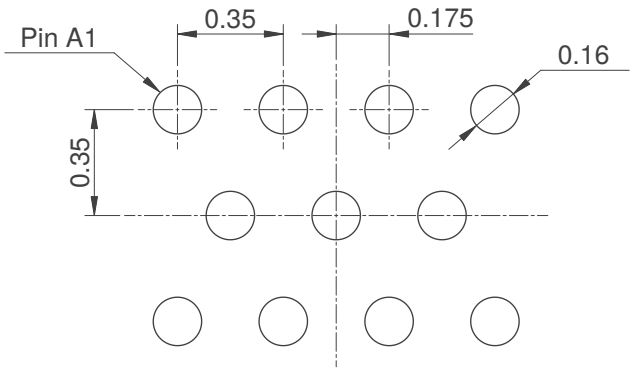


Figure 10.1: WLCSP11 (1.48x1.08) Package Outline Visual Description

Table 10.1: WLCSP11 (1.48x1.08) Package Outline Visual Description (mm)

Dimension	Min	Nom	Max
A	0.303	0.345	0.387
A1	0.076	0.090	0.104
A2	0.227	0.255	0.283
D	1.46	1.48	1.50
E	1.06	1.08	1.10
D1	1.05 BSC		
E1	0.700 BSC		
b	0.136	0.160	0.184
e	0.350 BSC		

10.2 Package Footprint Description – WLCSP11



NOTES:

1. Dimensions are expressed in millimeters.
2. Drawing is not to scale.
3. Drawing is subject to change without notice.
4. Final dimensions may vary due to manufacturing tolerance considerations.

Figure 10.2: WLCSP11 Recommended Footprint

10.3 Package Outline Description – DFN12

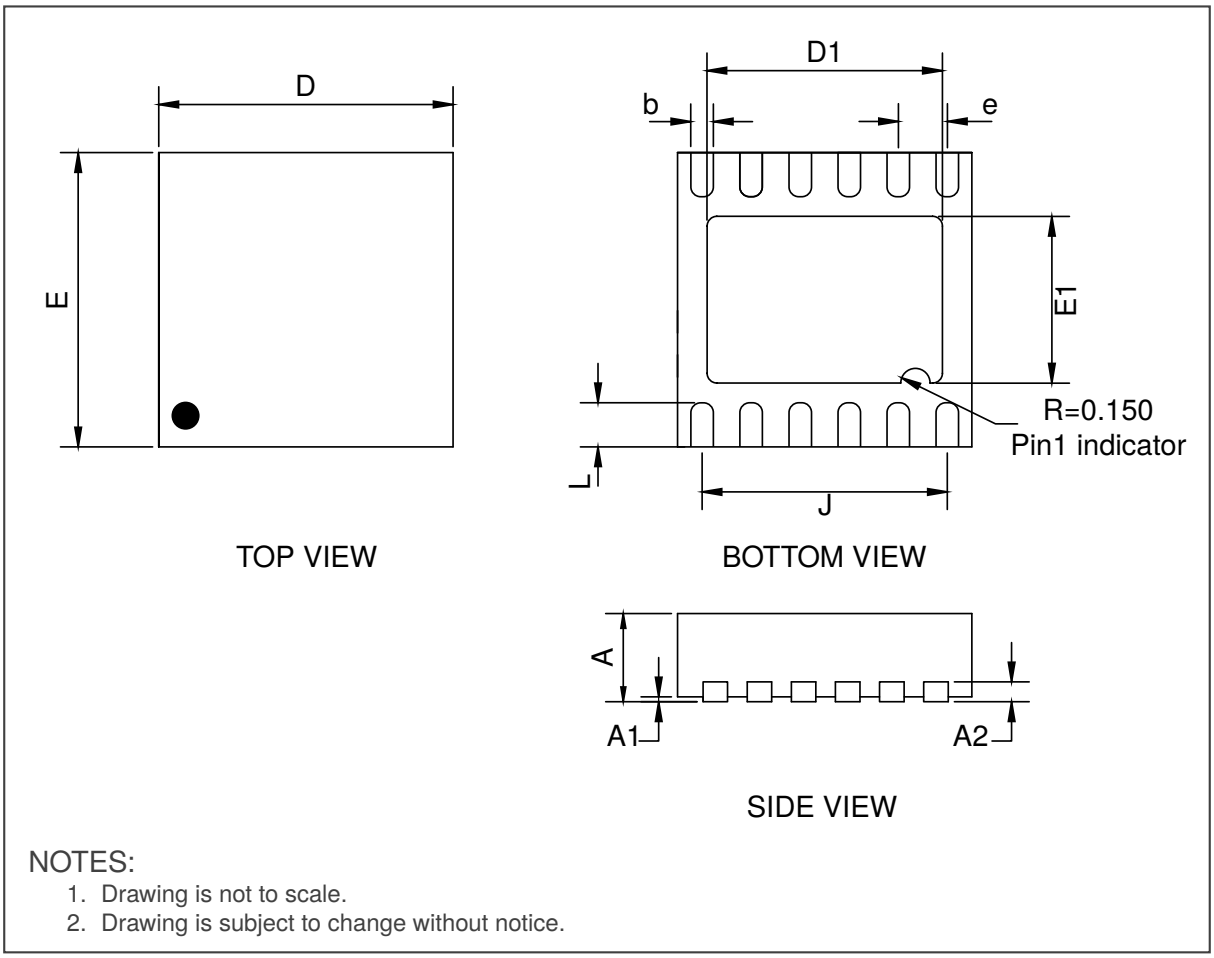
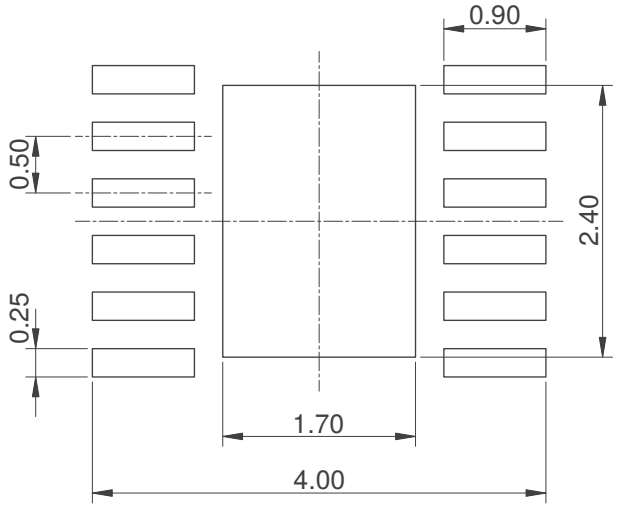


Figure 10.3: DFN (3x3)-12 Package Outline Visual Description

Table 10.2: DFN (3x3)-12 Package Outline Visual Description (mm)

Dimension	Min	Nom	Max
A	0.70	0.75	0.80
A1	0.00		0.05
A2		0.203 REF	
D	2.95	3.00	3.05
E	2.95	3.00	3.05
D1	2.35	2.40	2.45
E1	1.65	1.70	1.75
J		2.50 REF	
L	0.40	0.45	0.50
b	0.18	0.23	0.28
e		0.50 BSC	

10.4 Package Footprint Description – DFN12



NOTES:

1. Dimensions are expressed in millimeters.
2. Drawing is not to scale.
3. Drawing is subject to change without notice.
4. Final dimensions may vary due to manufacturing tolerance considerations.

Figure 10.4: DFN12 Recommended Footprint

10.5 Package Outline Description – QFN20 (QFR)

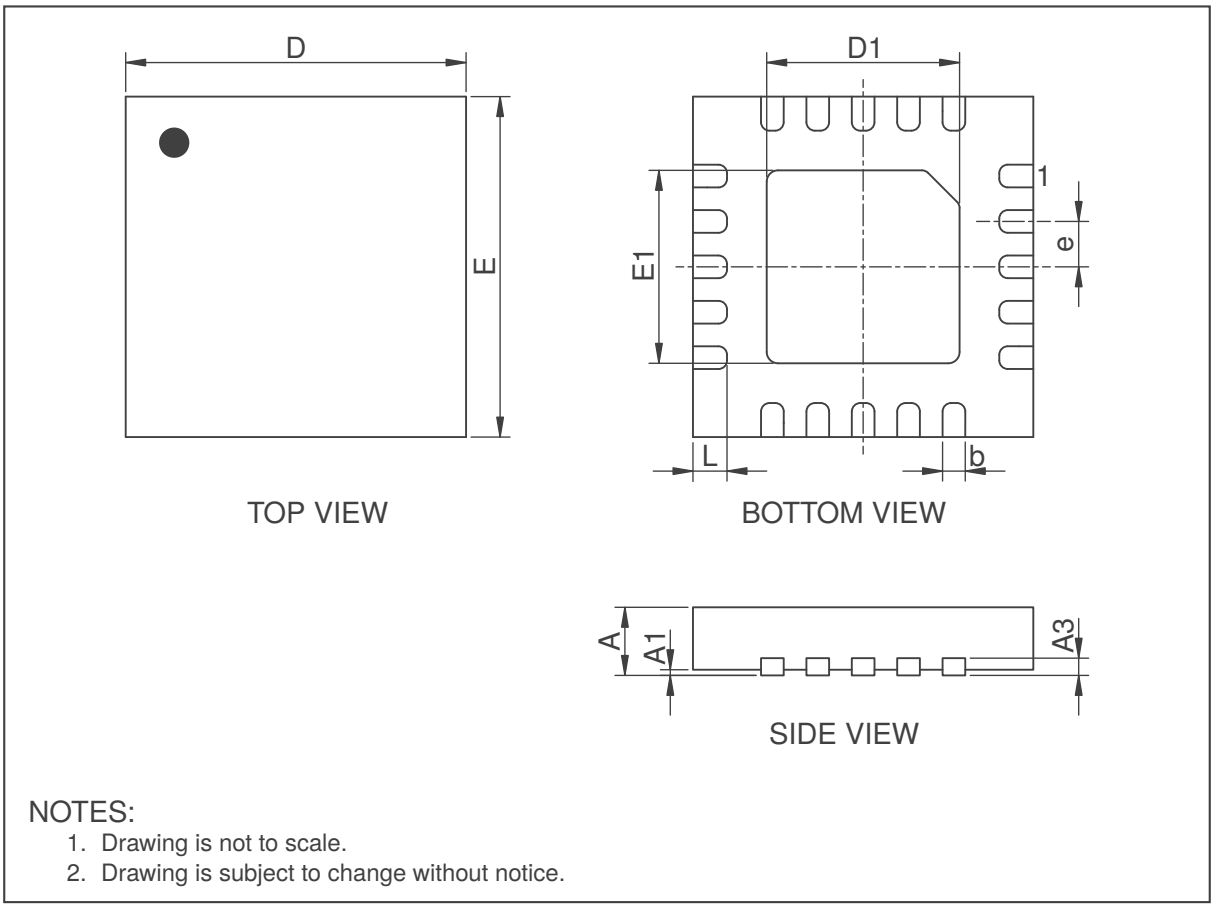
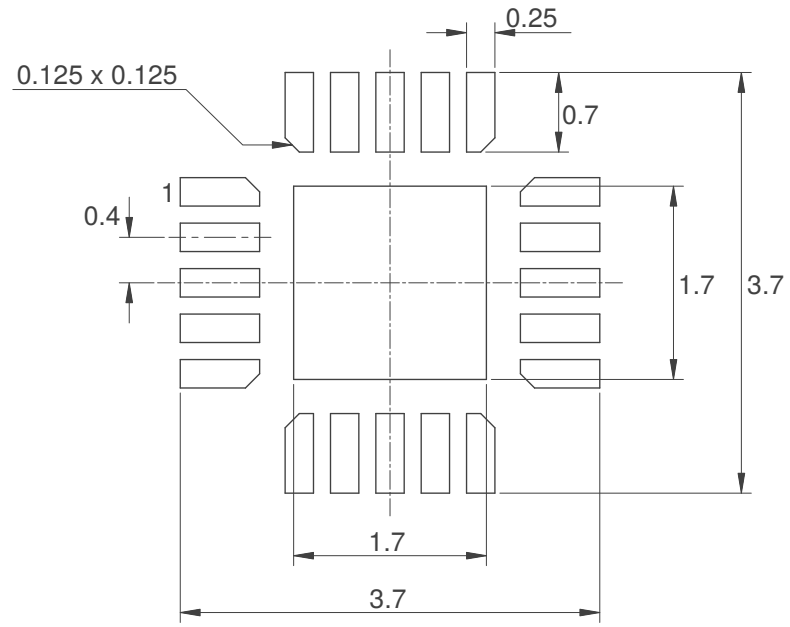


Figure 10.5: QFR (3x3)-20 Package Outline Visual Description

Table 10.3: QFR (3x3)-20 Package Outline Dimensions [mm]

Dimension	Min	Nom	Max
A	0.50	0.55	0.60
A1	0	0.02	0.05
A3		0.152 REF	
b	0.15	0.20	0.25
D	2.95	3.00	3.05
E	2.95	3.00	3.05
D1	1.60	1.70	1.80
E1	1.60	1.70	1.80
e		0.40 BSC	
L	0.25	0.30	0.35

10.6 Package Footprint Description – QFN20

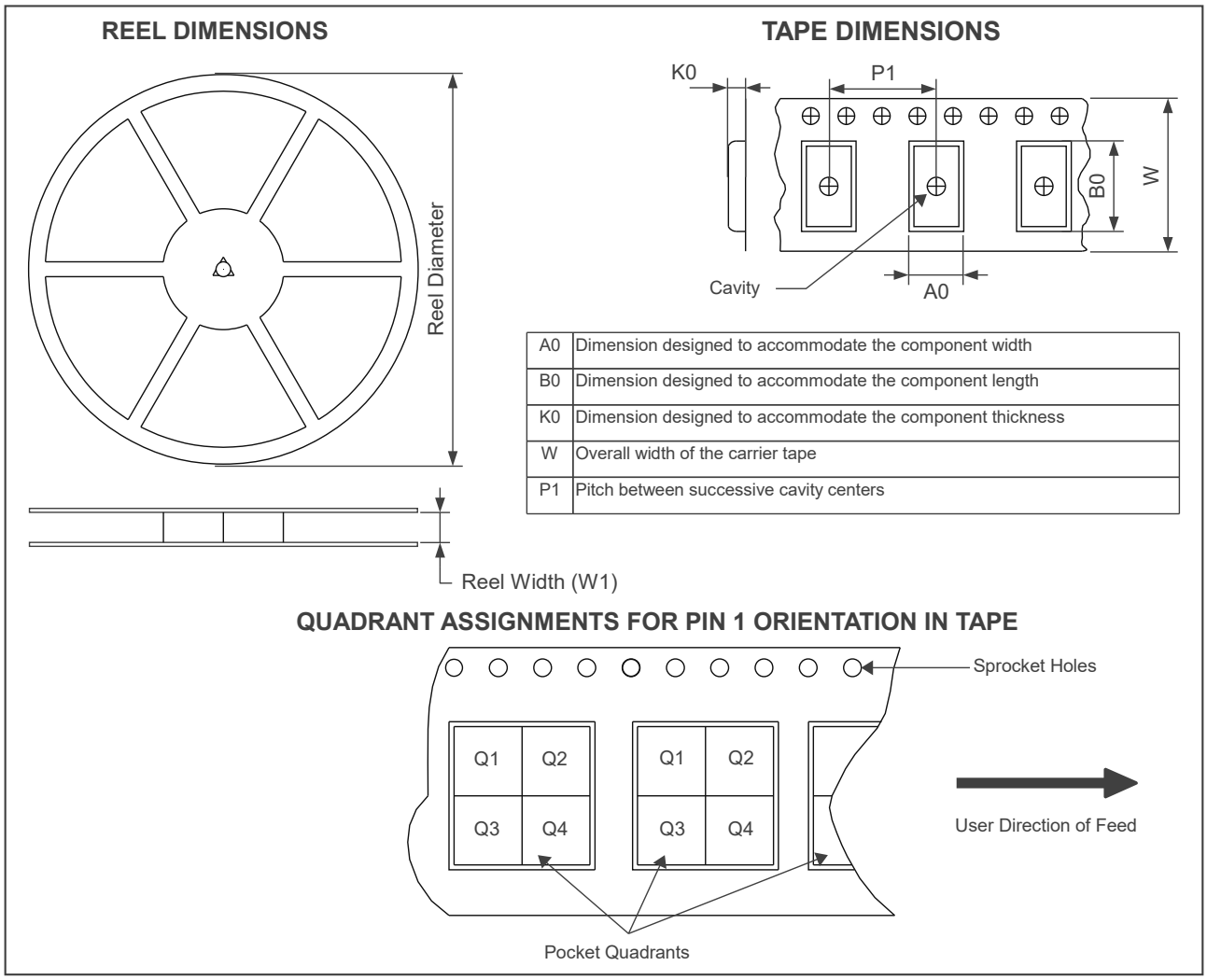


NOTES:

1. Dimensions are expressed in millimeters.
2. Drawing is not to scale.
3. Drawing is subject to change without notice.
4. Final dimensions may vary due to manufacturing tolerance considerations.

Figure 10.6: QFN20 Recommended Footprint

10.7 Tape and Reel Specifications



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

Figure 10.7: Tape and Reel Specification

Table 10.4: Tape and reel Specifications

Package Type	Pins	Reel Diameter (mm)	Reel Width (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
WLCSP11	11	179	8.4	1.35	1.75	0.5	4	8	Q2
DFN12	12	330	12.4	3.3	3.3	1.1	8	12	Q1
QFN20	20	180	12.4	3.3	3.3	0.8	8	12	Q2

A Memory Map Descriptions

A.1 Version Information (0x00 – 0x09)

Address	Category	Name	IQS318-xxx				
			000 / 001	100 / 101	200 / 201[i] / 202	501	510 / 511[ii] / 512
0x00	Version Information	Product Number	1863	1492	2101	1864	1864
0x01		Major Version	1	1	1	1	1
0x02		Minor Version	1	1	0	1	2
0x03		Reserved					
0x04							
0x05 - 0x09		Reserved					

A.2 System Status (0x11)

Bit	15	14	13	12	11	10	9	8
Description	Current Power Mode		ATI Active	Sampling Period	Threshold / Tx Frequency	Sensitivity	CH0 Touch	CH0 Prox

Bit	7	6	5	4	3	2	1	0
Description	Reset Event	ATI Error	ATI Event	Power Event	Direction	Output	Touch Event	Prox Event

- Bit 15-14: **Current Power Mode**
  - 00: Normal Power
  - 01: Ultra Low Power
- Bit 13: **ATI Active**
  - 0: ATI not active
  - 1: ATI active
- Bit 9: **CH0 Prox**
  - 0: CH0 not in Prox
  - 1: CH0 in Prox
- Bit 8: **CH0 Touch**
  - 0: CH0 not in Touch
  - 1: CH0 in Touch
- Bit 7: **Reset Event**
  - 0: No Reset Event occurred
  - 1: Reset Event occurred
- Bit 6: **ATI Error**
  - 0: No ATI Error occurred
  - 1: ATI Error occurred
- Bit 5: **ATI Event**
  - 0: No ATI Event occurred
  - 1: ATI Event occurred
- Bit 4: **Power Event**
  - 0: No Power Event occurred
  - 1: Power Event occurred
- Bit 3: **Touch Direction**[iii]
  - 0: Down
  - 1: Up
- Bit 2: **Output**
  - 0: Output low
  - 1: Output high
- Bit 1: **Touch Event**

[i] The IQS318-201 order code is not recommended for new designs.
[ii] The IQS318-511 order code is not recommended for new designs.
[iii] See Section 6.7.3 for more details.

- 0: No Touch Event occurred
- 1: Touch Event occurred

- Bit 0: **Prox Event**
  - 0: No Prox Event occurred
  - 1: Prox Event occurred

- **Note:** The default settings for channel sensitivity, sampling period, proximity and touch event timeout are given in Section 6.9.2.

A.3 Sensor Setup 0 (0x20)

Bit	15	14	13	12	11	10	9	8
Description	Reserved	CalCap Rx	CalCap Tx	Reserved	Reserved	Reserved	Rx1	Rx0/Tx0

Bit	7	6	5	4	3	2	1	0
Description	Reserved	Reserved	F_{OSC} Tx Frequency	Vbias	Invert	Dual Direct	Linearise Counts	Enable Channel

- Bit 14-11: **Reserved**
  - Set to '0'
- Bit 9: **Rx1**
  - 0: Pin disabled
  - 1: Pin enabled
- Bit 8: **Rx0/Tx0**
  - 0: Pin disabled
  - 1: Pin enabled
- Bit 5: **F_{OSC} Tx Frequency**[iv]
  - 0: Do not Tx at F_{OSC}
  - 1: Tx at F_{OSC}
- Bit 4: **Vbias**
  - Set to '0'
- Bit 3: **Invert**
  - 0: Do not invert channel logic
  - 1: Invert channel logic
- Bit 2: **Dual Direction Threshold Option**[v]
  - 0: Single direction thresholds
  - 1: Dual direction thresholds
- Bit 1: **Linearise Counts**
  - 0: Do not Linearise counts
  - 1: Linearise counts
- Bit 0: **Enable Channel**
  - 0: Channel disabled
  - 1: Channel enabled

A.4 Sampling Setup (0x21)

Bit	15	14	13	12	11	10	9	8
Description	Conversion Frequency Period							

Bit	7	6	5	4	3	2	1	0
Description	Conversion Frequency Fraction							

- Bit 15-8: **Conversion Frequency Period**

[iv] See Section 6.9.3 for more details.
[v] The default state is true for the IQS318-0xx and IQS318-5xx with DYCAL™ 2 UI. The default state is false for the remaining order codes (IQS318-1xx and IQS318-2xx).

- Range: 0 - 127

- Bit 7-0: **Conversion Frequency Fraction**
  - $256 * \frac{f_{xfer}}{f_{osc}}$
  - Range: 0 - 255
- **Note:** If dead-time is enabled (self-capacitive sensing) or disabled (inductive sensing), the following values for the conversion frequency periods (at fraction = 127) will result in the corresponding charge transfer frequencies (in MHz):

Fraction	Period	Dead-time disabled	Dead-time enabled
		F_{osc} = 14MHz	F_{osc} = 14MHz
127	0	7.00	4.66
	1	3.50	2.80
	2	2.33	2.00
	3	1.75	1.55
	5	1.15	1.07
	8	0.77	0.74
	17	3.88	0.38

A.5 Prox Control (0x22)

Bit	15	14	13	12	11	10	9	8
Description	Reserved	0v5 Discharge	Reserved	Cs Size	Reserved	Reserved	Reserved	

Bit	7	6	5	4	3	2	1	0
Description	Max Counts		PXS Mode					

- Bit 15: **Reserved**
  - Set to ‘0’
- Bit 14: **0v5 Discharge**
  - 0: Disabled
  - 1: Enabled
- Bit 13: **Reserved**
  - Set to ‘0’
- Bit 12: **Cs Size**
  - 0: Use 40pF Cs
  - 1: Use 80pF Cs (Default selection)
- Bit 11: **Reserved**
  - Set to ‘0’
- Bit 10: **Reserved**
  - Set to ‘0’
- Bit 9-8: **Reserved**
  - Set to ‘00’
- Bit 7-6: **Max Counts**
  - 00: 1023
  - 01: 2047
  - 10: 4095
  - 11: 16384
- Bit 5-0: **PXS Mode**
  - 0x3D: Inductive
  - 0x10: Self-Capacitance

A.6 Sensor Setup 1 (0x23)

Bit	15	14	13	12	11	10	9	8
Description	Reserved	Reserved	Reserved	Reserved	Calibration Cap Select	Rx2	Rx1	Rx0

Bit	7	6	5	4	3	2	1	0
Description	Reserved	Dead Time Enable	Reserved	Reserved	Reserved		Reserved	

- Bit 15: **Reserved**
  - Set to '0'
- Bit 14: **Reserved**
  - Set to '0'
- Bit 13: **Reserved**
  - Set to '0'
- Bit 11: **Calibration Capacitor Select**
  - Set to '0'
- Bit 10: **Reserved**
  - Set to '0'
- Bit 9: **Reserved**
  - Set to '0'
- Bit 8: **Reserved**
  - Set to '1'
- Bit 7: **Reserved**
  - Set to '1'
- Bit 6: **Dead Time Enable**
  - 0: Dead Time Disabled
  - 1: Dead Time Enabled
- Bit 4: **Reserved**
  - Set to '0'
- Bit 3-2: **Reserved**
  - Set to '10'
- Bit 1-0: **Reserved**
  - Set to '11'

A.7 Sensor Setup 2 (0x24)

Bit	15	14	13	12	11	10	9	8
Description	Wav Pattern 1				Wav Pattern 0			

Bit	7	6	5	4	3	2	1	0
Description	Reserved				Inactive Rxs			

- Bit 15-12: **Wav Pattern 1**
  - Set to '0x00'
- Bit 11-8: **Wav Pattern 0**
  - Set to '0x0B'
- Bit 3-0: **Inactive Rxs**
  - Selects state of Cx's when not in use
  - 0x00: Floating
  - 0x05: Bias voltage
  - 0x0A: VSS
  - 0x0F: VREG

A.8 Sensor Setup 3 (0x25)

Bit	15	14	13	12	11	10	9	8
Description	Reserved				Reserved			

Bit	7	6	5	4	3	2	1	0
Description	Wav Pattern Select							

- Bit 7-0: **Wav Pattern Select**
  - Set to '0x00'

A.9 ATI Setup (0x26)

Bit	15	14	13	12	11	10	9	8
Description	ATI Resolution Factor							

Bit	7	6	5	4	3	2	1	0
Description	ATI Resolution Factor				ATI Band	ATI Mode		

- Bit 15-4: **ATI Resolution Factor**
  - ATI Target = Actual ATI Base x $\frac{\text{ATI Resolution Factor}}{16}$
- Bit 3: **ATI Band**
  - 0: Small ATI Band = ($\frac{1}{16}$ x ATI Target)
  - 1: Large ATI Band = ($\frac{1}{8}$ x ATI Target)
- Bit 2-0: **ATI Mode**
  - 000: Disabled
  - 001: Compensation Only
  - 010: ATI from Compensation Divider
  - 011: ATI from Fine Fractional Divider
  - 100: Full

A.10 ATI Multipliers And Dividers (0x28)

Bit	15	14	13	12	11	10	9	8
Description	Fine Fractional Multiplier		Fine Fractional Divider					Coarse Fractional Multiplier

Bit	7	6	5	4	3	2	1	0
Description	Coarse Fractional Multiplier			Coarse Fractional Divider				

A.11 Compensation (0x29)

Bit	15	14	13	12	11	10	9	8
Description	Compensation Divider					Reserved	Compensation	

Bit	7	6	5	4	3	2	1	0
Description	Compensation							

- **Note:** The information in Tables A.10 and A.11 are for debugging only. These are determined by the ATI algorithm and "ATI mode: Full" is recommended for application use.

A.12 Prox Settings (0x40)

Bit	15	14	13	12	11	10	9	8
Description	Prox Debounce Exit				Prox Debounce Enter			

Bit	7	6	5	4	3	2	1	0
Description	Prox Threshold							

- Bit 15-12: **Prox Debounce Exit**
  - 0000: Prox Debounce disabled
  - 4-bit value
- Bit 11-8: **Prox Debounce Enter**
  - 0000: Prox Debounce disabled
  - 4-bit value
- Bit 7-0: **Prox Threshold**
  - 8 bit value
  - $\text{value} \times \frac{\text{LTA}}{256}$

A.13 Touch Settings (0x41)

Bit	15	14	13	12	11	10	9	8
Description	Touch Hysteresis							

Bit	7	6	5	4	3	2	1	0
Description	Touch Threshold							

- Bit 15-8: **Touch Hysteresis**
  - 8 bit value
- Bit 7-0: **Touch Threshold**
  - 8 bit value

A.14 System Control (0x70)

Bit	15	14	13	12	11	10	9	8
Description	Reserved							

Bit	7	6	5	4	3	2	1	0
Description	Interface Selection		Power Mode		Reseed	Re-ATI	Soft Reset	ACK Reset

- Bits 7-6: **Interface Selection**
  - 00: Standalone
  - 01: I^2C Streaming
  - 10: Reserved
  - 11: I^2C Events
- Bit 5-4: **Power Mode**
  - 00: Normal Power Mode
  - 01: Ultra Low Power Mode
  - 10: Automatic
- Bit 3: **Reseed**
  - 0: No Reseed
  - 1: Trigger Reseed
- Bit 2: **Re-ATI**
  - 0: No Re-ATI
  - 1: Trigger Re-ATI
- Bit 1: **Soft Reset**
  - 0: No Soft Reset

- 1: Trigger Soft Reset

- Bit 0: **ACK Reset**
  - 0: No ACK Reset
  - 1: ACK Reset

A.15 Event Timeouts (0x81)

Bit	15	14	13	12	11	10	9	8
Description	Touch Event Timeout							

Bit	7	6	5	4	3	2	1	0
Description	Prox Event Timeout							

- Bits 15-8: **Touch Event Timeout**
  - Touch Event Timeout = 8 bit value * 500ms. The default touch event timeout values for the different order codes are given in Section 6.9.2.
- Bits 7-0: **Prox Event Timeout**
  - Prox Event Timeout = 8 bit value * 500ms. The default prox event timeout values for the different order codes are given in Section 6.9.2.

- **Note:** In order codes 0xx and 5xx when in touch and this timer expires, the touch output will not be cleared, but with this time-out the signal will be adapted for optimal detection of a release event.

A.16 Events Mask (0x82)

Bit	15	14	13	12	11	10	9	8
Description	Reserved							

Bit	7	6	5	4	3	2	1	0
Description	Reset Event Mask	ATI Error Mask	ATI Event Mask	Power Event Mask	Reserved		Touch Event Mask	Prox Event Mask

- Bit 7: **Reset Event Mask**
  - 0: Reset Event disabled
  - 1: Reset Event enabled
- Bit 6: **ATI Error Mask**
  - 0: ATI Error disabled
  - 1: ATI Error enabled
- Bit 5: **ATI Event Mask**
  - 0: ATI Event disabled
  - 1: ATI Event enabled
- Bit 4: **Power Event Mask**
  - 0: Power Event disabled
  - 1: Power Event enabled
- Bit 1: **Touch Event Mask**
  - 0: Touch Event disabled
  - 1: Touch Event enabled
- Bit 0: **Prox Event Mask**
  - 0: Prox Event disabled
  - 1: Prox Event enabled

B Inductive Resonant Tank Design Guideline

Described below are the steps to design the inductive resonant tank with a certain resonant frequency.

1. For a given inductance L and Tx frequency, f_{tx}, calculate the capacitor C_{calc} for a resonant frequency $f_{tx} \times 1.05$ (±5 % tolerance on f_{tx}).
2. Select a capacitor C_{sel} such that $(C_{sel} \times 1.10) \leq C_{calc}$, assuming a ±10 % tolerance on the capacitor.
3. For better safety, 10 pF can be removed from parallel tank capacitors less than or equal to 200 pF, to account for the Tx and Rx pad capacitance.

B.1 Example

› Given $L = 1.1\,\text{mH}$, use f_{tx} from $f_{osc} = 14\,\text{MHz}$. Determine C_{calc}:

$$f_{resonant} = 14\,\text{MHz} + 5\,\% = 14.7\,\text{MHz}$$

$$14.7 \times 10^6 = \frac{1}{2\pi\sqrt{1.1 \times 10^{-6} \times C_{calc}}}$$

$$C_{calc} = 106.56\,\text{pF}$$

› Next, determine C_{sel} such that $(1.1 \times C_{sel}) \leq C_{calc}$:

$$C_{sel} \leq 96.87\,\text{pF}$$

› Subtract $10\,\text{pF}$ from C_{sel}, since $C_{sel} < 200\,\text{pF}$:

$$C_{sel} = 86.87\,\text{pF}$$

› Using ±10 % tolerance on C_{sel} and $f_{resonant} = \frac{1}{2\pi\sqrt{L \times C}} = \frac{1}{2\pi\sqrt{1.1x10^{-6} \times C_{sel}}}$, we get the results below and the summary of the result shown in Figure B.1.

$$C_{sel} = 86.87\,\text{pF} \quad \Rightarrow \quad f_{resonant} = 16.28\,\text{MHz}$$
$$C_{sel} = 86.87\,\text{pF} + 10\,\% \quad \Rightarrow \quad f_{resonant} = 15.52\,\text{MHz}$$
$$C_{sel} = 86.87\,\text{pF} - 10\,\% \quad \Rightarrow \quad f_{resonant} = 17.16\,\text{MHz}$$

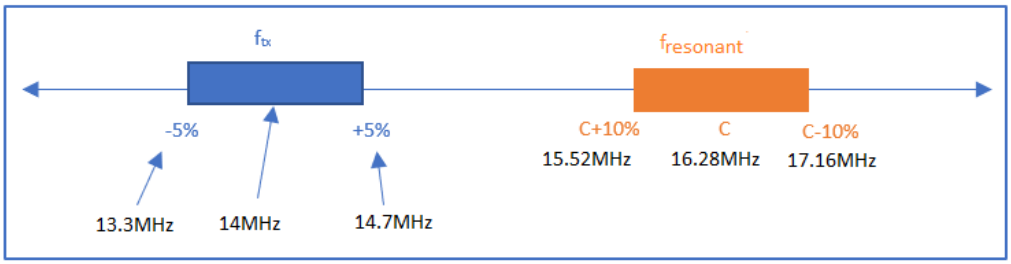


Figure B.1: Inductive Resonant Tank Design

Note: The following order codes start-up with a coil excitation frequency of 14 MHz:

- IQS318-001
- IQS318-101
- IQS318-201[i]
- IQS318-202

I²C order code options allow for the use of various excitation frequencies.

[i] The IQS318-201 order code is not recommended for new designs.

C Revision History

Release	Date	Changes
v 0.1	April/2023	Initial release
v 1.0	May/2023	Added the description of the IQS318 I²C order codes: IQS318-000, IQS318-100, and IQS318-500. Updated current measurements also included
v 1.1	August/2023	Introduced the IQS318-510/512 order codes, updated I²C address, added 14MHz inductive resonant tank design, and other minor updates
v 1.2	November/2023	Introduced the IQS318-200/201 order codes, updated I²C address, added f_{xfer} input selection, and other minor updates
v 1.3	January/2024	Added the QFN20 package and updated the pin attribute table and ordering information
v 1.4	March/2024	DFN12 Package Marking Updated
v 1.5	May/2024	QFN20 Schematic added and pin description table updated.
v 1.6	August/2024	Updated pinout to indicate I2C SDA and SCL pins. Updated top marking drawings. Updated I2C memory map table formatting. Introduction of IQS318-202 and IQS318-512.
v 1.7	February/2025	Updated the Order Code section.

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