Mercury+ XU9 SoC Module

User Manual

Purpose

The purpose of this document is to present the characteristics of Mercury+ XU9 SoC module to the user, and to provide the user with a comprehensive guide to understanding and using the Mercury+ XU9 SoC module.

Summary

This document first gives an overview of the Mercury+ XU9 SoC module followed by a detailed description of its features and configuration options. In addition, references to other useful documents are included.

Product Information	Code	Name
Product	ME-XU9	Mercury+ XU9 SoC Module

Document Information	Reference	Version	Date
Reference / Version / Date	D-0000-463-001	06	22-May-2025

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Document History

Version	Date	Author	Comment
06	22-May-2025	MGOS	Updated block diagram. Change the current rating of VCC_PSINT.
05	30-Jan-2024	MGOS	Updated for revision 3.0 modules: improved terminology, content, and layout for better readability and consistency
04	05-Sep-2022	TKAU	Updated for revision 2.1 modules: added information on discontinuation of support for power converter switching frequency synchronization, changes on base board descriptions
03	16-Feb-2021	DIUN	Added information on Mercury heat sinks, added Mercury+ ST1 to accessories section, added information on FPGA fuses and warranty, on differential I/Os, on voltage monitoring outputs, removed 15 Gbps limitation on MGTs due to Hirose connector, other style updates
02	15-Nov-2019	MMOS	Added information on revision 1 and 2 modules, other minor corrections
01	03-Jun-2019	DIUN	Version 01, preliminary

Table of Contents

Table of Contents **3**

1 Overview **6**
1.1 General . . . 6
1.1.1 Introduction . . . 6
1.1.2 Warranty . . . 6
1.1.3 RoHS . . . 6
1.1.4 Disposal and WEEE . . . 6
1.1.5 Safety Recommendations and Warnings . . . 7
1.1.6 Electrostatic Discharge . . . 7
1.1.7 Electromagnetic Compatibility . . . 7
1.2 Features . . . 7
1.3 Deliverables . . . 8
1.3.1 Reference Design . . . 8
1.3.2 Enclustra Build Environment . . . 8
1.3.3 Petalinux BSP . . . 9
1.4 Accessories . . . 9
1.4.1 Enclustra Heat Sink . . . 9
1.4.2 Mercury+ PE1 Base Board . . . 9
1.4.3 Mercury+ PE3 Base Board . . . 9
1.4.4 Mercury+ ST1 Base Board . . . 9
1.5 AMD Tool Support . . . 10

2 Module Description **11**
2.1 Block Diagram . . . 11
2.2 Module Configuration and Product Models . . . 12
2.3 EN-Numbers and Product Models . . . 13
2.4 Top and Bottom Views . . . 15
2.4.1 Top View . . . 15
2.4.2 Bottom View . . . 15
2.5 Top and Bottom Assembly Drawings . . . 16
2.5.1 Top Assembly Drawing . . . 16
2.5.2 Bottom Assembly Drawing . . . 16
2.6 Module Footprint and Mechanical Data . . . 17
2.7 Module Connector . . . 18
2.8 User I/O . . . 19
2.8.1 Pinout . . . 19
2.8.2 I/O Pin Exceptions . . . 20
2.8.3 Differential I/Os . . . 21
2.8.4 I/O Banks . . . 22
2.8.5 VCC_IO Usage . . . 23
2.8.6 Signal Terminations . . . 24
2.8.7 Multiplexed I/O (MIO) Pins . . . 25
2.8.8 Analog Inputs . . . 26
2.9 Multi-Gigabit Transceiver (MGT) . . . 27
2.10 Power . . . 29
2.10.1 Power Generation Overview . . . 29
2.10.2 Power Enable/Power Good . . . 30
2.10.3 Voltage Supply Inputs . . . 31
2.10.4 Voltage Supply Outputs . . . 32
2.10.5 Power Consumption . . . 32
2.10.6 Heat Dissipation . . . 32
2.10.7 Voltage Monitoring . . . 33

2.11 Clock Generation . . . 34
2.12 Reset . . . 35
2.13 LEDs . . . 35
2.14 DDR4 SDRAM (PS) . . . 36
2.14.1 DDR4 SDRAM Characteristics . . . 36
2.14.2 Signal Description . . . 36
2.14.3 Termination . . . 36
2.14.4 Parameters . . . 37
2.15 DDR4 SDRAM (PL) . . . 37
2.15.1 DDR4 SDRAM Characteristics . . . 38
2.15.2 Signal Description . . . 38
2.15.3 Termination . . . 38
2.15.4 Parameters . . . 38
2.16 QSPI Flash . . . 39
2.16.1 QSPI Flash Characteristics . . . 39
2.16.2 Signal Description . . . 39
2.16.3 Configuration . . . 39
2.17 eMMC Flash . . . 40
2.17.1 eMMC Flash Characteristics . . . 40
2.17.2 Signal Description . . . 40
2.18 SD Card . . . 40
2.19 Dual Gigabit Ethernet . . . 40
2.19.1 Ethernet PHY Characteristics . . . 40
2.19.2 Signal Description . . . 40
2.19.3 External Connectivity . . . 41
2.19.4 MDIO Address . . . 41
2.19.5 PHY Configuration . . . 41
2.19.6 RGMII Delays Configuration . . . 42
2.20 USB 2.0 . . . 42
2.20.1 USB PHY Characteristics . . . 42
2.20.2 Signal Description . . . 43
2.21 USB 3.0 . . . 43
2.22 DisplayPort . . . 44
2.23 Real-Time Clock (RTC) . . . 44
2.24 Secure EEPROM . . . 44
2.24.1 EEPROM Characteristics . . . 45

3 Device Configuration 46
3.1 Configuration Signals . . . 46
3.2 Module Connector C Detection . . . 46
3.3 Pull-Up During Configuration . . . 47
3.4 Power-on Reset Delay Override . . . 48
3.5 Boot Mode . . . 48
3.6 JTAG . . . 48
3.6.1 JTAG on Module Connector . . . 49
3.6.2 External Connectivity . . . 49
3.6.3 JTAG Boot Mode . . . 49
3.7 eMMC Boot Mode . . . 50
3.8 QSPI Boot Mode . . . 50
3.9 SD Card Boot Mode . . . 50
3.10 eMMC Flash Programming . . . 51
3.11 QSPI Flash Programming via JTAG . . . 51
3.12 QSPI Flash Programming from an External SPI Master . . . 51
3.13 Enclustra Module Configuration Tool . . . 52

4 I2C Communication 53

4.1 Overview . . . 53
4.2 Signal Description . . . 53
4.3 I2C Address Map . . . 53
4.4 Secure EEPROM . . . 54
4.4.1 Memory Map . . . 54

5 Operating Conditions **57**
5.1 Absolute Maximum Ratings . . . 57
5.2 Recommended Operating Conditions . . . 58

6 Ordering and Support **59**
6.1 Ordering . . . 59
6.2 Support . . . 59

List of Figures **60**

List of Tables **60**

References **62**

1 Overview

1.1 General

1.1.1 Introduction

The Mercury+ XU9 SoC module combines the AMD Zynq® UltraScale+ MPSoC (Multiprocessor System-on-Chip) device with fast DDR4 ECC SDRAM, eMMC flash, quad SPI flash, dual Gigabit Ethernet PHY, and dual USB 3.0. This module forms a complete and powerful embedded processing system, available in extended and industrial temperature ranges.

The use of the Mercury+ XU9 SoC module, in contrast to building a custom MPSoC hardware, significantly reduces development effort and redesign risk and improves time-to-market for the embedded system. Together with Mercury+ base boards, the Mercury+ XU9 SoC module allows the user to quickly build a system prototype and start with application development.

The Enclustra Build Environment [16] is available for the Mercury+ XU9 SoC module. This build system allows the user to quickly set up and run Linux on any Enclustra SoC module. It allows the user to choose the desired target and download all the required binaries, such as bitstream and FSBL (First Stage Boot Loader). It downloads and compiles all required software, such as U-Boot, Linux, and BusyBox based root file system.

1.1.2 Warranty

Refer to the General Business Conditions, available on the Enclustra website [1].

> **Tip**
>
> The warranty of Enclustra modules is void if the FPGA's one-time programmable eFuses are blown. This operation is irreversible. Enclustra cannot test the module in case of a product return.

NOTICE

Data loss or unusable product

The fuses of the FPGA can be blown to activate the user-defined Advanced Encryption Standard (AES). After blowing the fuses, only content encrypted using a specific key can be loaded on the FPGA. Your key is unique and cannot be retrieved in case of loss.

- Keep your key in a secure location.

1.1.3 RoHS

The Mercury+ XU9 SoC module is designed and produced according to the Restriction of Hazardous Substances (RoHS) Directives 2011/65/EU (RoHS 2) and 2015/863/EU (RoHS 3).

1.1.4 Disposal and WEEE

The Mercury+ XU9 SoC module must be properly disposed of at the end of its life.

The Mercury+ XU9 SoC module is not subject to the Waste Electrical and Electronic Equipment (WEEE) Directive (2012/19/EU).

1.1.5 Safety Recommendations and Warnings

Mercury+ modules are not designed to be "ready for operation" for the end-user. These can only be used in combination with suitable base boards. Proper configuration of the hardware before usage is required.

Ensure that the power supply is disconnected from the board before inserting or removing the Mercury+ XU9 SoC module, connecting interfaces, or connecting jumpers.

Touching the capacitors of the DC-DC converters can lead to voltage peaks and permanent damage; over-voltage on power or signal lines can also cause permanent damage to the module.

1.1.6 Electrostatic Discharge

Electronic boards are sensitive to electrostatic discharge (ESD). Ensure that the product is handled with care and only in an ESD-protected environment.

1.1.7 Electromagnetic Compatibility

The Mercury+ XU9 SoC module is a Class A product (as defined in IEC 61000-3-2 standard) and is not intended for use in domestic environments. The product may cause electromagnetic interference, for which appropriate measures must be taken.

1.2 Features

- AMD Zynq® UltraScale+™ MPSoC
  - XCZU4CG/XCZU4EV/XCZU5EV/XCZU7EV device
  - FBVB900 package
  - AMD 16nm FinFET+ FPGA fabric
  - Dual-/Quad-core ARM® Cortex™-A53 MPCore™ up to 1.333 GHz
  - Dual-core ARM® Cortex™-R5 MPCore™ up to 533 MHz
  - Mali-400 MP2 GPU (not for CG variants)
  - H.264 / H.265 Video Codec (only for EV variants)
  - 14 ARM peripheral I/Os (SPI, SDIO, CAN, I2C, UART)
  - 78 FPGA I/Os (single-ended, differential or analog)
    - 30 HP I/Os
      - 26 I/Os at 1.2 V (fixed voltage)
      - 4 I/Os up to 3.3 V (routed via level shifters)
    - 48 HD I/Os (up to 3.3 V)
  - 20 MGT transceivers
    - 16 GTH transceivers
      - Speed grade 1 devices: 12.5 Gbit/s
      - Other devices: 16.375 Gbit/s
    - 4 GTR transceivers @ 6 Gbit/s
  - 10 reference clock inputs
    - 8 GTH reference clock inputs
    - 2 GTR reference clock inputs
  - PCIe Gen3 ×16 (AMD built-in PCIe integrated block using GTH lanes)
  - PCIe Gen2 ×4 (AMD built-in PCIe hard block using GTR lanes)
- Up to 4 GB DDR4 SDRAM with ECC in the PS
- Up to 2 GB DDR4 SDRAM in the PL
- 64 MB quad SPI flash
- 16 GB eMMC flash
- 2 × Gigabit Ethernet PHYs (one PHY shared with one of the USB PHYs)
- 2 × USB 2.0 PHYs

    - PHY0 configured as host or device
    - PHY1 configured as host (shared with one of the Gigabit Ethernet PHYs)
- USB 3.0 (AMD built-in USB 3.0 hard block using GTR lanes)
- CAN, UART, SPI, I2C, SDIO/MMC
- Real-time clock
- Form factor: 74 × 54 mm
- 5 to 15 V supply voltage

1.3 Deliverables

- Mercury+ XU9 SoC module
- Mercury+ XU9 SoC module documentation, available via download:
    - Mercury+ XU9 SoC Module User Manual (this document)
    - Mercury+ XU9 SoC Module Reference Design [2]
    - Mercury+ XU9 SoC Module IO Net Length Excel Sheet [3]
    - Mercury+ XU9 SoC Module FPGA Pinout Excel Sheet [4]
    - Mercury+ XU9 SoC Module User Schematic (PDF) [5]
    - Mercury+ XU9 SoC Module Known Issues and Changes [6]
    - Mercury+ XU9 SoC Module Footprint (Altium, Eagle, Orcad and PADS) [7]
    - Mercury+ XU9 SoC Module 3D Model (PDF) [8]
    - Mercury+ XU9 SoC Module 3D Model (STEP) [9]
    - Mercury Mars Module Pin Connection Guidelines [10]
    - Mercury Master Pinout [11]
    - Mercury Heat Sink Kits User Manual [20]
- Additional resources, available online:
    - Enclustra Build Environment [16] (Linux build environment; refer to Section 1.3.2 for details)
    - Enclustra Build Environment How-To Guide [17]
    - Petalinux BSP and Documentation [18]
    - Enclustra I2C Application Note [21]

1.3.1 Reference Design

The Mercury+ XU9 SoC Module Reference Design [2] features an example configuration for the Zynq UltraScale+ MPSoC device, together with an example top level HDL file for the user logic.

A number of software applications are available for the reference design, that show how to initialize the peripheral controllers and how to access the external devices. Pre-compiled binaries are included in the archive, so that the user can easily check that the hardware is functional.

> **Tip**
>
> To get notified about updates to the Mercury+ XU9 SoC Module Reference Design, turn on the notifications from the Enclustra Github page [2].

1.3.2 Enclustra Build Environment

The Enclustra Build Environment (EBE) [16] enables the user to quickly set up and run Linux on any Enclustra SoC module or system board. It allows the user to choose the desired target, and download all the required binaries, such as bitstream and FSBL. It downloads and compiles all required software, such as U-Boot, Linux, and BusyBox based root file system.

The Enclustra Build Environment features a graphical user interface (GUI) and a command line interface (CLI) that facilitates the automatic build flow.

The Enclustra Build Environment How-To Guide [17] describes in more detail how to use the EBE to customize the provided software for the user application. The document provides information on the configuration options for U-boot, Linux kernel and Buildroot, debugging possibilities for Linux applications, customization of device trees and integration of existing or new kernel drivers.

1.3.3 Petalinux BSP

The Enclustra Petalinux BSPs enable the user to quickly set up a Petalinux project and to run Linux on the Enclustra SoC module or system board.

The documentation [18] describes the build process in detail and allows a user without Petalinux knowledge to build and run the desired design on the target hardware.

1.4 Accessories

1.4.1 Enclustra Heat Sink

For Mercury modules an Enclustra heat sink is available for purchase along with the product. Refer to Section 2.10.6 for further information on the available cooling options.

1.4.2 Mercury+ PE1 Base Board

The Mercury+ PE1 [13] is a versatile PCIe® x4 base board equipped with a multitude of I/O interfaces for use with the Mercury/Mercury+ family of FPGA and SoC modules, providing a head start for building custom FPGA and SoC based hardware systems.

It is compatible with a multitude of FMC boards from different suppliers to use in data acquisition systems, motor control, display and camera interfaces, software defined radio and more. The board is equally well suited for rapid prototyping and for building FPGA systems without designing custom hardware.

The available features depend on the Mercury module type and on the selected base board variant.

> **Tip**
>
> The pinout assignments (pin types and I/O voltage levels) on the module connectors B and C affects the FMC interfaces. The compatibility of the Mercury+ XU9 SoC module with the Mercury+ PE1 base board is therefore limited. Compare the FMC card pinout in detail with the Enclustra Mercury Master Pinout and with the module and base board schematic.

1.4.3 Mercury+ PE3 Base Board

The Mercury+ PE3 [15] is a versatile PCIe® x8 base board equipped with a multitude of I/O interfaces for use with the Mercury/Mercury+ family of FPGA and SoC modules, providing a head start for building custom FPGA and SoC based hardware systems.

This high performance base board provides a versatile set of I/O connectivity options, specialized for high-speed communication and video applications, including SFP+, QSFP+, HDMI, USB Type-C and Firefly. The board is equally well suited for rapid prototyping and for building FPGA systems without designing custom hardware.

The available features depend on the Mercury module type and on the selected base board variant.

1.4.4 Mercury+ ST1 Base Board

The Mercury+ ST1 board [14] is a compact, low-cost base board equipped with a multitude of I/O interfaces for use with the Mercury/Mercury+ family of FPGA and SoC modules.

It provides a versatile set of I/O connectivity options, specialized for video applications, including DisplayPort, HDMI, MIPI, and SFP+. The board is equally well suited for rapid prototyping and for building FPGA systems without designing custom hardware.

The available features depend on the Mercury module type and on the selected base board variant.

1.5 AMD Tool Support

The MPSoC devices assembled on the Mercury+ XU9 SoC module are supported by the Vivado ML Standard Edition software, which is available free of charge. Contact AMD for further information.

2 Module Description

2.1 Block Diagram

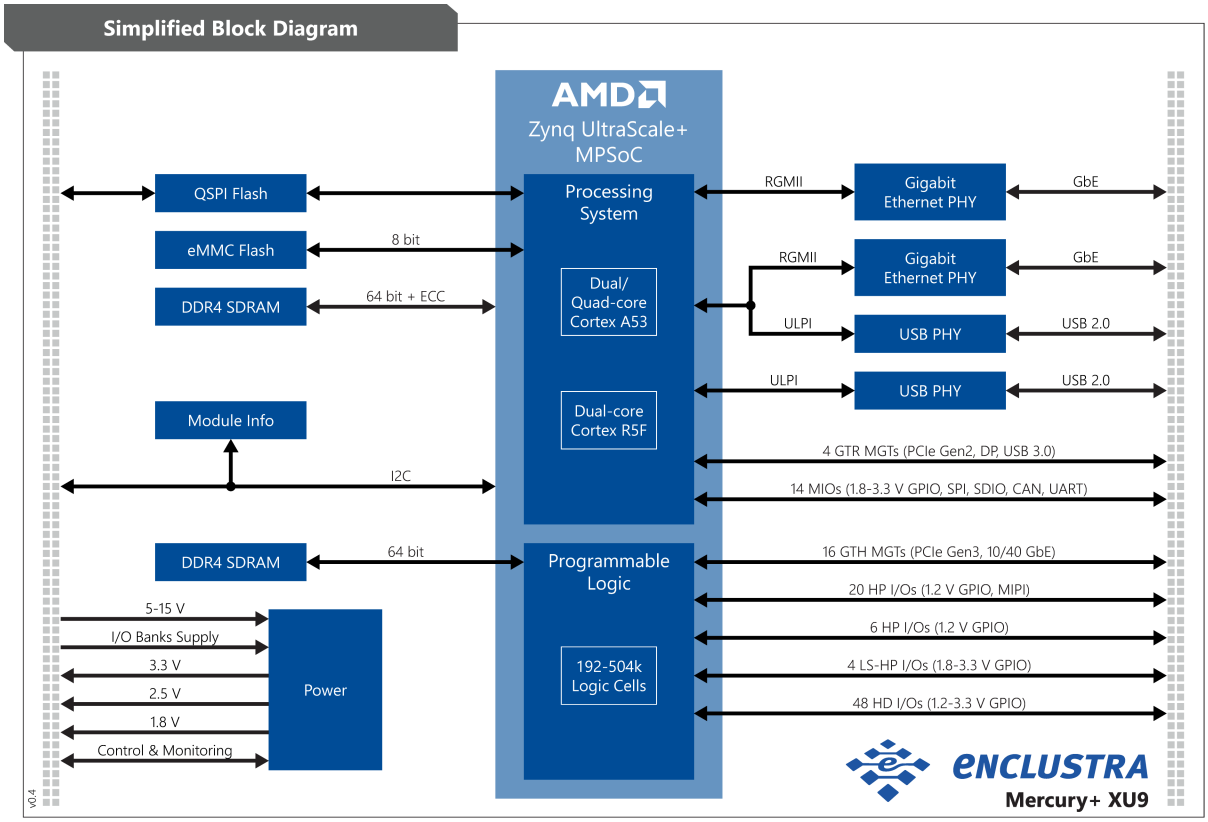

Figure 1: Hardware Block Diagram

The main component of the Mercury+ XU9 SoC module is the AMD Zynq UltraScale+ MPSoC device. All available I/O pins (which are not routed to on-board peripherals) are connected to the Mercury+ module connector, making 92 regular user I/Os available to the user. Further, twenty MGT pairs are available on the module connector, making possible the implementation of several high-speed protocols such as PCIe Gen3 ×16, PCIe Gen2 ×4 and USB 3.0 (simultaneous usage of all the interfaces is limited to the available hardware resources i.e. number of transceivers and lane mapping).

The MPSoC device can boot from the on-board QSPI flash, from the eMMC flash or from an external SD card. For development purposes, a JTAG interface is connected to Mercury module connector.

The available standard configurations include a 16 GB eMMC flash, a 64 MB quad SPI flash, up to 4 GB DDR4 SDRAM with ECC connected to the Processing System (PS) and up to 2 GB DDR4 SDRAM connected to the Programmable Logic (PL).

Further, the module is equipped with two Gigabit Ethernet PHYs and two USB 2.0 PHYs, making it ideal for communication applications.

A real-time clock is available on the AMD Zynq UltraScale+ MPSoC device.

On-board clock generation is based on a 33.33 MHz crystal oscillator and a 100 MHz LVDS oscillator providing a clock for the PL and a reference clock for the MGT GTR transceivers. In addition to this, another

27 MHz oscillator delivers a reference clock for the MGT GTR transceivers.

The module's internal supply voltages are generated from a single input supply of 5 - 15 V DC. Some of these voltages are available on the Mercury module connectors to supply circuits on the base board.

Five LEDs are connected to the MPSoC pins for status signaling.

2.2 Module Configuration and Product Models

Table 1 describes the available standard module configurations. The product model indicates the module type and main features. Figure 2 describes the fields within the product model. Custom configurations are available. Contact Enclustra for more information.

Product Model	MPSoC[1]	DDR4 ECC SDRAM (PS)	DDR4 SDRAM (PL)	Temperature Range
ME-XU9-4CG-1E-D11E[2]	XC**ZU4**CG-1FBVB900E	2 GB	2 GB	0 to +85°C
ME-XU9-5EV-1I-D12E-L11[2]	XC**ZU5**EV-1FBVB900I	4 GB	2 GB	-40 to +85°C
ME-XU9-7EV-2I-D12E-L11	XC**ZU7**EV-2FBVB900I	4 GB	2 GB	-40 to +85°C
ME-XU9-7EV-2E-D13E[2]	XC**ZU7**EV-2FBVB900I	8 GB	8 GB	0 to +85°C
ME-XU9-7EG-2E-D11E-L13[2]	XC**ZU7**EV-2FBVB900I	2 GB	8 GB	0 to +85°C

Table 1: Standard Module Configurations

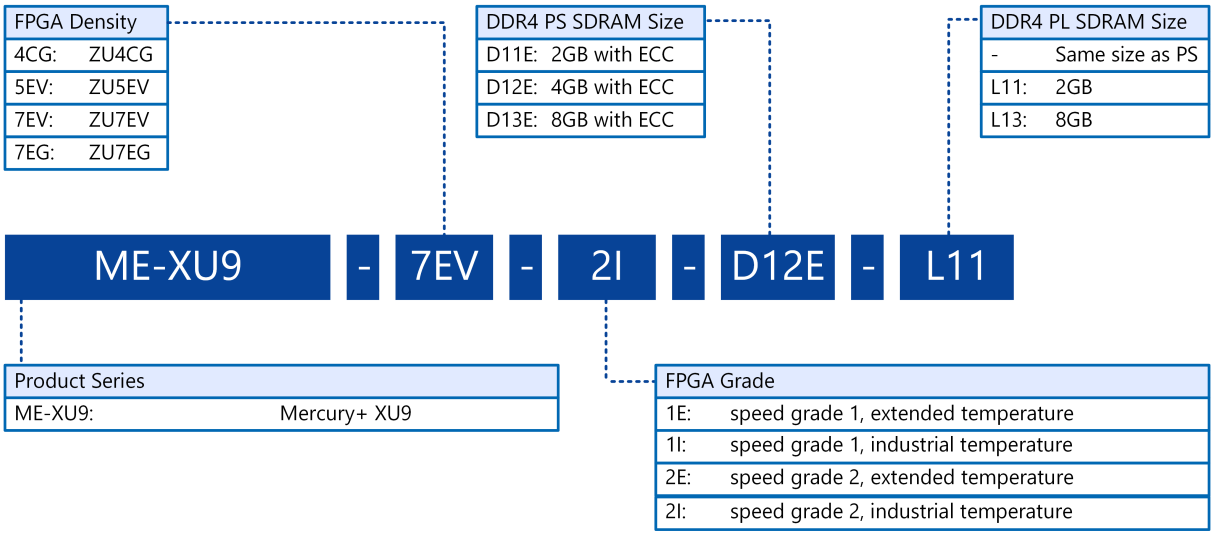

Figure 2: Product Model Fields

For the first revision modules or early access modules, the product model may not respect entirely this naming convention. Contact Enclustra for more information.

[1] The "device" is shown in bold.
[2] These product models are no longer available as standard products.

2.3 EN-Numbers and Product Models

Every product is uniquely labeled, showing the EN-number and serial number. An example is presented in Figure 3.

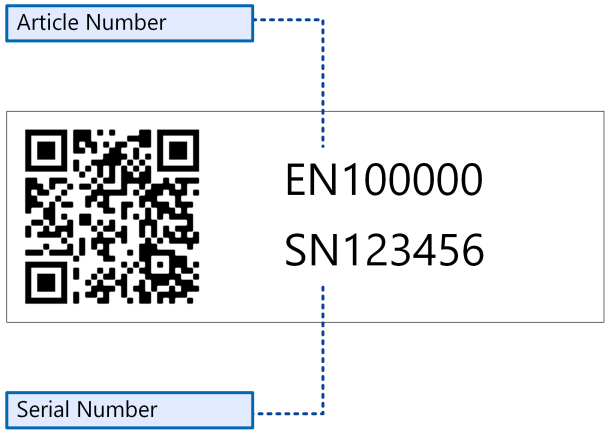

Figure 3: Product Label

The correspondence between EN-number and product model for each revision is shown in Table 2.

The known issues of the product and the changes between the revisions are described in the Mercury+ XU9 SoC Module Known Issues and Changes [6].

EN-Number	Product Model	Revision Number
EN105303	ME-XU9-7EV-2I-D12E-L11	R3.0
EN105302	ME-XU9-7EV-2E-D13E	R3.0
EN105301	ME-XU9-7EG-2E-D11E-L13	R3.0
EN105300	ME-XU9-5EV-1I-D12E-L11	R3.0
EN105299	ME-XU9-4CG-1E-D11E	R3.0
EN105166	ME-XU9-7EV-2I-D12E-L11	R2.1
EN105165	ME-XU9-7EV-2E-D13E	R2.1
EN105164	ME-XU9-7EG-2I-D11E-L13	R2.1
EN105163	ME-XU9-7EG-2E-D11E-L13	R2.1
EN105162	ME-XU9-5EV-1I-D12E-L11	R2.1
EN105161	ME-XU9-4CG-1E-D11E	R2.1
EN104681	ME-XU9-7EG-2E-D11E-L13	R2.0
EN104339	ME-XU9-7EG-2I-D11E-L13	R2.0
EN103349	ME-XU9-7EV-2E-D13E	R2.0
EN102682	ME-XU9-7EV-2I-D12E-L11	R2.0

Continued on next page...

EN-Number	Product Model	Revision Number
EN102680	ME-XU9-5EV-1I-D12E-L11	R2.0
EN102678	ME-XU9-4CG-1E-D11E	R2.0
EN102366	ME-XU9-7EV-2I-D12E-L11	R1.0
EN102364	ME-XU9-5EV-1I-D12E-L11	R1.0
EN102362	ME-XU9-4CG-1E-D11E	R1.0

Table 2: EN-Numbers and Product Models

2.4 Top and Bottom Views

Depending on the hardware revision and configuration, the module may look slightly different than shown in this document.

2.4.1 Top View

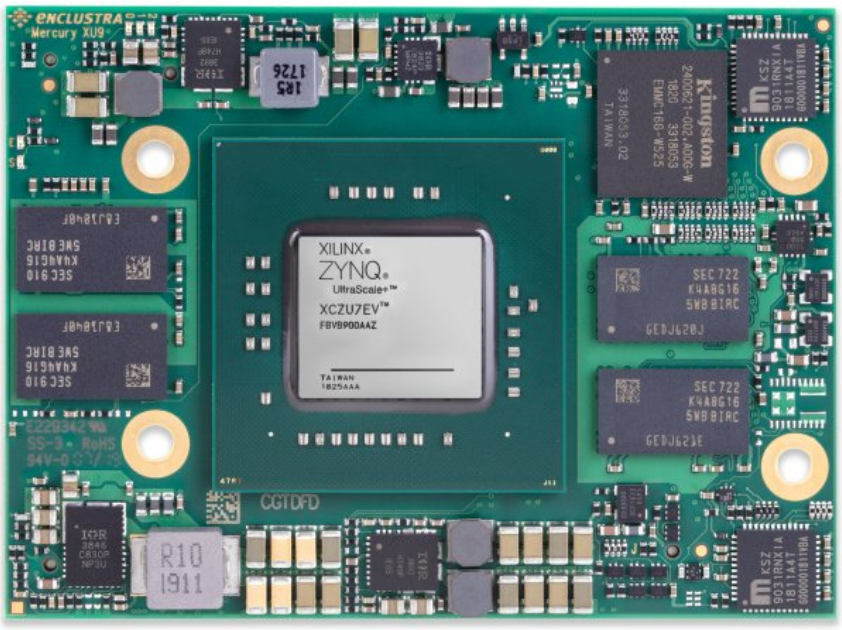

Figure 4: Module Top View

2.4.2 Bottom View

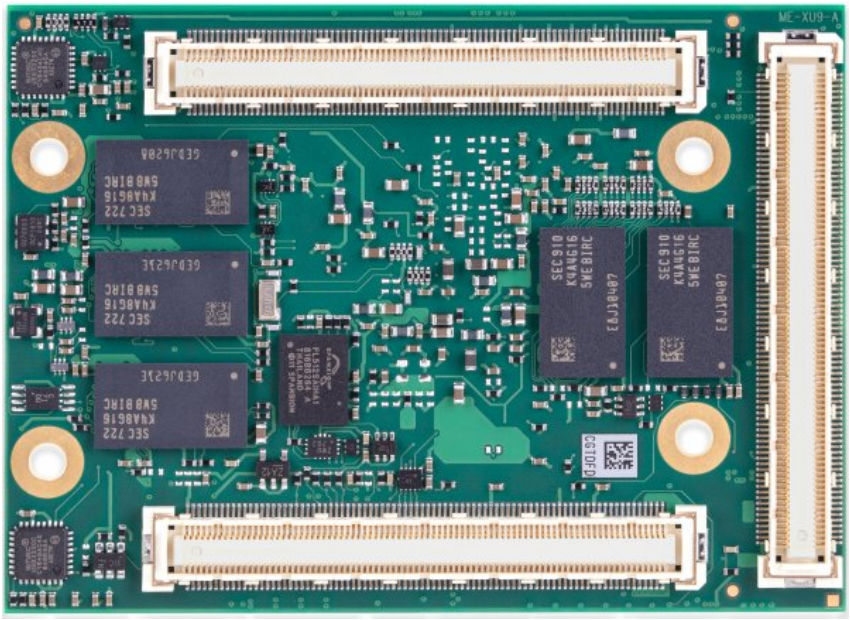

Figure 5: Module Bottom View

2.5 Top and Bottom Assembly Drawings

Depending on the hardware revision and configuration, the module may look slightly different than shown in this document.

2.5.1 Top Assembly Drawing

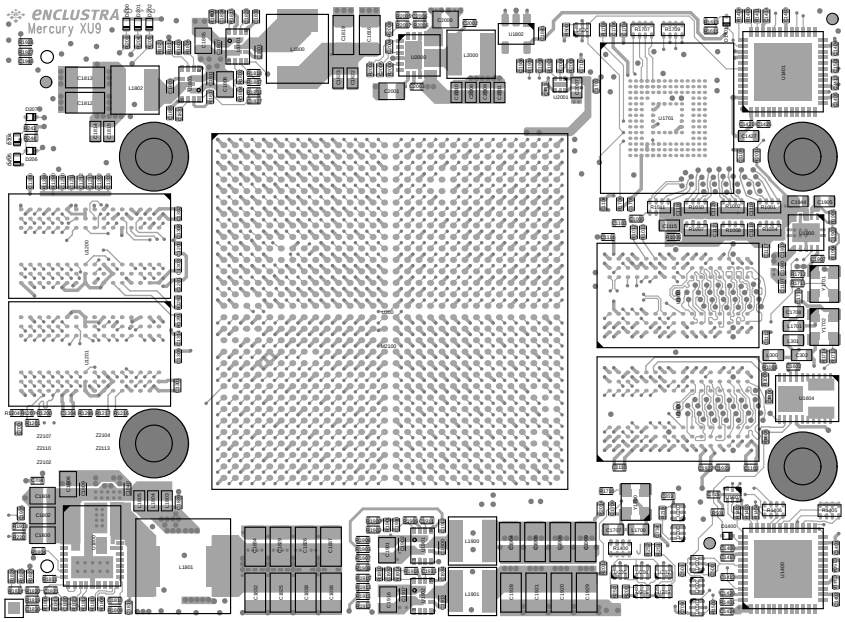

Figure 6: Module Top Assembly Drawing

2.5.2 Bottom Assembly Drawing

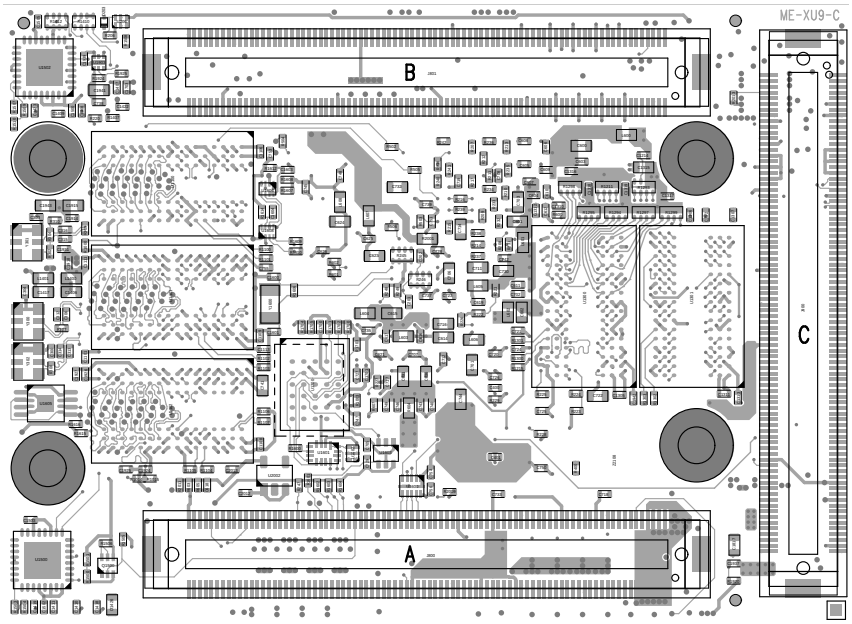

Figure 7: Module Bottom Assembly Drawing

2.6 Module Footprint and Mechanical Data

Figure 8 shows the dimensions of the module footprint on the base board.

Enclustra offers Mercury and Mercury+ modules of various geometries having widths of 56, 64, 65, 72 or 74 mm and having different topologies for the mounting holes. If different module types shall be fixed on the base board by screws, additional mounting holes may be required to accommodate different modules. The footprints of the module connectors for the base board design are available for different PCB design tools (Altium, PADS, Eagle, Orcad) [7] and include the required information on the module sizes and holes.

The maximum component height under the module is dependent on the connector type. Refer to Section 2.7 for detailed connector information.

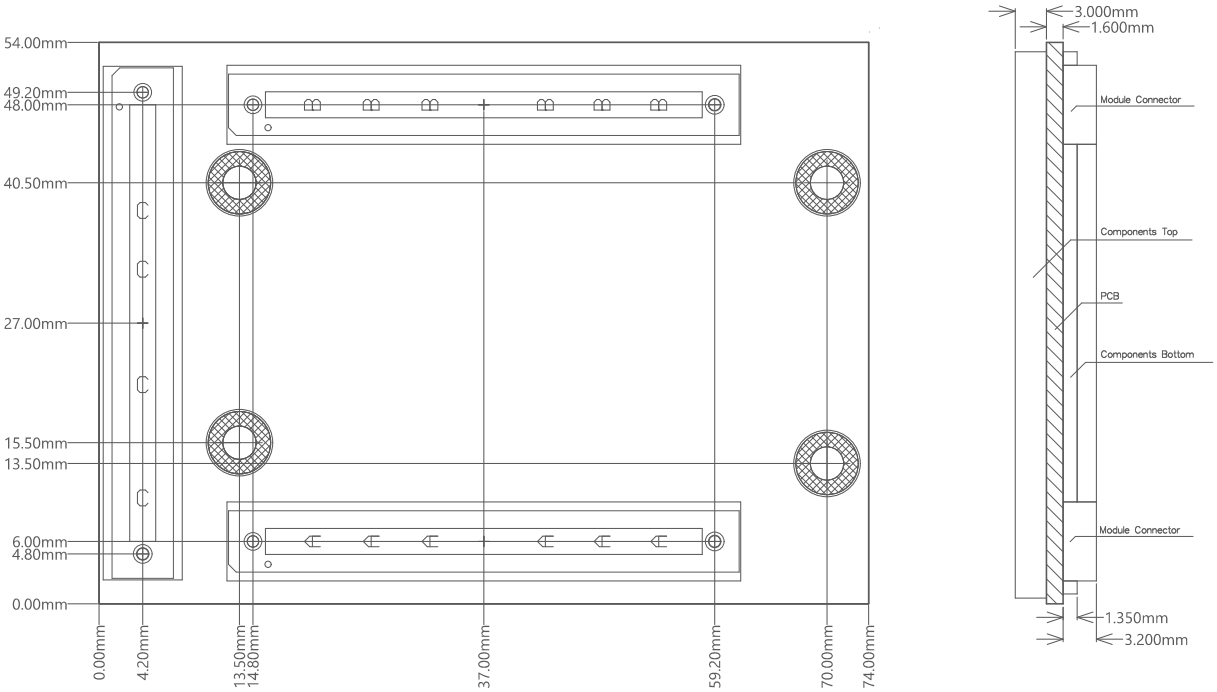

Figure 8: Model Footprint and Dimensions - Top View and Side View

Tip

A small golden square on the bottom left corner of Enclustra modules is provided as landmark. The same landmark is provided on the Enclustra base boards to help orient the module in the right direction when connecting it.

NOTICE

Damage to the connectors

The connectors of the module and the base board can be damaged if the connectors are not properly aligned during installation.

- Align the connectors carefully before applying force on the module.
- Do not use excessive force to latch the module into the connectors on the base board.

NOTICE

Damage to the device when applying power

The Mercury module could physically be mounted the wrong way around on the base board. The module and the base board can be damaged if the device is powered on while it is connected the wrong way around.

- Ensure that the mounting holes on the base board are aligned with the mounting holes of the module.

Table 3 describes the mechanical characteristics of the Mercury+ XU9 SoC module. A 3D model (PDF) and a STEP 3D model are available [8], [9].

Parameter	Value
Size	74 × 54 mm
Component height top	3.00 mm
Component height bottom	1.35 mm
Weight	32 g

Table 3: Mechanical Data

2.7 Module Connector

Three Hirose FX10 168-pin 0.5 mm pitch headers with a total of 504 pins have to be integrated on the base board [12]. Up to four M3 screws may be used to mechanically fasten the module to the base board. Do not use excessive force to tighten the screws, as this could damage the module.

The pinout of the module connector is found in the Mercury Master Pinout [11]. The connector is available in different packaging options and different stacking heights. Some examples are presented in Table 4. Refer to the connector datasheet for more information.

Component	Part Number	Description
Mercury module connector	FX10A-168S-SV	Hirose FX10, 168-pin, 0.5 mm pitch
Base board connector	FX10A-168P-SV(71)	Hirose FX10, 168-pin, 0.5 mm pitch, 4 mm stacking height
Base board connector	FX10A-168P-SV1(71)	Hirose FX10, 168-pin, 0.5 mm pitch, 5 mm stacking height

Table 4: Module Connector Characteristics

Figure 9 indicates the pin numbering for the Mercury module connectors from the top view of the base board. The connector pins are numbered as follows:

- Connector A: from J800-1 to J800-168
- Connector B: from J801-1 to J801-168
- Connector C: from J900-1 to J900-168

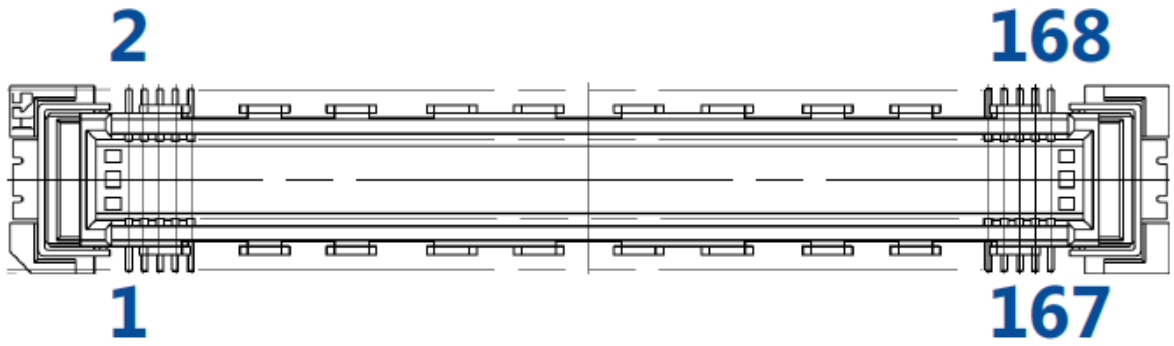

Figure 9: Pin Numbering for the Module Connector

2.8 User I/O

2.8.1 Pinout

Information on the Mercury+ XU9 SoC module pins can be found in the Mercury Master Pinout [11], and in the additional document Mercury Mars Module Pin Connection Guidelines [10].

> **Tip**
>
> The pin types on the schematic of the module connector and in the master pinout document are for reference only. On the Mercury+ XU9 SoC module, the connected pins might not have the targeted functions (such as primary clocks, differential pins, transceiver signals, etc).

The naming convention for the user I/Os located in HP banks is:
IO_B<BANK>_L<PAIR_NUMBER>_<SPECIAL_FUNCTION>_<PACKAGE_PIN>_<POLARITY>.

For example, IO_B65_L6_AD6_AF10_P is located on pin AF10 of I/O bank 65, pair 6, it is a System Monitor differential auxiliary analog input capable pin and it has positive polarity, when used in a differential pair.

The HD banks are numbered differently depending on the MPSoC device assembled on the module. Table 5 presents the mapping between the GTH generic bank letters and the device-specific bank numbers.

Device	Bank	
	N	O
ZU4 ZU5	46	45
ZU7	47	48

Table 5: Mapping Between the Generic I/O Bank Letters and the Device-Specific I/O Bank Numbers

The naming convention for the user I/Os located in HD banks is:
IO_B<BANK_LETTER>_L<PAIR_NUMBER>_<SPECIAL_FUNCTION>_<PACKAGE_PIN>_<POLARITY>

For example, IO_BN_L7_HDGC_AD5_E13_N is located on pin E13 of I/O bank N, pair 7, it is a System Monitor differential auxiliary analog input capable pin and also a clock capable pin and it has negative polarity, when used in a differential pair.

The global clock capable pins are marked with "GC" (HP I/O banks) or with "HDGC" (HD I/O banks) in the signal name. For details on their function and usage, refer to the AMD documentation.

Table 6 includes information related to the total number of I/Os available in each I/O bank and possible limitations.

Signal Name	Sign.	Pairs	Differential	Single-ended	Bank	Bank Type[3]
IO_B64_<...>	4	0	-	In/Out	64	HP
IO_B65_<...>	20	10	In/Out	In/Out	65	HP
IO_B66_<...>	6	0	-	In/Out	66	HP
IO_BN_<...>	24	12	In/Out (no LVDS/LVPECL outputs supported; internal differential termination not supported) Refer to Section 2.8.3 for details.	In/Out	N	HD
IO_BO_<...>	24	12	In/Out (no LVDS/LVPECL outputs supported; internal differential termination not supported) Refer to Section 2.8.3 for details.	In/Out	O	HD
Total	**78**	**34**	-	-	-	-

Table 6: User I/Os

The multi-gigabit transceiver (MGT) are described in Section 2.9.

2.8.2 I/O Pin Exceptions

The I/O pin exceptions are pins with special functions or restrictions (for example, when used in combination with certain Mercury boards they may have a specific role).

PCIe Reset Signal (PERST#)

Table 7 lists the I/O pin exceptions on the Mercury+ XU9 SoC module related to the PCIe reset connection.

I/O Name	Module Connector Pin	Description
PS_MIO42_PERST#	A104	When the pin has a low value, its value is routed via a 1 kΩ resistor to the ETH0_TXD3_PS_PERST# pin (MIO[30]) and via a 47 kΩ resistor and a level shifter to PL_PERST#_LS (MPSoC package pin AF2) for PCIe PERST# connection implementation.

Table 7: I/O Pin Exceptions - PERST#

[3] HD = high density pins, HP = high performance pins; Refer to the Zynq UltraScale+ MPSoC Data Sheet: Overview [26] for details.

When the Mercury+ XU9 SoC module is used in combination with a Mercury+ PE1 base board as a PCIe device, the PERST# signal coming from the PCIe edge connector on the module connector pin A104 (PS_MIO42_PERST#) is driven further to PL_PERST#_LS and to ETH0_TXD3_PS_PERST# (MIO[30]) when its value is low.

When a PCIe block on the PL side is used, the PERST# signal is connected to the MPSoC pin PL_PERST#_LS via a 47 kΩ resistor and a level shifter.

When a PCIe block on the PS side is used, the PERST# signal is routed via a 1 kΩ resistor to MIO30. This is the default MIO pin used for the reset signal of the PCIe PS built-in block, therefore it was chosen for the reset implementation. The Ethernet controller 0 is disabled when the PCIe hard block is used; note that any other valid position for PERST# would have resulted in having the Ethernet controller disabled.

Using a PCIe block in the PL simultaneously with Gigabit Ethernet 0 interface on the PS side is possible. Simultaneous usage of two PCIe endpoints on the PL and PS sides is not supported and was not tested on Enclustra side.

In situations in which PCIe functionality is not required, PS_MIO42_PERST# pin can be used in the same manner as a regular MIO pin.

For root complex applications the PERST# signal can be placed on any unused MIO pin (the restriction on MIO[30] and MIO[42] does not apply in this case).

I/O Pins with Level Shifter

There are four signals on the Mercury+ XU9 SoC module that are routed from the FPGA banks to the module connector via level shifters. These are presented in Table 8.

I/O Name	Module Connector Pin	Description
IO_B64_AF17_LS	A88	These pins have a level shifter from VCC_1V2 to VCC_CFG_MIO
IO_B64_AC19_LS	A90	
IO_B64_AH16_LS	A92	
IO_B64_AG19_LS	A94	

Table 8: I/O Pin Exceptions - Level Shifters

The level shifters used for the I/O pins mentioned in Table 8 are NXP NTB0104 and the maximum achievable data rate on these pins is 30 Mbit/s.

2.8.3 Differential I/Os

When using differential pairs, a differential impedance of 100 Ω must be matched on the base board, and the two nets of a differential pair must have the same length.

The information regarding the length of the signal lines from the MPSoC device to the module connector is available in Mercury+ XU9 SoC Module IO Net Length Excel Sheet [3]. This enables the user to match the total length of the differential pairs on the base board if required by the application.

Tip

The trace length of various signals may change between revisions of the Mercury+ XU9 SoC module. Use the information provided in the Mercury+ XU9 SoC Module IO Net Length Excel Sheet [3] to check which signals are affected. The differential signals will also be routed differentially in subsequent product revisions.

The I/Os in the HD banks (N, O) can be used only as differential inputs when LVDS/LVPECL standards are used; LVDS/LVPECL outputs are not supported.

Internal differential termination is not supported for the HD pins; all differential signal pairs from both HD banks may optionally be equipped with 100 Ω differential termination resistors on the module. Refer to Section 2.8.6 for details.

2.8.4 I/O Banks

Table 9 describes the main attributes of the Programmable Logic (PL) and Processing System (PS) I/O banks, and indicates which peripherals are connected to each I/O bank. All I/O pins within a particular I/O bank must use the same I/O (VCC_IO) and reference (VREF) voltages.

Bank	Bank Type	Connectivity	Supply Voltage	Ref. Voltage
PL MGT Banks				
A	MGT	Module connector	0.9 V	-
B	MGT	Module connector	0.9 V	-
C	MGT	Module connector	0.9 V	-
D	MGT	Module connector	0.9 V	-
PL I/O Banks				
64	HP	Module connector, DDR4 SDRAM, I2C, LEDs	1.2 V	½ × VCC_1V2
65	HP	Module connector, DDR4 SDRAM, clock oscillator	1.2 V	½ × VCC_1V2
66	HP	Module connector, DDR4 SDRAM	1.2 V	½ × VCC_1V2
N	HD	Module connector	VCC_IO_BN, user selectable	-
O	HD	Module connector	VCC_IO_BO, user selectable	-
PS Banks				
500	PS MIO	eMMC and QSPI flash devices, I2C, LEDs	1.8 V	-

Continued on next page...

Bank	Bank Type	Connectivity	Supply Voltage	Ref. Voltage
501	PS MIO	Module connector, Gigabit Ethernet PHY 0	VCC_CFG_MIO, user selectable	-
502	PS MIO	USB PHY 0, Gigabit Ethernet PHY 1 / USB PHY 1 (shared)	1.8 V	-
503	PS CONFIG	FPGA PS configuration	VCC_CFG_MIO, user selectable	-
504	PS DDR	DDR4 SDRAM	1.2 V	½ × VCC_1V2
505	PS GTR	Module connector, GTR oscillators	VCC_0V85	-

Table 9: I/O Banks

2.8.5 VCC_IO Usage

The VCC_IO voltages for the I/O banks located on the module connector are configurable by applying the required voltage to the VCC_IO_B[x], respectively VCC_CFG_[x] pins. All VCC_IO_B[x] or VCC_CFG_[x] pins in a given bank must be connected to the same voltage.

For compatibility with other Enclustra Mercury modules, it is recommended to use a single I/O voltage per module connector.

Signal Name	MPSoC Pins	Supported Voltages	Connector A Pins
VCC_CFG_MIO	VCCO_PSIO1_501, VCCO_PSIO3_503	1.8 V - 3.3 V ±5%	A74, A77
VCC_IO_BN	VCCO_N	1.2 V - 3.3 V ±5%[5]	A38
VCC_IO_BO	VCCO_O	1.2 V - 3.3 V ±5%[5]	A41

Table 10: VCC_IO Pins

On module connectors B and C there are no VCC_IO pins available, as the signals routed to this connector belong to FPGA banks which are powered by fixed voltages generated on the module. The VCC_IO pins on connectors B and C are used on other Enclustra modules. For compatibility purposes, it is acceptable to power these pins even if they are not used on the Mercury+ XU9 SoC module.

The Mercury+ XU9 SoC module may be used in combination with base boards having only two module connectors.

Figure 10 illustrates the requirements of the VCC_IO power sequence. Do not power the VCC_IO pins when PWR_GOOD and PWR_EN signals are not active. If the module is not powered, make sure that the VCC_IO voltages are disabled, for example, by using a switch that uses PWR_GOOD as enable signal on the base board.

[4] For HD I/O banks generic supply names are used - refer to Section 2.8.4 for details on I/O banks connectivity and supplies.
[5] For voltages of 3.3 V for VCC_IO_BN and VCC_IO_BO, the tolerance range is -5% to +3%.

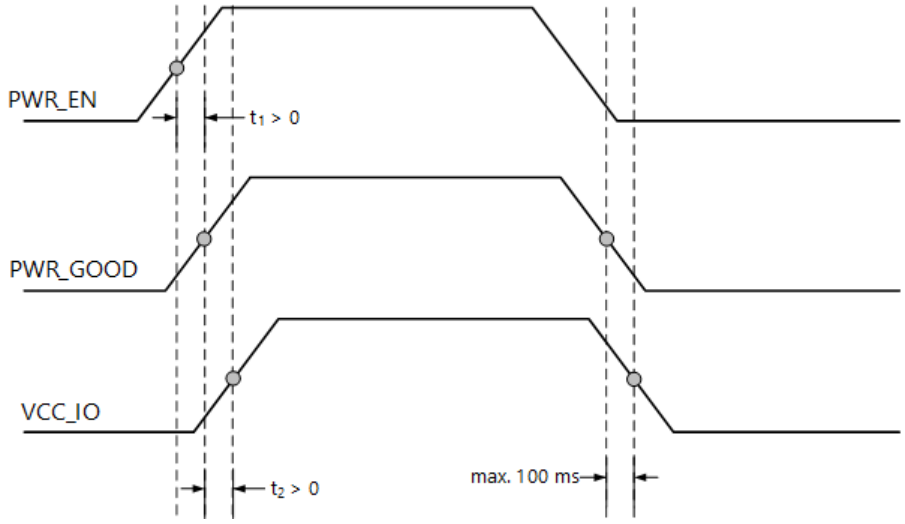

Figure 10: Power-Up Sequence - VCC_IO in Relation with PWR_GOOD and PWR_EN Signals

NOTICE

Damage to the device due to unsuitable voltage

Unsuitable voltages may damage the MPSoC device as well as other devices on the Mercury+ XU9 SoC module.

- Only use VCC_IO voltages compliant with the assembled MPSoC device.

NOTICE

Damage to the device due to floating VCC_IO pins

Floating VCC_IO pins reduce ESD protection.

- Do not leave any VCC_IO pin floating.

⚠ CAUTION

Injury due to uncontrolled device

If an I/O is connected to an external device, violating the power sequence or leaving the corresponding VCC_IO pin floating will leave the pin in an undefined state. This can lead to any behavior of the devices attached to this pin and, potentially, to damage or injuries.

- Follow the power sequence diagram shown in Figure 10. This ensures that the I/Os are tri-stated at power-on and power-off.
- Do not leave VCC_IO pins floating.

2.8.6 Signal Terminations

Differential Inputs

Internal differential termination is not supported for the HD pins. If required, differential signal pairs from the HD banks may optionally be equipped with 100 Ω differential termination resistors on the base board.

The resistor identifiers for each differential input pair can be retrieved from the Mercury+ XU9 SoC Module User Schematic [5].

Single-Ended Outputs

There are no series termination resistors on the Mercury+ XU9 SoC module for single-ended outputs. If required, series termination resistors may be assembled on the base board (close to the module pins).

2.8.7 Multiplexed I/O (MIO) Pins

Details on the MIO/EMIO terminology are available in the Zynq UltraScale+ MPSoC Technical Reference Manual [22].

Some of the MIO pins on the Mercury+ XU9 SoC module are connected to on-board peripherals, while others are available on the module connector; the suggested functions below are for reference only. Always verify your MIO pinout with the AMD device handbook.

Table 11 gives an overview over the MIO pin connections on the Mercury+ XU9 SoC module. Only the pins marked with "user functionality" are available on the module connector.

MIO Pins	Function(s)	Connection(s)
[0:5]	QSPI flash	QSPI flash
[6]	QSPI feedback clock	-
[7:9]	Unused	-
[10:11]	I2C	On-board I2C bus and module connector via level shifter
[12]	I2C interrupt	On-board I2C bus
[13:22]	eMMC flash	eMMC flash
[23]	USB PHY 1 reset	USB 2.0 PHY 1
[24:25]	LED0#, LED1#	On-board LEDs
[26:29,31:37]	Ethernet 0	Gigabit Ethernet PHY 0
[30]	Ethernet 0 PCIe block PERST# signal[6]	Gigabit Ethernet PHY 0 Module connector via series resistor
[38]	UART RX[7] User functionality	Module connector
[39]	UART TX[7] User functionality	Module connector
[40:41,43:44]	User functionality	Module connector

Continued on next page...

MIO Pins	Function(s)	Connection(s)
[42]	PCIe block PERST# signal[6] User functionality	Module connector
[45:51]	SD card User functionality	Module connector
[52:63]	USB 0	USB 2.0 PHY 0
[64:75]	Ethernet 1 USB 1	Gigabit Ethernet PHY 1 USB 2.0 PHY 1
[76:77]	Ethernet MDIO	Gigabit Ethernet PHY 1 and PHY 0 via level shifter

Table 11: MIO Pins Connections Overview

2.8.8 Analog Inputs

The Zynq UltraScale+ MPSoC devices contain a system monitor in the PL and an additional system monitor block in the PS. These are used to sample analog inputs and to collect information on the internal voltages and temperatures.

The system monitor block in the PL provides a 10-bit ADC, which supports up to 17 external analog signal lines (1 dedicated differential input, 16 auxiliary differential inputs). The auxiliary analog signal lines of the MPSoC device are available on the module connector; these I/Os have the abbreviation "AD" followed by the ADC channel in the signal name. The ADC input channels are always used differentially. For single-ended applications, the *_N line must be connected to ground. The dedicated channel is not available on the module connector.

The analog input signals can be connected to any normal I/O FPGA bank, provided that all analog pins belong to the same bank. Note that the HD I/O banks have a limited number of analog inputs and they must be connected directly to the SYSMONE4 primitive instead of to the AMD System Management Wizard IP core.

For detailed information on the ADC and system monitor, refer to the UltraScale Architecture System Monitor document [23], Zynq UltraScale+ MPSoC Technical Reference Manual [22] and System Management Wizard Product Guide [25].

Table 12 presents the ADC Parameters for the PL System Monitor (SYSMON). The PS System Monitor is only used for monitoring the on-chip power supply voltages and die temperature.

[6] Used for PCIe PERST# connection implementation. Refer to Section 2.8.2 for details.
[7] UART RX is an MPSoC input; UART TX is an MPSoC output.

Parameter	Value (PL SYSMON)
VCC_ADC	1.8 V
VREF_ADC	Internal
ADC Range	0-1 V
Sampling Rate per ADC	0.2 MSPS
Total number of channels available on the module connector	Maximum 12 auxiliary inputs (12 HD pairs or 6 HP pairs)

Table 12: System Monitor (PL) Parameters

2.9 Multi-Gigabit Transceiver (MGT)

There are two types of multi-gigabit transceivers available on the Mercury+ XU9 SoC module: GTH transceivers (connected to the PL) and GTR transceivers (connected to the PS).

Tip

For optimal performance of high-speed interfaces, for example, PCIe, use redrivers on the base board.

Tip

The maximum data rate on the transceivers on the Mercury+ XU9 SoC module depends on the routing path for these signals. When using transceivers at high performance rates, ensure adequate signal integrity over the full signal path.

NOTICE

Damage to the transceivers

No AC coupling capacitors are placed on the Mercury+ XU9 SoC module on the transceivers.

- If required by your application, ensure that capacitors are mounted on the base board, close to the module pins.

GTH Transceivers

The GTH banks are numbered differently depending on the MPSoC device assembled on the module. Table 13 presents the mapping between the GTH generic bank letters and the device-specific bank numbers.

Device	Bank			
	A	B	C	D
ZU4 ZU5	223	224	225	226
ZU7	224	225	226	227

Table 13: Mapping Between the Generic GTH Bank Letters and the Device-Specific GTH Bank Numbers

There are 16 GTH MGTs available on the Mercury+ XU9 SoC module organized in four FPGA banks. Table 14 describes the connections.

The naming convention for the GTH MGT I/Os is:
MGT_B<BANK_LETTER>_<FUNCTION>_<PACKAGE_PIN>_<POLARITY>.

For example, MGT_BB_TX2_L3_N is located on pin L3 of MGT I/O bank B, it is a transmit pin and it has negative polarity.

Signal Name	Signal Description	Pairs	I/O Bank
MGT_BA_RX<...>	MGT receivers	4	A
MGT_BA_TX<...>	MGT transmitters	4	
MGT_BA_REFCLK<...>	MGT reference input clocks	2	
MGT_BB_RX<...>	MGT receivers	4	B
MGT_BB_TX<...>	MGT transmitters	4	
MGT_BB_REFCLK<...>	MGT reference input clocks	2	
MGT_BC_RX<...>	MGT receivers	4	C
MGT_BC_TX<...>	MGT transmitters	4	
MGT_BC_REFCLK<...>	MGT reference input clocks	2	
MGT_BD_RX<...>	MGT receivers	4	D
MGT_BD_TX<...>	MGT transmitters	4	
MGT_BD_REFCLK<...>	MGT reference input clocks	2	
Total		**40**	

Table 14: MGT Pairs

Twelve of the GTH pairs and six corresponding clocks are routed to module connector C, while four GTH pairs and two reference input clock differential pairs are routed to module connector B.

The GTH MGTs on the MPSoC device support data rates of 12.5 Gbit/s on speed grade 1 devices and of 16.375 Gbit/s on the other devices. Hirose has removed the bandwidth limitation to 15 Gbit/s from the past, thefore the maximum MPSoC performance may be achieved.

The MPSoC devices assembled on the Mercury+ XU9 SoC module can support up to two integrated PCIe Gen3 ×16 interfaces on the PL side, implemented using GTH transceivers. Simultaneous usage of these

interfaces is limited to the available hardware resources (number of transceivers and lane mapping).

GTR Transceivers

There are four GTR MGT pairs and two reference input clock differential pairs on the Mercury+ XU9 SoC module connected to I/O bank 505; these are routed to module connector B.

The naming convention for the GTR MGT I/Os is:
MGTPS_<FUNCTION>_<PACKAGE_PIN>_<POLARITY>.

For example, MGTPS_RX2_H28_N is located on pin H28 of PS GTR bank (bank 505), it is a receive pin and it has negative polarity.

All Mercury+ XU9 SoC module variants support the implementation of a PCIe Gen2 ×4 interface.

When the PCIe hard block is used, it is not possible to use the Ethernet 0 interface. Ethernet PHY 0 is connected to ETH 0 controller from the PS I/O bank 501; one of the Ethernet TX data signals is shared with the PCIe reset signal (PERST#). Refer to Sections 2.8.2 and 2.8.7 for details on the PERST# connection.

The GTR pairs support data rates of 6 Gbit/s and can be used for the implementation of several interfaces such as PCIe Gen2 ×4, USB 3.0, DisplayPort, SATA, or Ethernet SGMII. Refer to the Zynq UltraScale+ MPSoC Technical Reference Manual [22] and to the Zynq UltraScale+ MPSoC Data Sheet: Overview [26] for details.

A 100 MHz LVDS oscillator and a 27 MHz CMOS oscillator provide reference clock inputs to the PS GTR bank 505. Refer to Section 2.11 for details.

2.10 Power

2.10.1 Power Generation Overview

The Mercury+ XU9 SoC module uses a 5 V to 15 V DC power input for generating the on-board supply voltages. Some of these voltages are accessible on the module connector. Table 15 describes the power supplies generated on the module.

Output Supply Name	Voltage Value	Rated Current	Input Supply Name	Shut down via PWR_EN	Influences PWR_GOOD
VCC_INT	0.72 V/0.85 V/0.9 V (PL core supply)	35 A	VCC_MOD	Yes	Yes
VCC_PSINT	0.85 V/0.9 V (PS core supply)	5 A	VCC_MOD	Yes	Yes
VCC_0V85[8]	0.85 V (GTR transceiver supply)	0.5 A	VCC_1V2	Yes	No
VCC_0V9	0.9 V	6 A	VCC_MOD	Yes	Yes
VCC_1V2	1.2 V	6 A	VCC_MOD	Yes	Yes
VCC_BAT_FPGA	1.2 V	10 mA	VCC_BAT	No	No
VCC_1V8	1.8 V	3 A	VCC_MOD	Yes	Yes
VCC_2V5	2.5 V	0.5 A	VCC_3V3	Yes	No
VCC_3V3	3.3 V	6 A	VCC_MOD	No	Yes
VCC_5V0	5.0 V	0.15 A	VCC_MOD	No	No

Table 15: Generated Power Supplies

In the standard configuration the PL core supply is 0.85 V. For custom configurations, in which a speed grade -3E MPSoC device is assembled, an assembly variant is available to switch the PL core operating voltage to 0.9 V. Similarly, in situations in which a speed grade -2LE or -1LI device is used, an assembly variant is available to switch the PL core operating voltage to 0.72 V.

In the standard configuration the PS core supply is 0.85 V. For custom configurations, in which a speed grade -3E MPSoC device is assembled, an assembly variant is available to switch the PS core operating voltage to 0.9 V.

Refer to the Mercury Mars Module Pin Connection Guidelines [10] for general rules on the power pins.

Power Converter Synchronization

Starting with revision 2.1 modules, the switching converters used on the Mercury+ XU9 SoC module are upgraded to a newer version due to end of life of the original parts. They do not support synchronization of the switching frequency with any clock signal anymore. The signal PWR_SYNC from previous revisions (package pin W9) is not connected anymore.

2.10.2 Power Enable/Power Good

The Mercury+ XU9 SoC module provides a power enable input on the module connector. This input may be used to shut down the DC/DC converters and LDOs for 0.72/0.85/0.9 V, 0.85/0.9 V, 0.9 V, 1.2 V, 1.8 V and 2.5 V. The list of converters that can be disabled via PWR_EN signal is provided in Section 2.10.1.

[8] An LDO is used to generate the GTR transceiver supply when a -1LI, -2LE, or -3E speed grade MPSoC device is used. For the other speed grades, VCC_INT is used.

The PWR_EN input is pulled to VCC_3V3 on the Mercury+ XU9 SoC module with a 10 kΩ resistor. The PWR_GOOD signal is pulled to VCC_3V3 on the Mercury+ XU9 SoC module with a 10 kΩ resistor.

PWR_GOOD is an open collector signal and must not be used to drive a load directly. This signal is pulled to ground if the on-board regulators fail or if the module is disabled via PWR_EN. The list of converters that influence the state of the PWR_GOOD signal is provided in Section 2.10.1.

The role of PWR_GOOD and PWR_EN on the VCC_IO power sequence is presented in Section 2.8.5.

NOTICE

Damage to the device due to unsuitable voltage

Appling unsuitable voltage to the PWR_EN or PWR_GOOD pins can damage the Mercury+ XU9 SoC module.

- Do not actively drive the PWR_EN or PWR_GOOD pins to anything other than ground.
- Do not pull these pins up to a voltage level higher than 3.3 V.

Pin Name	Module Connector Pin	Comment
PWR_EN	A10	Floating/3.3 V: Module power enabled Driven low: Module power disabled
PWR_GOOD	A12	0 V: Module supply not ok 3.3 V: Module supply ok

Table 16: Module Power Status and Control Pins

2.10.3 Voltage Supply Inputs

Table 17 describes the power supply inputs on the Mercury+ XU9 SoC module. The VCC voltages used as supplies for the I/O banks are described in Section 2.8.5.

Supply Name	Module Connector Pins	Voltage	Description
VCC_MOD	A1, A2, A3, A4, A5, A6, A7, A8, A9, A11	5 - 15 V	Supply for on-module generated power supplies. The 2.5 V supply is generated from the 3.3 V supply. The input current is rated at 3 A (0.3 A per connector pin).
VCC_BAT	A168	2.7 - 3.6 V	Supply for the battery voltage for MPSoC battery-backed RAM and battery-backed RTC.

Table 17: Voltage Supply Inputs

2.10.4 Voltage Supply Outputs

Table 18 presents the supply voltages generated on the Mercury+ XU9 SoC module, that are available on the module connector.

Supply Name	Module Connector Pins	Voltage	Maximum Current[9]	Comment
VCC_3V3	A26, A29, A50, A86 B55, B79, B115, B127, B152, B155 C96, C103, C136, C143	3.3 V ±5%	4 A (max. 0.3 A per pin)	Always active
VCC_2V5	A53, A62, A65, A89	2.5 V ±5%	0.25 A	Controlled by PWR_EN
VCC_1V8	B52, B76, B108, B128 C83, C123, C165	1.8 V ±5%	1.5 A	Controlled by PWR_EN

Table 18: Voltage Supply Outputs

NOTICE

Damage to the device due to unsuitable usage of the output pins

- Do not connect any power supply to the voltage supply outputs.
- Do not short circuit any of the voltage supply outputs to ground.

2.10.5 Power Consumption

The power consumption of any MPSoC device strongly depends on the application (on the configured bitstream and I/O activity).

To estimate the power consumption of your design, use the AMD Power Estimator (XPE) available on the AMD website.

2.10.6 Heat Dissipation

High performance devices like the AMD Zynq UltraScale+ MPSoC need cooling in most applications; always make sure the MPSoC is adequately cooled.

For Mercury modules an Enclustra heat sink kit is available for purchase along with the product. It represents an optimal solution to cool the Mercury+ XU9 SoC module - the heat sink body is low profile and usually covers the whole module surface. The kit comes with a gap pad for the MPSoC device, a fan and required mounting material to attach the heat sink to the module PCB and baseboard PCB. With additional user configured gap pads, it is possible to cool other components on the board as well.

Alternatively, if the Enclustra heat sink does not match the application requirements, a third-party heat sink body (ATS) and an additional gap pad (t-Global) may be used. The Enclustra heat sink kit already contains all necessary items for cooling the module (heat sink body, gap pad, fan, mounting material).

[9] The maximum available output current depends on your design. See Sections 2.10.1 and 2.10.5 for details.

Table 19 lists the heat sink and thermal pad part numbers that are compatible with the Mercury+ XU9 SoC module. Details on the Mercury heat sink kit can be found in the Mercury Heat Sink Kits User Manual [20].

Product Name	Package Name	Enclustra Heat Sink	ATS Heat Sink	t-Global Thermal Pad
Mercury+ XU9	FBVB900 [27]	ACC-HS4-Set	ATS-52310G-C1-R0	TG6050-30-30-1

Table 19: Heat Sink Characteristics

Tip

The adhesive heat sink part is recommended only for prototyping purposes. When the module is used in environments subject to vibrations, additional mechanical fixation is recommended.

NOTICE

Damage to the device due to overheating

Depending on the user application, the Mercury+ XU9 SoC module may consume more power than can be dissipated without additional cooling measures.

- Ensure that the MPSoC is always adequately cooled by installing a heat sink and/or providing air flow.

2.10.7 Voltage Monitoring

Several pins on the module connector on the Mercury+ XU9 SoC module are marked as VMON. These are voltage monitoring outputs that are used in the production test for measuring some of the on-board voltages.

It is not allowed to draw power from the voltage monitoring outputs.

Tip

The voltage monitoring outputs are for Enclustra-use only. Pinout changes may be applied between revisions.

Table 20 presents the VMON pins on the Mercury+ XU9 SoC module.

Pin Name	Mod. Conn. Pin	Assembly Variant	Connection	Description
VMON_INT	A102	All	VCC_INT	PL core voltage
VMON_VTT_VBAT	B8	Default Custom	VCC_VTT VCC_BAT_FPGA	DDR termination voltage MPSoC battery voltage
VMON_PSINT	B168	All	VCC_PSINT	PS core voltage
VMON_0V9	B167	All	VCC_0V9	0.9 V on-board voltage
VMON_1V2	C8	All	VCC_1V2	1.2 V on-board voltage

Table 20: Voltage Monitoring Outputs

2.11 Clock Generation

A 33.33 MHz oscillator is used for the Mercury+ XU9 SoC module clock generation; the 33.33 MHz clock is fed to the PS. A 100 MHz LVDS oscillator is connected to FPGA bank 65 and can serve as a reference for the PLL used to generate the clocks required for the PL DDR interface. The signal is terminated with a 100 Ω parallel resistor close to the FPGA pins. The same 100 MHz clock is used as a reference clock input for PS GTR bank 505.

A 27 MHz CMOS oscillator provide a reference clock input to the PS GTR bank 505. A 24 MHz clock and a 25 MHz clock are used for the USB PHYs and Ethernet PHYs respectively. The crystal pads for the MPSoC RTC are connected to a 32.768 kHz oscillator on the Mercury+ XU9 SoC module.

Table 21 describes the clock connections to the MPSoC device.

Signal Name	Frequency	Package Pin	MPSoC Pin Type
CLK33	33.33 MHz	P19	PS_REF_CLK
GTR_CLK27_P GTR_CLK27_N	27 MHz	H23 H24	PS_MGTREFCLK3P_505 PS_MGTREFCLK3N_505
GTR_CLK100_P GTR_CLK100_N	100 MHz	K23 K24	PS_MGTREFCLK2P_505 PS_MGTREFCLK2N_505
CLK100_P CLK100_N	100 MHz	AH6 AJ6	IO_L13P_T2L_N0_GC_QBC_65 IO_L13N_T2L_N1_GC_QBC_65
PS_PADI PS_PADO	32.768 kHz	M21 N21	PS_PADI (crystal pad input for MPSoC built-in RTC) PS_PADO (crystal pad output for MPSoC built-in RTC)

Table 21: Module Clock Resources

2.12 Reset

The power-on reset signal (POR) and the PS system reset signal (SRST) of the MPSoC device are available on the module connector.

Pulling PS_POR# low resets the MPSoC device, the Ethernet and the USB PHYs, and the QSPI and eMMC flash devices. Refer to the Mercury Mars Module Pin Connection Guidelines [10] for general rules regarding the connection of reset pins.

Pulling PS_SRST# low resets the MPSoC device and enables the connection between QSPI flash and module connector, allowing the flash to be programmed from an external SPI master.

For details on the functions of the PS_POR_B and PS_SRST_B signals refer to the Zynq UltraScale+ MPSoC Technical Reference Manual [22].

Table 22 presents the available reset signals. Both signals, PS_POR# and PS_SRST#, have on-board 10 kΩ pull-up resistors to VCC_CFG_MIO. For on-board devices using 1.8 V signaling, a PS_POR# low voltage variant is generated (PS_POR#_LV).

Signal Name	Connector Pin	MPSoC Pin	Pin Name	Description
PS_POR#	A132	N19	PS_POR_B	Power-on reset
PS_SRST#	A124	P20	PS_SRST_B	System reset

Table 22: Reset Resources

PS_POR# is automatically asserted if PWR_GOOD is low.

2.13 LEDs

There are three active-low user LEDs on the Mercury+ XU9 SoC module - two of them are connected to the PS and one connected to the PL.

Signal Name	Package Pin	Pin Name	Comment
PS_LED0#	A18	MIO[24]	User function / active-low
PS_LED1#	B18	MIO[25]	User function / active-low
PL_LED2#	AF13	IO_T1U12_64	User function / active-low

Table 23: User LEDs

The module is also equipped with two status LEDs, which offer details on the configuration process for debugging purposes.

Signal Name	Package Pin	Pin Name	Comment
PS_ERROR	R22	PS_ERROR_OUT	Refer to Zynq UltraScale+ MPSoC Technical Reference Manual [22]
PS_STATUS	R20	PS_ERROR_STATUS	Refer to Zynq UltraScale+ MPSoC Technical Reference Manual [22]

Table 24: Status LEDs

2.14 DDR4 SDRAM (PS)

There are two DDR4 SDRAM channels on the Mercury+ XU9 SoC module: one attached directly to the PS side (which is available only as a shared resource to the PL side) and one attached directly to the PL side.

The DDR4 SDRAM connected to the PS is mapped to I/O bank 504. The memory configuration on the Mercury+ XU9 SoC module supports ECC error detection and correction; the correction code type used is single bit error correction and double bit error detection (SEC-DED).

Five 16-bit memory chips are used to build an 72-bit wide memory (8 bits are unused): 64 bits for data and 8 bits for ECC.

The maximum memory bandwidth on the Mercury+ XU9 SoC module is:
2'400 Mbit/s × 64 bit = 19'200 MB/s

2.14.1 DDR4 SDRAM Characteristics

Table 25 describes the memory availability and configuration on the Mercury+ XU9 SoC module.

Module	Density	Configuration
ME-XU9-D11E	4 Gbit	256 M × 16 bit
ME-XU9-D12E	8 Gbit	512 M × 16 bit
ME-XU9-D13E	16 Gbit	1 G × 16 bit

Table 25: DDR4 SDRAM (PS) Characteristics

2.14.2 Signal Description

Refer to the Mercury+ XU9 SoC Module FPGA Pinout Excel Sheet [4] for detailed information on the DDR4 SDRAM connections.

2.14.3 Termination

> **Tip**
>
> No external termination is implemented for the data signals on the Mercury+ XU9 SoC module. Enclustra strongly recommends enabling the on-die termination (ODT) feature of the assembled device.

2.14.4 Parameters

Table 26 shows the parameters of the PS DDR4 SDRAM to be set in the Vivado project such that it corresponds to the reference design [2] of the Mercury+ XU9 SoC module.

Parameter	Value
Requested device frequency	1'200 MHz
Memory type	DDR4
Effective DRAM bus width	64 bit
ECC	Enabled
Speed bin	DDR4 2400T
CAS latency	17 cycles
RAS to CAS delay	17 cycles
Precharge time	17 cycles
CAS write latency	12 cycles
tRC	46.16 ns
tRASmin	32 ns
tFAW	30 ns
Additive latency	0 cycles
DRAM IC bus width (per die)	16 bit
DRAM device capacity (per die)	4'096, 8'192, or 16'384 Mbit
Bank group address count	1 bit
Bank address count	2 bit
Row address count	15-16 bit
Column address count	10 bit

Table 26: DDR4 SDRAM (PS) Parameters

2.15 DDR4 SDRAM (PL)

The DDR4 SDRAM connected to the PL[10] is mapped to I/O banks 64, 65 and 66. The DDR bus width is 64-bit.

The DDR4 SDRAM memory controller on the MPSoC device supports speeds up to 2'666 Mbit/s (1'333 MHz), however the memories equipped on the Mercury+ XU9 SoC module are rated 2'400 Mbit/s (1'200 MHz).

[10] DDR4 SDRAM connected to the PL is not functional on revision 1 modules. This issue was fixed starting with revision 2 modules.

The maximum PL memory bandwidth on the Mercury+ XU9 SoC module is:
2'400 Mbit/s × 64 bit = 19'200 MB/s

Note that for MPSoC low power mode (at 0.72 V) the DDR speed is lower than mentioned above. For details, refer to the Zynq UltraScale+ MPSoC Data Sheet: DC and AC Switching Characteristics [24].

2.15.1 DDR4 SDRAM Characteristics

Table 27 describes the memory availability and configuration on the Mercury+ XU9 SoC module.

Module	Density	Configuration
ME-XU9-D11E ME-XU9-D12E-L11	4 Gbit	256 M × 16 bit
ME-XU9-D13E ME-XU9-D11E-L13	16 Gbit	1 G × 16 bit

Table 27: DDR4 SDRAM (PL) Characteristics

2.15.2 Signal Description

Refer to the Mercury+ XU9 SoC Module FPGA Pinout Excel Sheet [4] for detailed information on the DDR4 SDRAM connections.

2.15.3 Termination

> **Tip**
>
> No external termination is implemented for the data signals on the Mercury+ XU9 SoC module. Enclustra strongly recommends enabling the on-die termination (ODT) feature of the assembled device.

2.15.4 Parameters

Table 28 shows the parameters of the PL DDR4 SDRAM to be set in the Vivado project such that it corresponds to the reference design [2] of the Mercury+ XU9 SoC module.

Parameter	Value
Memory device interface speed	833 ps
Reference input clock speed	10'000 ps (100 MHz)[11]
Memory part	MT40A256M16[12]
Data width	64 bit
Data mask and DBI	DM NO DBI
CAS latency	17 cycles
CAS write latency	12 cycles

Table 28: DDR4 SDRAM (PL) Parameters

2.16 QSPI Flash

The QSPI flash can be used to boot the PS, and to store the FPGA bitstream, ARM application code and other user data.

2.16.1 QSPI Flash Characteristics

Table 29 describes the memory availability and configuration on the Mercury+ XU9 SoC module.

As there is one QSPI flash chip assembled on the Mercury+ XU9 SoC module, type "single" must be selected when programming the flash from Vivado tools.

Part Number	Size	Manufacturer
S25FL512S	512 Mbit	Cypress (Spansion)

Table 29: QSPI Flash Characteristics

> **Tip**
>
> Different flash memory devices may be assembled in future revisions of the Mercury+ XU9 SoC module. Any flash memory with a different speed and temperature range fulfilling the requirements of the module variant may be used.

2.16.2 Signal Description

The QSPI flash is connected to the PS MIO pins 0 to 5. Some of these signals are available on the module connector, allowing the user to program the QSPI flash from an external source.

The reset of the QSPI flash is connected to the PS_POR#_LV power-on reset signal.

Refer to Section 3 for details on programming the flash memory.

> **Tip**
>
> For optimal signal integrity, avoid long traces when when connecting the QSPI flash signals on the base board. Long traces or high capacitance may disturb the data communication between the MPSoC and the flash device.

2.16.3 Configuration

The QSPI flash supports up to 50 MHz operation for standard read. For fast, dual and quad read speed values, refer to the flash device datasheet. The "Feedback Clk" option on pin MIO[6] must be enabled in the Zynq configuration for clock rates higher than 40 MHz.

Refer to Zynq UltraScale+ MPSoC Technical Reference Manual [22] for details on booting from the QSPI flash.

Using the Write Register (WWR) command can corrupt the QSPI flash. This issue is described in more details in the Mercury+ XU9 SoC Module Known Issues and Changes [6].

[11] An exact period of 10'000 ps may not be achievable. The clock speed closest to the desired frequency should be selected.

[12] The memory devices assembled on the module may not be available in Vivado. In this case, a similar memory part with compatible timing requirements should be selected.

2.17 eMMC Flash

The eMMC flash can be used to boot the PS, and to store the FPGA bitstream, ARM application code and other user data.

2.17.1 eMMC Flash Characteristics

The Mercury+ XU9 SoC module is equipped with a 16 GB eMMC flash.

> **Tip**
>
> Different flash memory devices may be assembled in future revisions of the Mercury+ XU9 SoC module. Any flash memory with a different speed and temperature range fulfilling the requirements of the module variant may be used.

2.17.2 Signal Description

The eMMC flash signals are connected to the MIO pins 13 to 22 for 8-bit data transfer mode. The command signal has a 4.7 kΩ pull-up resistor to 1.8 V and the data signal lines have 47 kΩ pull-up resistors to 1.8 V.

2.18 SD Card

An SD card can be connected to the PS MIO pins 45 to 51. The corresponding MIO pins are available on the module connector. Information on SD card boot mode is available in Section 3.9.

External pull-ups are needed for SD card operation. Depending on the selected voltage for VCC_CFG_MIO, a level shifter to 3.3 V may be required (some level shifters also have built-in pull-ups).

For booting from an Ultra High Speed (UHS) SD card, an SD 3.0 compliant level shifter is required on the base board and VCC_CFG_MIO must be set to 1.8 V. This boot mode has not been tested, but it may be supported in the future.

2.19 Dual Gigabit Ethernet

Two 10/100/1000 Mbit Ethernet PHYs are available on the Mercury+ XU9 SoC module, both connected to the PS via RGMII interfaces.

2.19.1 Ethernet PHY Characteristics

Table 30 describes the Ethernet PHY devices assembled on the Mercury+ XU9 SoC module.

Part Number	Manufacturer	Description
KSZ9031RNX	Microchip (Micrel)	10/100/1000 Mbit

Table 30: Gigabit Ethernet PHYs Characteristics

2.19.2 Signal Description

PHY 0 is connected to ETH 0 controller from the PS I/O bank 501. One of the Ethernet TX data signals is shared with the PCIe reset signal (PERST#); if the application requires a hard PCIe block, the ETH 0 interface is not available. Refer to Section 2.8.2 for details on the PERST# connection.

Tip

Remember that the gigabit Ethernet 0 interface is not available when the PCIe endpoint in the PS is used, because of the PERST# connection.

PHY 1 is connected to ETH 3 controller from the PS bank 502. The corresponding MIO signals (pins 64 to 75) are shared between Ethernet PHY 1 and USB PHY 1, therefore only one of them can be used. By default the Ethernet connection is enabled.

Tip

Remember that the USB 1 and Gigabit Ethernet 1 interfaces cannot be used simultaneously.

USB1_RST#_ETH1_RST is pulled to ground via a 1 kΩ resistor; to release the USB PHY from reset, this signal must be driven high from MIO[23]. ETH1_RST# is pulled to 1.8 V via a 10 kΩ resistor; if USB1_RST#_ETH1_RST signal is driven high from the PS, the Ethernet reset is connected to ground.

Both reset signals (for Ethernet and USB) are pulled to ground if the PS_POR# is active. Table 31 describes the behavior of the USB1/ETH1 selection circuit; the default selection is marked in bold.

Condition		Function	
PS_POR#	**USB1_RST#_ETH1_RST (MIO[23])**	USB PHY 1	Ethernet PHY 1
0	-	In reset	In reset
1	**0**	**In reset**	**Active**
1	1	Active	In reset

Table 31: USB1/ETH1 Selection

The two Gigabit Ethernet PHYs have a shared MDIO interface and a shared interrupt signal line. The interrupt outputs of the Ethernet PHYs are connected to the I2C interrupt signal line, which is available on the MIO pin 12.

2.19.3 External Connectivity

The Ethernet signal lines can be connected directly to the magnetics. Refer to the Mercury Mars Module Pin Connection Guidelines [10] for details regarding the connection of Ethernet signals.

2.19.4 MDIO Address

The MDIO interface is shared between the two Gigabit Ethernet PHYs - these can be configured using the corresponding address. The MDIO address assigned to PHY 0 is 3 and to PHY 1 is 7.

The MDIO signals are mapped to MIO pins 76 to 77 and they are routed directly to PHY 1 and via a level shifter to PHY 0.

2.19.5 PHY Configuration

The configuration of the Ethernet PHYs is bootstrapped when the PHYs are released from reset. Make sure all I/Os on the RGMII interface are initialized and all pull-up or pull-down resistors are disabled at that moment.

The bootstrap options of the Ethernet PHYs are set as indicated in Table 32.

Strap Input	Signal Value	Description
MODE[3:0]	1110	RGMII mode: advertise all capabilities (10/100/1000, half/full duplex) except 1000Base-T half duplex.
PHYAD[2:0]	011 111	PHY0: MDIO address 3 PHY1: MDIO address 7
CLK125_EN	0	125 MHz clock output disabled
LED_MODE	1	Single LED mode

Table 32: Gigabit Ethernet PHYs Configuration - Bootstraps

For the Ethernet PHY configuration via the MDIO interface, the MDC clock frequency must not exceed 2 MHz.

The PHY is configured in single LED mode with active-low LEDs 1 and 2.

2.19.6 RGMII Delays Configuration

The two Ethernet PHYs are connected directly to hard MAC controllers present in the MPSoC device. In order to achieve the best sampling eye for the RX and TX data, it is recommended to adjust the pad skew delays as specified in Table 33.

The delays can be adjusted by programming the RGMII pad skew registers of the Ethernet PHY. Refer to the PHY datasheet for details.

PHY Register Name	Register Value [binary]	Delay Value
RXD0-RXD3	0111	0 ps
RX_DV	0111	0 ps
RX_CLK	01111	0 ps
TXD0-TXD3	0111	0 ps
TX_EN	0111	0 ps
GTX_CLK	11110	900 ps

Table 33: Gigabit Ethernet PHYs Configuration - RGMII Delays

2.20 USB 2.0

Two USB 2.0 PHYs are available on the Mercury+ XU9 SoC module, both connected to the PS to I/O bank 502. USB PHY 0 can be configured as host or device and USB PHY 1 can be used only as host.

2.20.1 USB PHY Characteristics

Table 34 describes the USB PHY devices assembled on the Mercury+ XU9 SoC module.

Part Number	Manufacturer	Description
USB3320C	Microchip	USB 2.0 PHY

Table 34: USB 2.0 PHY Characteristics

2.20.2 Signal Description

The ULPI interface for the PHY 0 is connected to MIO pins 52 to 63 for use with the integrated USB controller.

The ULPI interface for the PHY 1 is connected to MIO pins 64 to 75. The MIO signals are shared between Ethernet PHY 1 and USB PHY 1, therefore only one of them can be used. By default the Ethernet connection is enabled. Refer to Section 2.19.2 for details on how to select Ethernet or USB mode.

> **Tip**
>
> Remember that the USB 1 and Gigabit Ethernet 1 interfaces cannot be used simultaneously.

2.21 USB 3.0

AMD Zynq UltraScale+ devices feature two built-in USB 3.0 controllers and PHYs, configurable as host or device. The PHY interface used by the USB 3.0 controller is PIPE3, supporting a 5 Gbit/s data rate in host or device modes. The interface of each USB 3.0 controller uses one of the PS GTR lanes.

A 100 MHz differential clock is available on the module and connected to PS_MGTREFCLK2 pins, to be used as a reference clock for the USB 3.0 interface. It is also possible to provide another reference clock from the base board to the MGTPS_REFCLK* pins.

Details on the built-in USB 2.0/3.0 controller and on the usage of the PS GTR lanes are available in the Zynq UltraScale+ MPSoC Technical Reference Manual [22] and in the Zynq UltraScale+ MPSoC Data Sheet: Overview [26].

Figure 11 shows an example of a USB 3.0 implementation using the built-in AMD USB 3.0 interface and the USB 2.0 signals from the PHY, all routed to a USB 3.0 connector on the base board.

> **Tip**
>
> The USB 3.0 interface on the Mercury+ XU9 SoC module uses the GTR signal lines (MGTPS signals on module connector B), and not the USB_SSRX_P/N and USB_SSTX_P/N signal lines on module connector A.

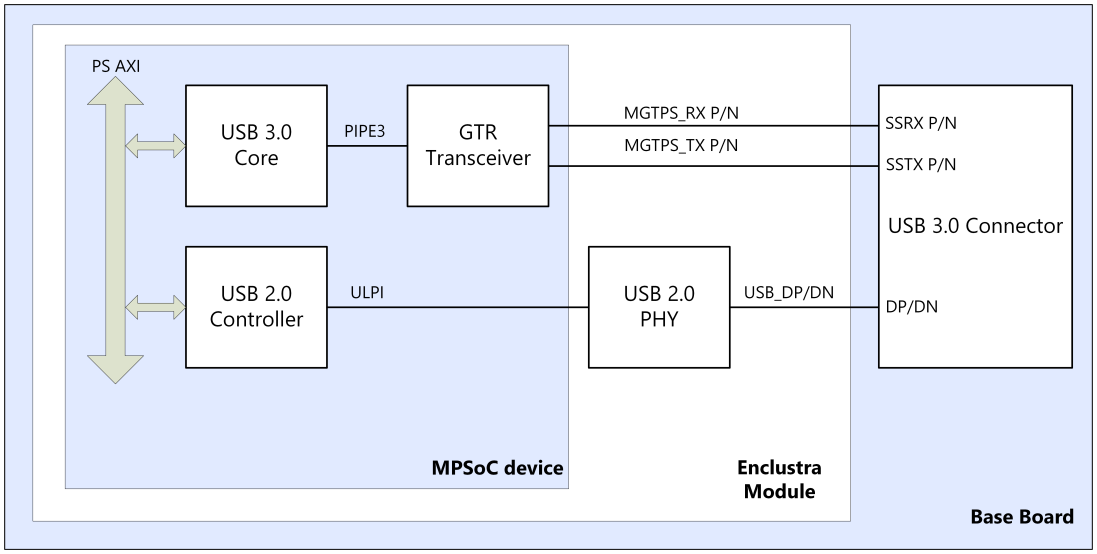

Figure 11: USB 3.0 Implementation Example

2.22 DisplayPort

AMD Zynq UltraScale+ devices feature two built-in DisplayPort controllers and PHYs, supporting up to two lanes at a 5.4 Gbit/s line rate. Each lane is represented by one of the PS GTR transceivers connected to the module connector.

A 27 MHz differential clock is available on the module and connected to PS_MGTREFCLK3 pins, to be used as a reference clock for the DisplayPort interface. It is also possible to provide another reference clock from the base board to the MGTPS_REFCLK* pins.

Details on the built-in DisplayPort controller and on the usage of the PS GTR lanes is available in the Zynq UltraScale+ MPSoC Technical Reference Manual [22] and in the Zynq UltraScale+ MPSoC Data Sheet: Overview [26].

2.23 Real-Time Clock (RTC)

Zynq UltraScale+ devices include an internal real-time clock. The internal RTC can be accessed by the platform management unit (PMU) - more information on the PMU is available in the Zynq UltraScale+ MPSoC Technical Reference Manual [22].

The RTC crystal pad input and crystal pad output are connected on the Mercury+ XU9 SoC module to a 32.768 kHz oscillator.

A 1.5 V LDO[13] is used to generate the battery voltage for the built-in RTC (supplied to VCC_PSBATT pin), based on the VCC_BAT voltage mapped to the module connector. This pin can be connected directly to a 3 V battery on the base board. Refer to the Mercury Mars Module Pin Connection Guidelines [10] for details.

2.24 Secure EEPROM

The secure EEPROM is used to store the module type and serial number, as well as the Ethernet MAC address and other information. It is connected to the I2C bus.

[13] For revisions prior to R3.0, a 1.2 V LDO was used.

The secure EEPROM must not be used to store user data.

Refer to Section 4.4 for details on the content of the EEPROM.

2.24.1 EEPROM Characteristics

Table 35 describes the EEPROM device assembled on the Mercury+ XU9 SoC module.

Part Number	Manufacturer	Assembly Variant
ATSHA204A-MAHDA-T	Atmel	Default
DS28CN01	Maxim	Custom

Table 35: EEPROM Characteristics

An example demonstrating how to read data from the EEPROM is included in the Mercury+ XU9 SoC Module Reference Design [2].

3 Device Configuration

3.1 Configuration Signals

The PS of the MPSoC needs to be configured before the FPGA logic can be used. AMD Zynq devices need special boot images to boot from QSPI flash, eMMC flash or SD card. For more information, refer to the Zynq UltraScale+ MPSoC Technical Reference Manual [22].

Table 36 describes the most important configuration pins and their location on the module connector. These signals allow the MPSoC to boot from QSPI flash, eMMC flash or SD card, and can be used to program the QSPI flash from an external master. Refer to Section 3.12 for details.

Signal Name	MPSoC Pin Type	Mod. Conn. Pin	Description	Comment
PS_DONE	PS_DONE	A130	MPSoC device configuration done	1 kΩ pull-up to VCC_CFG_MIO
PS_POR#	PS_POR_B	A132	MPSoC power-on reset	10 kΩ pull-up to VCC_CFG_MIO
PS_SRST#	PS_SRST_B	A124	MPSoC system reset	10 kΩ pull-up to VCC_CFG_MIO
BOOT_MODE0	-	A126	Boot mode selection	10 kΩ pull-up to VCC_CFG_MIO
BOOT_MODE1	-	A112	Boot mode selection	10 kΩ pull-up to VCC_CFG_MIO

Table 36: MPSoC Configuration Pins

NOTICE

Damage to the device

- Only allow the signals PS_POR# and PS_SRST# to be driven low.
- Do not drive PS_POR# or PS_SRST# to a logic high level.
- Do not drive onto the PS_DONE pin on the base board.

3.2 Module Connector C Detection

Signal C_PRSNT# (pin C167) is equipped with a 4.7 kΩ pull-up resistor to 3.3 V on the module. Since the VCC_IO pins on connector C are not used, C_PRSNT# does not influence the behavior of the module.

For compatibility with other Enclustra modules, it is recommended to connect C_PRSNT# to ground on the base board if the designed base board has three connectors.

3.3 Pull-Up During Configuration

The Pull-Up During Configuration signal (PUDC) is pulled to ground on the module. As PUDC is an active-low signal, all FPGA I/Os will have the internal pull-up resistors enabled during device configuration.

If the application requires the pull-up during configuration to be disabled, this can be achieved by removing R222 component and by mounting R221. In this configuration, the PUDC pin is connected to 1.8 V.

Figure 12 illustrates the configuration of the I/O signals during power-up. Figure 13 indicates the location of the pull-up/pull-down resistors on the module PCB - lower right part on the bottom view drawing.

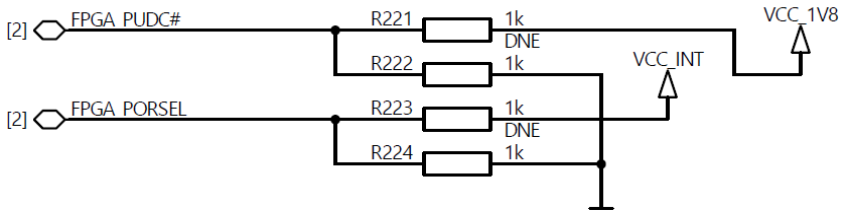

Figure 12: Pull-Up During Configuration (PUDC) and Power-on Reset Delay Override (PORSEL)

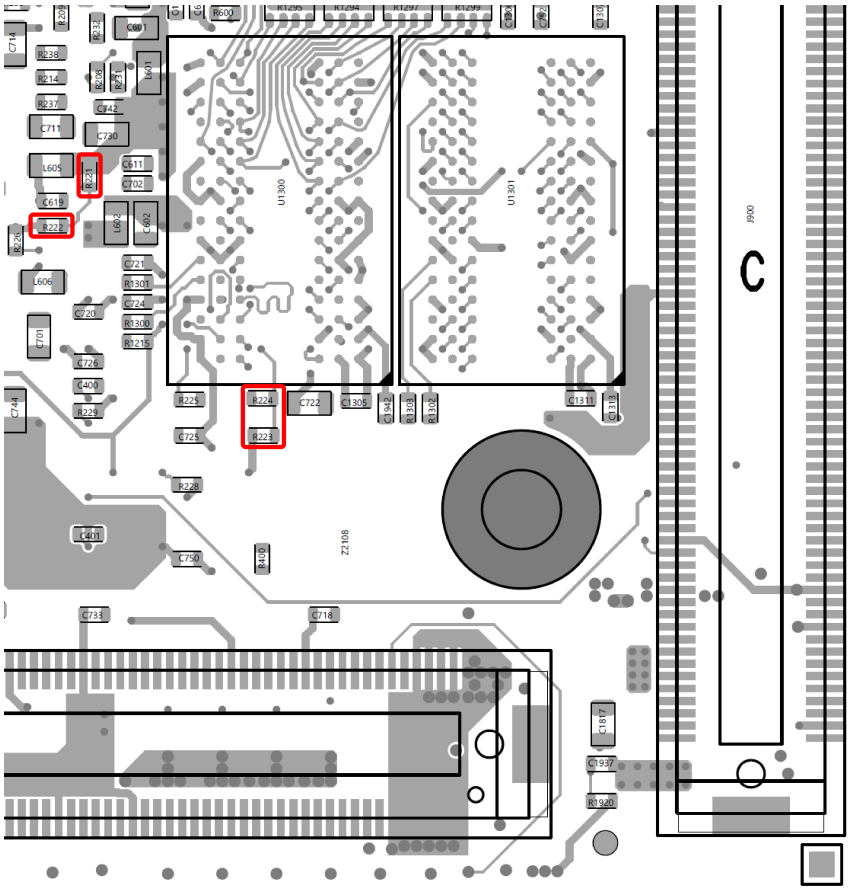

Figure 13: Pull-Up During Configuration (PUDC) and Power-on Reset Delay Override (PORSEL) Resistors - Assembly Drawing Bottom View (lower right part)

For details on the PUDC signal, refer to the Zynq UltraScale+ MPSoC Technical Reference Manual [22].

3.4 Power-on Reset Delay Override

The power-on reset delay override MPSoC signal (POR_OVERRIDE) is pulled to ground on the module, setting the PL power-on delay time to the default standard time.

If the application requires faster PL power-on delay time, this can be achieved by removing R224 component and by mounting R223.

Figure 12 illustrates the configuration of the POR_OVERRIDE signal. Figure 13 indicates the location of the pull-up/pull-down resistors on the module PCB - lower right part on the bottom view drawing.

For details on the POR_OVERRIDE signal, refer to the Zynq UltraScale+ MPSoC Technical Reference Manual [22].

3.5 Boot Mode

The boot mode can be selected via two signals available on the module connector.

Table 37 describes the available boot modes on the Mercury+ XU9 SoC module.

BOOT MODE1	BOOT MODE0	Mode Straps [3:0]	Description	Comment
0	0	0110	Boot from eMMC flash	-
0	1	1110	Boot from SD card (with an external SD 3.0 compliant level shifter; only available when VCC_CFG_MIO is 1.8 V)	Not supported (may be supported in the future)
1	0	0010	Boot from QSPI flash	-
1	1	0101	Boot from SD card (default mode)	-
1	0	0000	JTAG boot mode	Available only in certain conditions (refer to Section 3.6.3 for details).

Table 37: Boot Modes

3.6 JTAG

The Zynq UltraScale+ devices include two separate JTAG controllers: the Zynq UltraScale+ TAP and the ARM DAP. The first one uses the PS dedicated JTAG pins and has access to both PS and PL and the second one uses the PS PJTAG pins and is used for loading programs, system test, and PS debug.

Details on JTAG and on system test and debug are available in the Zynq UltraScale+ MPSoC Technical Reference Manual [22].

Certain AMD tool versions support QSPI flash programming via JTAG only when JTAG boot mode is used. Alternatively, the QSPI flash can be programmed in u-boot or Linux by the SPI controller in the PS or from an SPI external master.

3.6.1 JTAG on Module Connector

The PL and the PS JTAG interfaces are connected into one single chain available on the module connector. The PS_JTAG pins are used by the Zynq UltraScale+ TAP controller. The controller has full functionality only after the PS boot is complete. In order to enable the ARM DAP controller, special commands must be sent to the Zynq UltraScale+ TAP.

The MPSoC device and the flash devices can be configured via JTAG from AMD Vivado Hardware Manager or AMD Vitis. For this operation, the ARM DAP must be enabled.

Signal Name	Module Connector Pin	PS Dedicated Pin	Comment
JTAG_TCK	A123	PS_JTAG_TCK	10 kΩ pull-up to VCC_CFG_MIO
JTAG_TMS	A119	PS_JTAG_TMS	10 kΩ pull-up to VCC_CFG_MIO
JTAG_TDI	A117	PS_JTAG_TDI	10 kΩ pull-up to VCC_CFG_MIO
JTAG_TDO	A121	PS_JTAG_TDO	10 kΩ pull-up to VCC_CFG_MIO

Table 38: JTAG Interface - PL and PS Access and Debug

3.6.2 External Connectivity

The JTAG signals can be connected to a JTAG connector on the base board. No pull-up/pull-down resistors are necessary. The VREF pin of the programmer must be connected to VCC_CFG_MIO.

It is recommended to add series termination resistors between the module and the JTAG header, close to the source. Enclustra also recommends adding a transient-voltage-suppression diode close to the JTAG connector to protect the MPSoC from damage due to ESD (Electrostatic Discharge). Refer to the Enclustra Module Pin Connection Guidelines for details on JTAG interface.

3.6.3 JTAG Boot Mode

Support for JTAG boot mode has been implemented on the Mercury+ XU9 SoC module to increase the usability of the module with AMD tools, for example for QSPI flash programming or FPGA bitstream loading.

> **Tip**
>
> JTAG boot mode is used explicitly for initial booting and is not required for the general JTAG mode used for programming, debugging, and in-system testing.

The following steps are required in order to boot the module in JTAG mode:

1. Set the boot mode selection signals for QSPI boot.
2. While powering-up the module, short-circuit R252 (see Figure 14). This allows to sample the MPSoC boot selection pins correctly for JTAG boot mode.

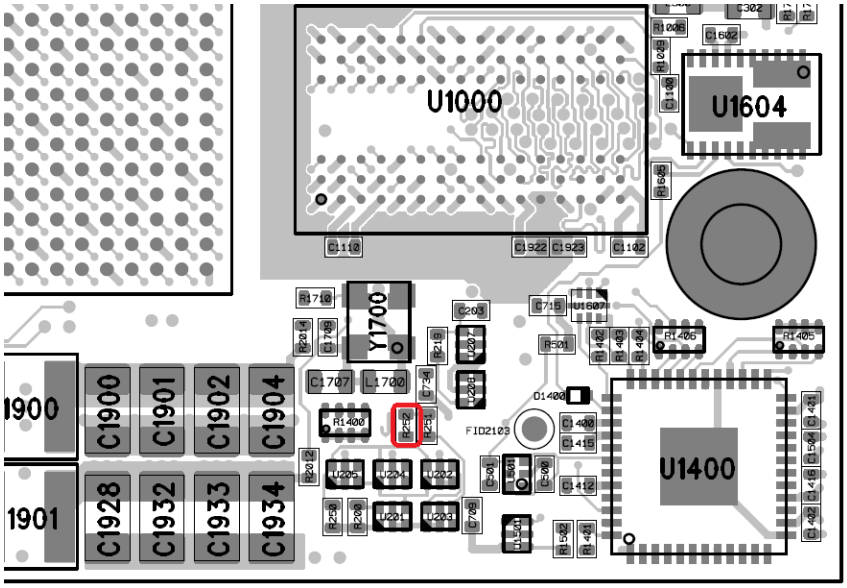

Figure 14: JTAG Boot Mode Resistor - Assembly Drawing Top View (lower right part)

3.7 eMMC Boot Mode

In the eMMC boot mode, the PS boots from the eMMC flash located on the module. The flash device is connected to the PS MIO pins 13 to 22 for 8-bit data transfer mode.

3.8 QSPI Boot Mode

In the QSPI boot mode, the PS boots from the QSPI flash located on the module. The flash device is connected to the PS MIO pins 0 to 5.

3.9 SD Card Boot Mode

In the SD card boot mode the PS boots from the SD card located on the base board. There are two SD card boot modes available on the Mercury+ XU9 SoC module. The SD boot mode with level shifter is currently not supported.

The SD boot mode with level shifter is used with Ultra High Speed (UHS) SD cards. The controller will start the communication at 3.3 V and afterwards it will command the card to drop from 3.3 V operation to 1.8 V operation. For this mode, an external SD 3.0 compliant level shifter is required. This boot mode may be supported in the future by Enclustra modules and base boards.

Two SD card boot modes are available on the Mercury+ XU9 SoC module, as described in Table 37.
For the SD card boot mode, the following requirements must be met:

- The SD card must be connected to MIO pins 45 to 51.
- A Zynq boot image must be generated from an MPSoC design having the SDIO controller enabled.
- The boot image must be named “boot.bin” and then copied to the SD card.
- The SDIO controller must be fed with a reasonable clock frequency. Refer to the reference design for guidelines on SDIO settings.

For details on SD card boot, refer to the Zynq UltraScale+ MPSoC Technical Reference Manual [22].

3.10 eMMC Flash Programming

The eMMC flash can be formatted and/or programmed in u-boot or Linux, like a regular SD card. The boot image or independent partition files can be transmitted via Ethernet or copied from another storage device.

Certain AMD tool versions support eMMC flash programming via JTAG.

3.11 QSPI Flash Programming via JTAG

The AMD Vivado and Vitis software offer QSPI flash programming support via JTAG.

Certain AMD tools versions support QSPI flash programming via JTAG only when JTAG boot mode is used. For more information, refer to the Zynq UltraScale+ MPSoC Technical Reference Manual [22]. Alternatively, the QSPI flash can be programmed in u-boot or Linux by the SPI controller in the PS or from an SPI external master.

3.12 QSPI Flash Programming from an External SPI Master

The signals of the QSPI flash are directly connected to the module connector for flash access. As the flash signals are connected to the MPSoC device as well, the MPSoC device pins must be tri-stated while accessing the QSPI flash directly from an external device. This is ensured by pulling the PS_SRST# signal to ground followed by a pulse on PS_POR#, which puts the MPSoC device into reset state and tri-states all I/O pins. PS_SRST# must be low when PS_POR# is released and kept low until the flash programming has finished. Afterwards, all SPI signals and PS_SRST# must be tri-stated and another reset impulse must be applied to PS_POR#.

Signal Name	MPSoC Pin	Mod. Conn. Pin	Description	Comment
FLASH_CLK	MIO[0]	A118	SPI CLK	10 kΩ pull-up to VCC_CFG_MIO
FLASH_DO	MIO[1]	A122	SPI MISO	-
FLASH_DI	MIO[4]	A114	SPI MOSI	10 kΩ pull-up to VCC_CFG_MIO
FLASH_CS#	MIO[5]	A116	SPI CS#	10 kΩ pull-up to VCC_CFG_MIO

Table 39: QSPI Flash Signals for External Access

Figure 15 shows the signal diagrams corresponding to flash programming from an external master.

In addition, a non-QSPI boot mode must be used during QSPI flash programming, otherwise the MPSoC device will attempt to boot from the flash and will disturb the clock.

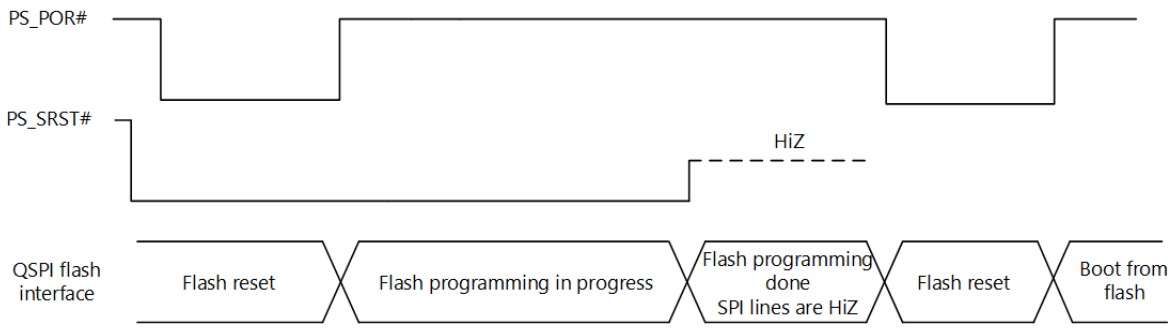

Figure 15: QSPI Flash Programming from an External SPI Master - Signal Diagrams

NOTICE

Damage to the device

The module can be damaged if the QSPI flash signals are driven simultaneously by the module and the base board.

- While accessing the QSPI flash from the module connector, put the MPSoC device into reset and select a non-QSPI boot mode.

3.13 Enclustra Module Configuration Tool

In combination with an Enclustra base board, the QSPI flash can be programmed using Enclustra Module Configuration Tool (MCT) [19]. For this method, a non-QSPI boot mode must be used during QSPI flash programming. The entire procedure is described in the reference design documentation.

The AMD Zynq devices do not support slave serial configuration, therefore only flash programming is supported by the Enclustra MCT for the Mercury+ XU9 SoC module.

4 I2C Communication

4.1 Overview

The I2C bus on the Mercury+ XU9 SoC module is connected to the MPSoC device and to the EEPROM, and is available on the module. This allows external devices to read the module type and to connect more devices to the I2C bus.

The I2C clock frequency should not exceed 400 kHz.

Tip

Maximum I2C speed may be limited by the routing path and additional loads on the base board.

Tip

If the I2C traces on the base board are very long, 100 Ω series resistors should be added between the module and the I2C device on the base board.

4.2 Signal Description

Table 40 describes the signals of the I2C interface. The pins are connected to both PS and PL.

All signals must be connected to open collector outputs and must not be driven high from any source. I2C_INT# is an input to the MPSoC and must not be driven from the MPSoC device.

Level shifters are used between the I2C bus and MPSoC pins, as I/O banks 500 and 64 are supplied with 1.8 V and 1.2 V respectively. Make sure that all pins are configured correctly and no pull-down resistors are enabled.

Signal Name	PS Pin	PL Package Pin	Connector Pin	Comment
I2C_SDA	MIO[11]	AH13	A113	2.2 kΩ pull-up to VCC_3V3
I2C_SCL	MIO[10]	AB13	A111	2.2 kΩ pull-up to VCC_3V3
I2C_INT#	MIO[12]	-	A115	4.7 kΩ pull-up to VCC_3V3

Table 40: I2C Signal Description

4.3 I2C Address Map

Table 41 describes the addresses for several devices connected on I2C bus. For details on the EEPROM characteristics, refer to Section 2.24.

Address (7-bit)	Description	Assembly Variant
0x64	Secure EEPROM	Default
0x5C	Secure EEPROM	Custom

Table 41: I2C Addresses

4.4 Secure EEPROM

The secure EEPROM is used to store the module serial number and configuration. An example demonstrating how to read the module information from the EEPROM memory is included in the Mercury+ XU9 SoC module reference design.

> **Tip**
>
> Any attempt to write data to the secure EEPROM causes the warranty to be rendered void.

4.4.1 Memory Map

Address	Length (bits)	Description
0x00	32	Module serial number
0x04	32	Module product information
0x08	40	Module configuration
0x0D	24	Reserved
0x10	48	Ethernet MAC address
0x16	48	Reserved
0x1C	32	Checksum (only for DS28CN01 EEPROM type)

Table 42: EEPROM Sector 0 Memory Map

Module Serial Number

The module serial number is a unique 32-bit number that identifies the module. It is stored using big-endian byte order (MSB on the lowest address).

Module Product Information

This field indicates the type of module and hardware revision.

Module	Product Series	Reserved	Revision	Product Information
Mercury+ XU9 SoC module	0x0336	0x[XX]	0x[YY]	0x0336 [XX][YY]

Table 43: Product Information

Module Configuration

Addr.	Bits	Description	Min. Value	Max. Value	Comment
0x08	[7:4]	MPSoC type	0	3	See Table 45
	[3:0]	MPSoC device speed grade	1	3	
0x09	[7:6]	Temperature range	0	2	See Table 46
	[5]	Power grade	0 (Normal)	1 (Low power)	
	[4:3]	Gigabit Ethernet port count	0	2	
	[2]	RTC equipped	0	1	
	[1:0]	Reserved	-	-	
0x0A	[7:2]	Reserved	-	-	
	[1:0]	USB 2.0 port count	0	2	
0x0B	[7:4]	DDR4 ECC RAM (PS) size (GB)	0 (0 GB)	4 (8 GB)	Resolution = 1 GB
	[3:0]	DDR4 RAM (PL) size (GB)	0 (0 MB)	4 (8 GB)	Resolution = 1 GB
0x0C	[7:4]	eMMC flash size (GB)	0 (0 GB)	5 (16 GB)	Resolution = 1 GB
	[3:0]	QSPI flash memory size (MB)	0 (0 MB)	7 (64 MB)	Resolution = 1 MB

Table 44: Module Configuration

The memory sizes are defined as Resolution$\times 2^{(\text{Value}-1)}$, for example:

- DRAM = 0: none
- DRAM = 1: 1 GB
- DRAM = 2: 2 GB
- DRAM = 3: 4 GB

Table 45 shows the available MPSoC types.

Value	MPSoC Device Type
0	XCZU4CG
1	XCZU4EV
2	XCZU5EV
3	XCZU7EV

Table 45: MPSoC Device Types

Table 46 shows the available temperature ranges.

Value	Module Temperature Range
0	Commercial
1	Extended
2	Industrial

Table 46: Module Temperature Range

Ethernet MAC Address

The Ethernet MAC address is stored using big-endian byte order (MSB on the lowest address). Each module is assigned two sequential MAC addresses; only the lower one is stored in the EEPROM.

5 Operating Conditions

5.1 Absolute Maximum Ratings

Table 47 indicates the absolute maximum ratings for Mercury+ XU9 SoC module. The values given are for reference only. For details, refer to the Zynq UltraScale+ MPSoC Data Sheet: DC and AC Switching Characteristics [24].

Parameter	Description	Min.	Max.	Unit
VCC_MOD	Supply voltage relative to ground	-0.5	16.0	V
VCC_BAT	Supply voltage for MPSoC battery-backed RAM and battery-backed RTC	0.0	6.0	V
VCC_IO_BN VCC_IO_BO	I/O bank supply voltage relative to ground (V_{CCO})	-0.5	3.4	V
VCC_CFG_MIO	I/O bank supply voltage relative to ground (V_{CCO_PSIO})	-0.5	3.63	V
IO_B[x]_<...>	I/O signal lines input voltage relative to ground (V_{IN})	-0.5	V_{CCO}+0.5	V
PS_MIO[x]_<...>	PS I/O signal lines input voltage relative to ground (V_{IN_PSIN})	-0.5	V_{CCO_PSIO}+0.55	V
Temperature[14]	Temperature range for extended temperature modules (E)	0	+85	°C
	Temperature range for industrial modules (I)	-40	+85	°C

Table 47: Absolute Maximum Ratings

NOTICE

Damage to the device due to overheating

Depending on the user application, the Mercury+ XU9 SoC module may consume more power than can be dissipated without additional cooling measures.

- Ensure that the MPSoC is always adequately cooled by installing a heat sink and/or providing air flow.

[14] The components used on the hardware are specified for the relevant temperature range. The user must provide adequate cooling in order to keep the temperature of the components within the specified range.

5.2 Recommended Operating Conditions

Table 48 indicates the recommended operating conditions for Mercury+ XU9 SoC module. The values given are for reference only. For details, refer to the Zynq UltraScale+ MPSoC Data Sheet: DC and AC Switching Characteristics [24].

Parameter	Description	Min.	Typ.	Max.	Unit
VCC_MOD	Supply voltage relative to ground	5.0	12.0	15.0	V
VCC_BAT	Supply voltage for MPSoC battery-backed RAM and battery-backed RTC	2.0[16]	–	5.5	V
VCC_IO_B[x]	I/O bank supply voltage relative to ground (V_{CCO})	Refer to Section 2.8.5			
VCC_CFG_MIO	I/O bank supply voltage relative to ground (V_{CCO_PSIO})				
IO_B[x]_<...>	I/O signal lines input voltage relative to ground (V_{IN})	-0.2	–	V_{CCO}+0.2	V
PS_MIO[x]_<...>	PS I/O signal lines input voltage relative to ground (V_{IN_PSIN})	-0.2	–	V_{CCO_PSIO}+0.2	V
Temperature[15]	Temperature range for extended temperature modules (E)	0	–	+85	°C
	Temperature range for industrial modules (I)	-40	–	+85	°C

Table 48: Recommended Operating Conditions

NOTICE

Damage to the device due to overheating

Depending on the user application, the Mercury+ XU9 SoC module may consume more power than can be dissipated without additional cooling measures.

- Ensure that the MPSoC is always adequately cooled by installing a heat sink and/or providing air flow.

[15] The components used on the hardware are specified for the relevant temperature range. The user must provide adequate cooling in order to keep the temperature of the components within the specified range.

[16] For revisions prior to R3.0, the minimum value is 2.7 V.

6 Ordering and Support

6.1 Ordering

Use the Enclustra online request/order form for ordering or requesting information:
http://www.enclustra.com/en/order/

6.2 Support

Follow the instructions on the Enclustra online support site:
http://www.enclustra.com/en/support/

List of Figures

1 Hardware Block Diagram . . . 11
2 Product Model Fields . . . 12
3 Product Label . . . 13
4 Module Top View . . . 15
5 Module Bottom View . . . 15
6 Module Top Assembly Drawing . . . 16
7 Module Bottom Assembly Drawing . . . 16
8 Model Footprint and Dimensions - Top View and Side View . . . 17
9 Pin Numbering for the Module Connector . . . 19
10 Power-Up Sequence - VCC_IO in Relation with PWR_GOOD and PWR_EN Signals . . . 24
11 USB 3.0 Implementation Example . . . 44
12 Pull-Up During Configuration (PUDC) and Power-on Reset Delay Override (PORSEL) . . . 47
13 Pull-Up During Configuration (PUDC) and Power-on Reset Delay Override (PORSEL) Resistors - Assembly Drawing Bottom View (lower right part) . . . 47
14 JTAG Boot Mode Resistor - Assembly Drawing Top View (lower right part) . . . 50
15 QSPI Flash Programming from an External SPI Master - Signal Diagrams . . . 52

List of Tables

1 Standard Module Configurations . . . 12
2 EN-Numbers and Product Models . . . 14
3 Mechanical Data . . . 18
4 Module Connector Characteristics . . . 18
5 Mapping Between the Generic I/O Bank Letters and the Device-Specific I/O Bank Numbers 19
6 User I/Os . . . 20
7 I/O Pin Exceptions - PERST# . . . 20
8 I/O Pin Exceptions - Level Shifters . . . 21
9 I/O Banks . . . 23
10 VCC_IO Pins . . . 23
11 MIO Pins Connections Overview . . . 26
12 System Monitor (PL) Parameters . . . 27
13 Mapping Between the Generic GTH Bank Letters and the Device-Specific GTH Bank Numbers 28
14 MGT Pairs . . . 28
15 Generated Power Supplies . . . 30
16 Module Power Status and Control Pins . . . 31
17 Voltage Supply Inputs . . . 31
18 Voltage Supply Outputs . . . 32
19 Heat Sink Characteristics . . . 33
20 Voltage Monitoring Outputs . . . 34
21 Module Clock Resources . . . 34
22 Reset Resources . . . 35
23 User LEDs . . . 35
24 Status LEDs . . . 36
25 DDR4 SDRAM (PS) Characteristics . . . 36
26 DDR4 SDRAM (PS) Parameters . . . 37
27 DDR4 SDRAM (PL) Characteristics . . . 38
28 DDR4 SDRAM (PL) Parameters . . . 38
29 QSPI Flash Characteristics . . . 39
30 Gigabit Ethernet PHYs Characteristics . . . 40
31 USB1/ETH1 Selection . . . 41
32 Gigabit Ethernet PHYs Configuration - Bootstraps . . . 42
33 Gigabit Ethernet PHYs Configuration - RGMII Delays . . . 42

34 USB 2.0 PHY Characteristics . . . 43
35 EEPROM Characteristics . . . 45
36 MPSoC Configuration Pins . . . 46
37 Boot Modes . . . 48
38 JTAG Interface - PL and PS Access and Debug . . . 49
39 QSPI Flash Signals for External Access . . . 51
40 I2C Signal Description . . . 53
41 I2C Addresses . . . 53
42 EEPROM Sector 0 Memory Map . . . 54
43 Product Information . . . 54
44 Module Configuration . . . 55
45 MPSoC Device Types . . . 55
46 Module Temperature Range . . . 56
47 Absolute Maximum Ratings . . . 57
48 Recommended Operating Conditions . . . 58

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