UCC25660x Family 750kHz Wide V_{IN}/V_{OUT} Range LLC Controller Optimized for Light-Load Efficiency

1 Features

- 50kHz to 750kHz full-load switching frequency
- IPPC control enables wide input and output LLC (WLLC) operation
- Enhanced light load management:
  - High frequency pulse skip for improved light load efficiency
  - Low frequency burst for low standby power
  - Audible frequency range skip for reduced audible noise
  - Integrated PFC on/off control signal to help further reduce standby power
- Internal resonant-capacitor voltage synthesizer for enhanced signal reliability and high startup frequency support
- Automatic capacitive region avoidance
- Adaptive soft start with minimized inrush current
- Integrated high-voltage startup (UCC256601, UCC256602, and UCC256604)
- X-capacitor discharge (UCC256601 and UCC256604).
- Integrated +0.6/-1.2A gate drive
- Complete protections
  - 50ns Over-Current Protection (OCP) - cycle-by-cycle current limit
  - Over-Voltage Protection (OVP), internal and external Over-Temperature Protection (OTP)
  - Input and VCCP UVLO with internal 19V VCCP Clamp
- SOIC-14 package with removed pins for high-voltage clearance

2 Applications

- SMPS power supply for TV
- Industrial AC and DC
- Lighting and battery chargers
- Notebook and gaming console adapter
- Medical power supply
- PC power supply

3 Description

The UCC25660x family is a high-frequency LLC controller implementing Input-Power Proportional Control (IPPC) scheme, along with an enhanced light-load management and multiple protection features.

IPPC widens the control range of the LLC converter simplifies the design of wide input and output-voltage range applications such as LED drivers, battery chargers. It can even work without a PFC for non-universal input applications.

The UCC25660x family's enhanced light-load management improves while minimizing audible noise. To minimize standby power, the UCC25660x family can directly disable the PFC controller when operating in burst mode.

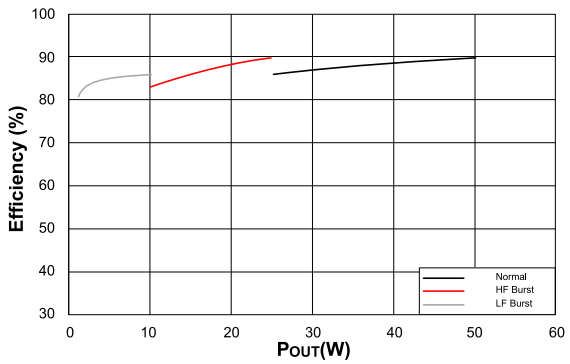
The automatic capacitive region avoidance scheme along with the adaptive soft start with reverse recovery avoidance scheme ensures that the device can never work in a mode where there is a potential to damage the FET's. This scheme makes the controller ideal for working with a pre-biased load.

The UCC25660x family comes with robust protection to help you design a reliable power supply. The UCC25660x family has options supporting high-voltage startup, X-capacitor (X-cap) discharge, OVP response, and extended Gain range. See details in the device comparison table.

Device Information

PART NUMBER	PACKAGE	BODY SIZE (NOM)
UCC25660x family	SOIC	9.9mm x 3.9mm

1. For all available packages, see the orderable addendum at the end of the data sheet.



Typical Efficiency Curve

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Device Comparison Table

Orderable Part Number	Integrated High-Voltage Startup	Integrated X-Capacitor Discharge	PFC On/Off during LF Burst	Extended Gain Range	Output-Voltage (OVP) Latch	I_{FB} Typical Value (uA)	$R_{FBInternal}$ Typical Value (kΩ)
UCC256601	Yes	Yes	No	No	Yes	80	100
UCC256602	Yes	No	No	No	No	160	50
UCC256603	No	No	No	No	No	160	50
UCC256604	Yes	Yes	Yes	Yes	No	80	100

5 Pin Configuration and Functions

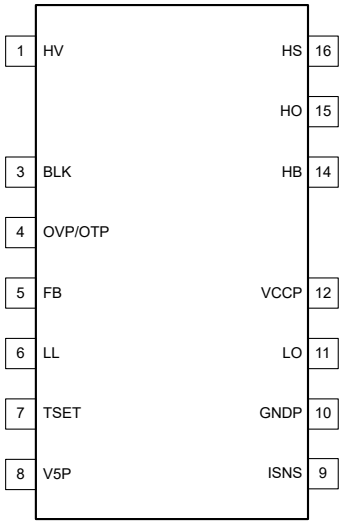

Figure 5-1. DDB Package 16-Pin SOIC (Pins 2, 13 removed) Top View

Table 5-1. Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
HV	1	I	High-voltage (HV) Startup and X-Capacitor Discharge. This pin is used to to perform HV startup. After startup is completed, the HV pin is used for AC presence detection and X-Capacitor discharge. This pin is connected to the rectified AC line (for UCC256601 and 604) or input bulk capacitor (for UCC256602).
	2	-	Missing. HV spacer for creepage between high voltage and low voltage pins
BLK	3	I	Bulk input UVLO/OVLO and input voltage feedforward. This pin is connected to a resistor divider that looks at bulk capacitor voltage.
OVP/OTP	4	I	Overvoltage protection and external overtemperature protection. This pin connects through an NTC resistor to ground and to a Zener diode that connects to VCC
FB	5	I	Feedback signal. This pin is connected to the collector of an opto-coupler. This pin is for feedback input.
LL	6	I	Light load operation options and burst mode threshold setting. This pin is connected to an external resistor divider. The top resistor of the divider is connected to V5P. The impedance and voltage of this pin is used to select the theresholds for high frequncy and low frequency burst mode operation .

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Table 5-1. Pin Functions (continued)

PIN		I/O	DESCRIPTION
NAME	NO.		
TSET	7	I/O	This pin is used to program the internal resonant tank current integrator (VCR synthesizer) time constant and minimum switching frequency. Depending on the option programmed, the maximum deadtime is also selected. After the programming phase ends, TSET pin provides PFC on/off signal in the UCC256604 variant.
V5P	8	P	5V bias. This pin is externally connected to a decoupling capacitor to GNDP.
ISNS	9	I	Resonant current sensing. This pin senses the differentiated resonant capacitor voltage.This signal is internally used to: 1. Generate the control signal. 2. OCP & Cycle-by-Cycle current limiting. 3. Capacitive region avoidance.
GNDP	10	P	This pin is connected to primary-side bulk capacitor negative terminal
LO	11	O	Low-side gate driver output.
VCCP	12	P	IC supply voltage This pin is connected to a decoupling capacitor. For applications including a bias winding on the LLC transformer, the VCC pin is connected through a diode to the bias winding. For applications where HV startup is disabled, VCCP is supplied by an auxilliary bias supply. The VCCP pin is internally clamped to 19V.
	13	N/A	Missing pin. High-voltage spacer for creepage between high-voltage and low-voltage pins.
HB	14	P	High-side gate driver bias. A capacitor connecting between HB and HS provides the high-side driver energy.
HO	15	O	High-side gate driver output.
HS	16	P	High-side gate driver return. This pin is connected to the switch node of the half-bridge structure in the LLC power stage.

Please refere to section 8.2 Typical Application for more details.

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6 Specifications

6.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted), all voltages are with respect to GND, currents are positive into and negative out of the specified terminal.(1)

		MIN	MAX	UNIT
Input voltage	HV, HB	-0.3	700	V
	ISNS	-6.5	6.5	V
	BLK, LL, TSET	-0.55	5.5	V
	HB - HS	-0.3	25	V
	VCCP	-0.55	30	V
	OVP/OTP	-0.55	5.5	V
5V	DC	-0.55	5.5	V
HO output voltage	DC	HS – 0.3	HB + 0.3	V
	Transient, less than 100 ns	HS – 2	HB + 0.3	
LO output voltage	DC	-0.3	VCCP+ 0.3	V
	Transient, less than 100 ns	-2	VCCP + 0.3	
Floating ground slew rate	dV_{HS}/dt	-200	200	V/ns
HO, LO pulsed current	I_{OUT_PULSED}	-0.6	1.2	A
Junction temperature range	T_J	-40	150	°C
Storage temperature range, T_{stg}	T_{stg}	-65	150	
Lead temperature	Soldering, 10 second		300	
	Reflow		260	

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, HV, HO, HS, HB pins(1)	±1000	V
		Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all other pins(1)	±2000	
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

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6.3 Recommended Operating Conditions

All voltages are with respect to GND, -40°C < T_J = T_A < 125°C, currents are positive into and negative out of the specified terminal, unless otherwise noted.

		MIN	NOM	MAX	UNIT
HV, HS	Input voltage			640	V
V_{VCCP}	Supply voltage		15	18.5	V
HB - HS	Driver bootstrap voltage	10	14	17.5	V
C_B	Ceramic bypass capacitor from HB to HS	0.1		5	µF
C_{VCCP}	VCCP pin decoupling capacitor	33		470	µF
$I_{VCCPMAX}$	Maximum input current of VCCP			100	mA
T_A	Operating ambient temperature	-40		125	°C

6.4 Thermal Information

THERMAL METRIC(1)		UCC25640x D (SOIC) 14 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	74.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	30.7	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	31.8	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	4.4	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	31.4	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report, SPRA953.

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6.5 Electrical Characteristics

All voltages are with respect to GND, -40°C< T_J =T_A < 125°C, VCC =15V, currents are positive into and negative out of the specified terminal, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY VOLTAGE						
VCC_{Short}	Below this threshold, use reduced start up current		0.6	1	1.4	V
$VCC_{ReStartJfet}$	Below this threshold, re-enable JFET.			10.2		V
$VCC_{ReStart}$	HV startup is re-enabled when VCC is below this level during startup phase		12.5	13	13.5	V
$VCC_{StartSelf}$	Startup when VCC is above this level		13.5	14	14.5	V
$VCC_{StartExt}$	Startup when VCC is above this level		10.5	10.9	11.3	V
$VCC_{StopSwitching}$	Switching Stopped below this threshold		9	9.5		V
VCC_{UVLOr}	VCC under voltage lockout voltage (rising)		7.25	7.5	7.75	V
VCC_{UVLOf}	VCC under voltage lockout voltage hysteresis		6.5	6.8	7.1	V
VCC_{Hold_r}	Jfet Stop voltage during startup programming phase		7.9	8.2	8.5	V
VCC_{Hold_f}	Jfet Start voltage during startup programming phase		7.65	7.9	8.15	V
VCC_{Shunt}	VCC internal clamp voltage			19		V
$IVCC_{Clamp}$	VCC internal clamp current			15		mA
VCC_OV	VCC OVP threshold			20.5		V
SUPPLY CURRENT						
$I_{CCSleep}$	Current drawn from VCC rail during burst off period			800		µA
I_{CCRun}	Current drawn from VCC Pin while gate is switching. Excluding Gate Current	Dead time = 1µs maximum dead time		8		mA
$I_{CCLatchFault}$	Current drawn from VCC pin in latched fault state (1)	For UCC256601			1	mA
REGULATED SUPPLY						
V5P	Regulated supply voltage(1)	no load	4.75	5	5.25	V
	Regulated supply voltage	10mA load	4.75	5	5.25	V
$V5P_{UVLO}$	V5P under voltage lock out voltage(1)			4		V
$I_{V5PStartupCurrLimit}$	Max current that can be drawn on the pin when VCCP< $VCC_{StartSelf}$ (1)			6		mA
$I_{V5PCurrLimit}$	V5P at IV5P =15mA (1)	VCCP=15V	10.2			mA

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All voltages are with respect to GND, -40°C< T_J =T_A < 125°C, VCC =15V, currents are positive into and negative out of the specified terminal, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
HIGH VOLTAGE STARTUP						
$I_{VCC_Charge_Low}$	Reduced VCCP charge current from HV Pin	V_{HV} = 20V, VCC = 0V, For UCC256601,UCC256602,UCC256604	0.23	0.44	0.65	mA
$I_{VCC_Charge_High}$	Full VCCP charge current	V_{HV} = 20V, VCC = 4V, For UCC256601,UCC256602,UCC256604	7.5	10	13.8	mA
I_{HVZCD}	Highest AC zero crossing detection test current	For UCC256601,UCC256604		0.625		mA
$I_{XCAPDischarge}$	X-cap discharge current	For UCC256601,UCC256604	8.7	11.5	13.5	mA
$V_{zero\text{-}crossing}$	HV pin voltage threshold that zero-crossing is detected	For UCC256601,UCC256604	8	9	11	V
$t_{XCAPZCD}$	AC zero crossing detection window length for first four test current stage (1)	For UCC256601,UCC256604	10	12	14	ms
$t_{XCAPZCDLast}$	AC zero crossing detection window length for final test current stage (1)	For UCC256601,UCC256604		36		ms
$t_{XCAPIdle}$	AC zero crossing detection idle period length (1)	For UCC256601,UCC256604		700		ms
$t_{XCAPDischarge}$	Time for X-cap discharge current active (1)	For UCC256601,UCC256604		360		ms
$t_{XCAPJFETON}$	Time of first X-cap detection after JFETON (1)	For UCC256601,UCC256604		12		ms
I_{XCAP_I0}	X-Cap test current I0	For UCC256601,UCC256604		125		uA
I_{XCAP_Idel1}	X-Cap test current I1	For UCC256601,UCC256604		125		uA
I_{XCAP_Idel1}	X-Cap test current I2	For UCC256601,UCC256604		250		uA
I_{XCAP_Idel1}	X-Cap test current I3	For UCC256601,UCC256604		375		uA
BULK VOLTAGE SENSE						
$V_{BLKStartHys}$	BLK voltage that allows LLC to start switching (1)		0.09	0.1	0.11	V
$V_{BLKStop}$	BLK voltage that forces LLC operation to stop		0.98	1	1.02	V
I_{BLKHys}	BLK hysteresis current			5		µA
$t_{BLKStopDC}$	BLK shut down duration(1)		12	14	16	µs

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PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
FEEDBACK PIN						
$R_{FBInternal}$	Internal pull down resistor value	For UCC256601, UCC256604	85	100	115	kΩ
$R_{FBInternal}$	Internal pull down resistor value	For UCC256602, UCC256603	42.5	50	57.5	kΩ
I_{FB}	FB internal current source	For UCC256601, UCC256604	68	80	92	µA
I_{FB}	FB internal current source	For UCC256602, UCC256603	136	160	184	µA
V_{FB}	FB pin voltage when FB pin sink current is at (I_{FB} - 50 µA)	Iopto = 0.37 * IFB	3.3	3.5	3.7	V
ΔV_{FB}	FB pin voltage variation when FB pin sink current ranges from (Iopto = 0.37*IFB to Iopto = 0.94*IFB)				0.6	V
ΔV_{clamp}	FB pin voltage variation when FB pin sink current ranges from (Iopto = 0.94*IFB) to (Iopto = 1.06*IFB)	(Iopto = 0.94*IFB) to (Iopto = 1.06*IFB)	0.3			V
$I_{FBclamp}$	Maximum FB internal current source when FB is clamped	For UCC256601, UCC256604	75	87.5	100	µA
$I_{FBclamp}$	Maximum FB internal current source when FB is clamped	For UCC256602, UCC256603	150	175	200	µA
$\Delta V_{FBclamp}$	FB pin voltage variation when FB pin sink current ranges from (Ilopto = 1.06IFB) to (Ilopto = IFB + 0.94*IFBClamp)	(Ilopto = 1.06IFB) to (Ilopto = IFB + 0.94*IFBClamp)			0.5	V
f_{-3dB}	Feedback chain -3 dB cut off frequency (2)	FBReplica from 4.5V to 0.5V	1			MHz
V_{FBOLP}	OLP protection(1)			4.75		V
T_{OLP}	OLP protection time (1)			100		ms
RESONANT CURRENT SENSE						
V_{ISNS_OCP}	OCP threshold	For TSET option >2.5V (1)	3.9	4	4.1	V
V_{ISNS_OCP}	OCP threshold	For TSET option <2.5V	3.4	3.5	3.6	V
$V_{ISNS_OCP_SS}$	OCP threshold during soft start		2.9	3	3.1	V
n_{OCP}	Number of OCP cycles before OCP fault is tripped (1)			7		
n_{OCP_SS}	Number of OCP cycles before OCP fault is tripped at startup(2)			50		
$V_{IpolarityHyst}$	ISNS Polarity comparator hysterisis			40		mV
V_{ISNS_ZCS}	ZCS comparator +Ve threshold after Soft Start			100		mV
V_{ISNS_ZCSn}	ZCS comparator -Ve threshold, after Soft Start			-100		mV
$V_{ISNS_MINCURR_SS}$	+Ve ISNS threshold during Soft Start			50		mV
$V_{ISNS_MINCURR_SSn}$	-Ve ISNS threshold during Soft Start			-50		mV
t_{leb}	Leading edge blanking for ZCS & OCP1 comparators(1)			250		ns
$TZCS_{Fault}$	Fault detected when ZCS event persisits for the idicated time(2)	ZCS Event persists		10		ms

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All voltages are with respect to GND, -40°C< T_J =T_A < 125°C, VCC =15V, currents are positive into and negative out of the specified terminal, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
GATE DRIVER						
V_{LOL}	LO output low voltage	I_{sink} = 20mA			0.12	V
V_{RVCC} - V_{LOH}	LO output high voltage	I_{source} = 20mA			0.3	V
V_{HOL} - V_{HS}	HO output low voltage	I_{sink} = 20mA			0.12	V
V_{HB} - V_{HOH}	HO output high voltage	I_{source} = 20mA			0.35	V
$V_{HB-HSUVLOFall}$	High side gate driver UVLO falling threshold		6.6	7.25	8	V
$V_{HB-HSUVLOHys}$	High side gate driver UVLO threshold hysteresis		0.78	0.9	1.05	V
$I_{source_pk_HO}$	HO peak source current (2)	At VCCP=12V		-0.6		A
$I_{source_pk_LO}$	LO peak source current (2)	At VCCP=12V		-0.6		A
$I_{sink_pk_HO}$	HO peak sink current (2)	At VCCP=12V		1.2		A
$I_{sink_pk_LO}$	LO peak sink current (2)	At VCCP=12V		1.2		A
BOOTSTRAP						
$I_{BOOT_QUIESCENT}$	(HB - HS) quiescent current	HB - HS = 12V		60	70	µA
I_{BOOT_LEAK}	HB to GND leakage current	V_{HB} = 600V		0.40	5.40	µA
$t_{ChargeBoot}$	Length of charge boot state(1)		230	265	300	µs
SOFT START						
SSRamp	Soft Start Ramp time(1)			25		ms
OVP/OTP						
Vclamp_otp	Clamp Voltage at 0mA(1)	At 0mA current flowing throug the clamp	1.35	1.5	1.65	V
Vclamp_otp	Clmap Voltage at 1mA(1)	At 1mA current flowing throug the clamp	2.9	3.5	4.1	V
I_{OTP}	Courent source on the BW/OTP pin			100		uA
$VOVP_{pos}$	Output voltage OVP - Threshold rising			3.5		V
$VOTP_{Neg}$	OTP - Threshold falling			0.8		V
$OTP_{CompHys}$	OTP comparator hysteresis		60	90	125	mV
$OVP_{CompHys}$	OVP comparator hysteresis		65	100	145	mV
$OTPBlanking_{startup}$	OTP bkanking time at startup			50		ms
$TOTP_{Fault}$	OTP Fuault detection time			330		us
$TOVP_{Fault}$	OVP Fuault detection time(2)			40		us
I_{LLPrgm}	LL pin sourcing current for Burst mode transition threshold programming(2)			10		µA
t_{LLPrgm}	Burst mode transition threshold programming time(2)			2		ms
ADAPTIVE DEADTIME						
dV_{HS}/dt	Detectable slew rate (falling slope) (2)		0.1		200	V/ns
FAULT RECOVERY						
$t_{PauseTimeOut}$	Paused timer (1)			1		s
THERMAL SHUTDOWN						
T_{J_r}	Thermal shutdown temperature (1)	Temperature rising	130	140		°C
T_{J_H}	Thermal shutdown hsyterisis (1)			20		°C

(1) Not tested in production. Ensured by characterization
(2) Not tested in production. Ensured by design

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6.6 Switching Characteristics

All voltages are with respect to GND, -40°C< T_J =T_A < 125°C, VCC =15V, currents are positive into and negative out of the specified terminal, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{r(LO)}$	Rise time	10% to 90%, 1nF load		30	50	ns
$t_{f(LO)}$	Fall time	10% to 90%, 1nF load		20	30	ns
$t_{r(HO)}$	Rise time	10% to 90%, 1nF load		30	55	ns
$t_{f(HO)}$	Fall time	10% to 90%, 1nF load		15	50	ns
$t_{DT(min)}$	Minimum dead time (1)			50		ns
$t_{DT(max)}$	Maximum dead time (dead time fault) (1)	ZCS event is not detected		1		µs
$t_{DT(max_ZCS)}$	Maximum dead time (dead time fault) (1)	ZCS event is detected		1.1		µs
$t_{ON(min)}$	Minimum gate on time			250		ns
$t_{ON(max)}$	Maximum gate on time			10		µs
$t_{Ipol(ZCS)}$	Blanking time after which the IPOL signal can be used to terminate DT	ZCS event is detected		500		nS

(1) Not tested in production. Ensured by design

6.7 Typical Characteristics

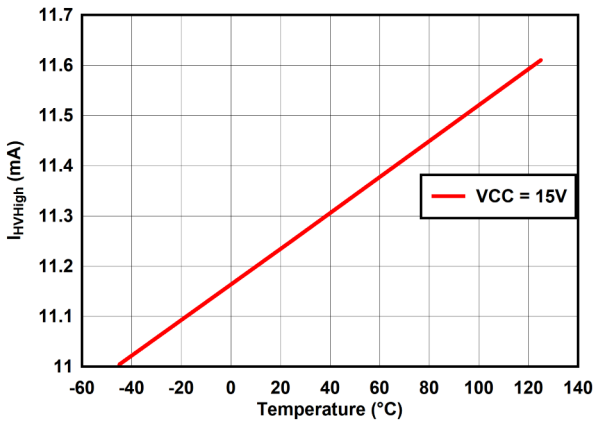

Figure 6-1. I_{HVHigh} vs Temperature

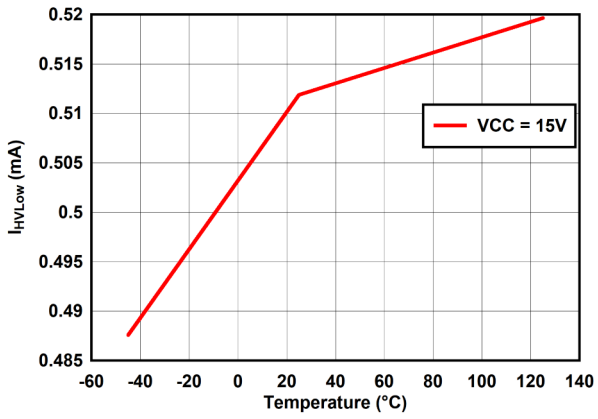

Figure 6-2. I_{HVLow} vs Temperature

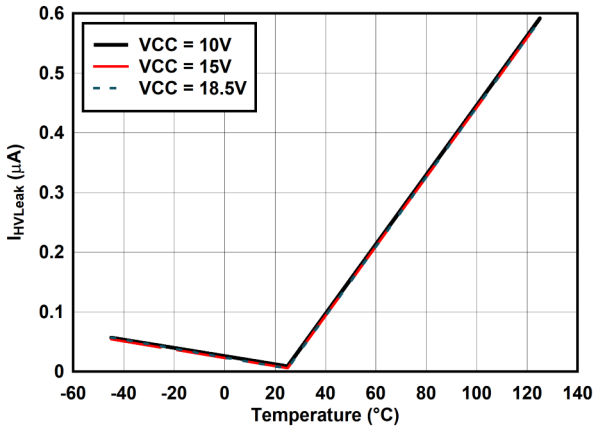

Figure 6-3. I_{HVLeak} vs Temperature

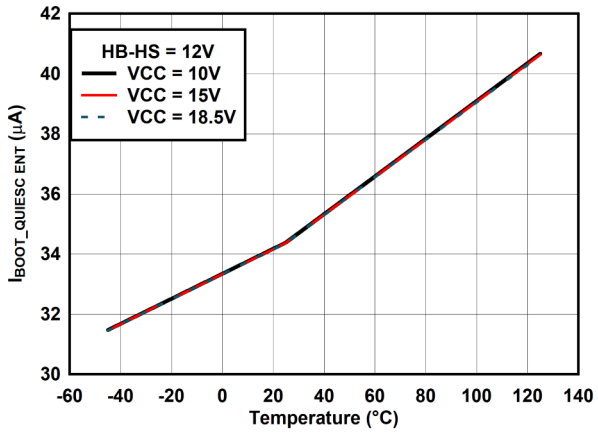

Figure 6-4. $I_{BOOT_QUIESCENT}$ vs Temperature

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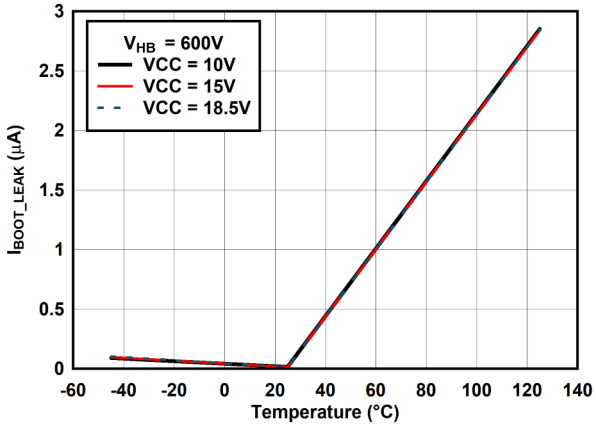

Figure 6-5. I_{BOOT_LEAK} vs Temperature

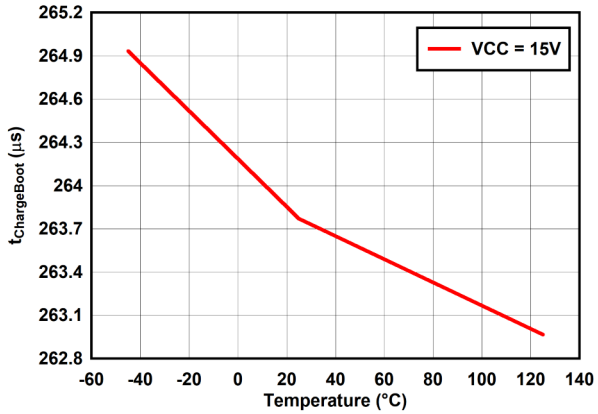

Figure 6-6. $t_{ChargeBoot}$ vs Temperature

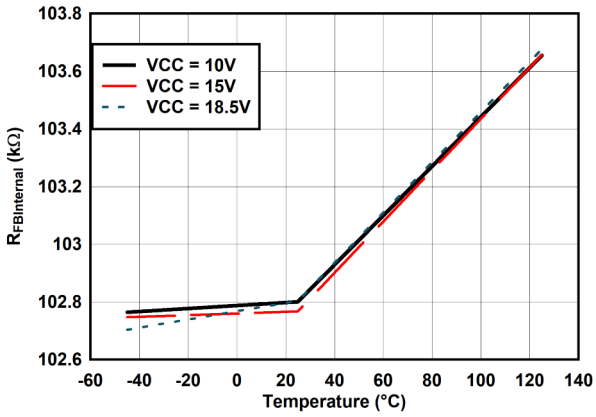

Figure 6-7. $R_{FBInternal}$ vs Temperature

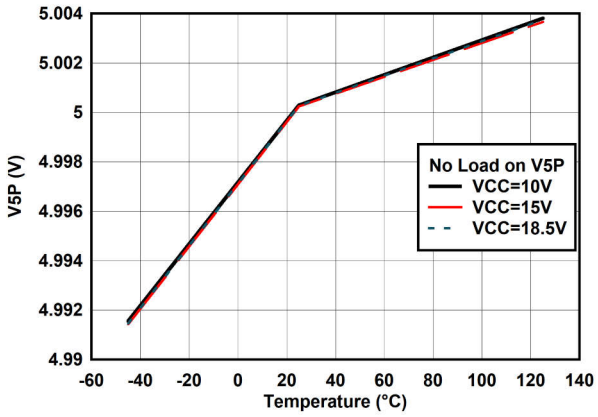

Figure 6-8. V5P (no load) vs Temperature

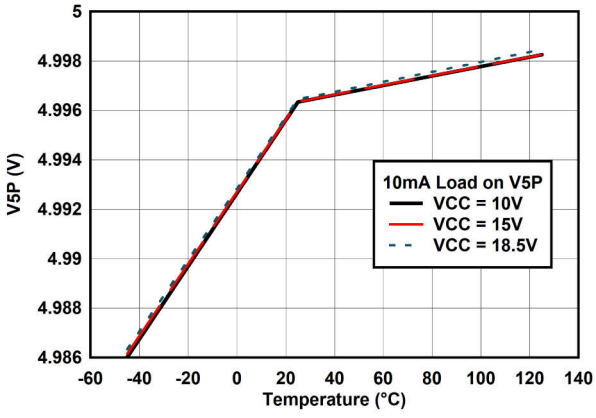

Figure 6-9. V5P (10mA Load)vs Temperature

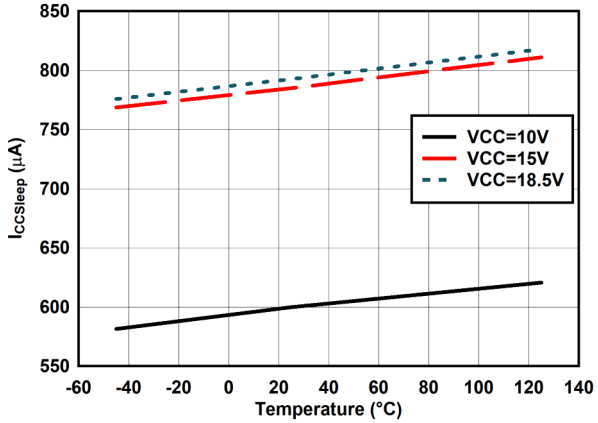

Figure 6-10. $I_{CCSleep}$ vs Temperature

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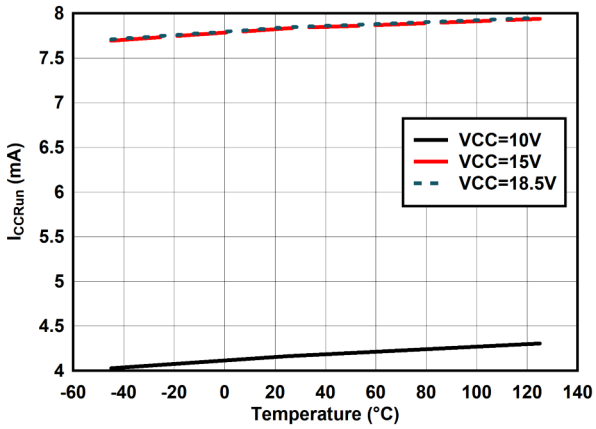

Figure 6-11. I_{CCRun} vs Temperature

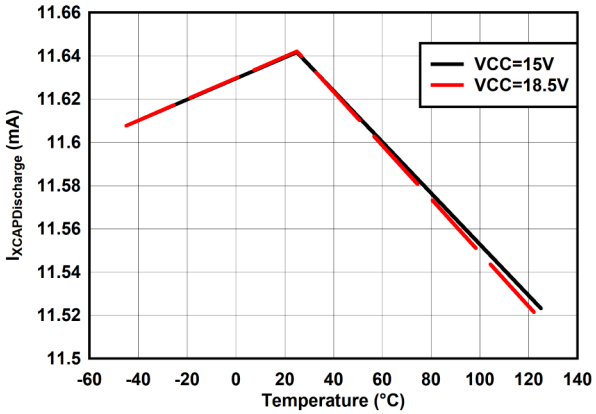

Figure 6-12. $I_{XCAPDischarge}$ vs Temperature

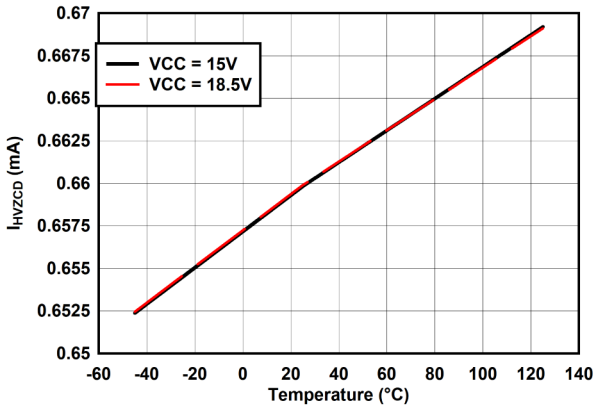

Figure 6-13. I_{HVZCD} vs Temperature

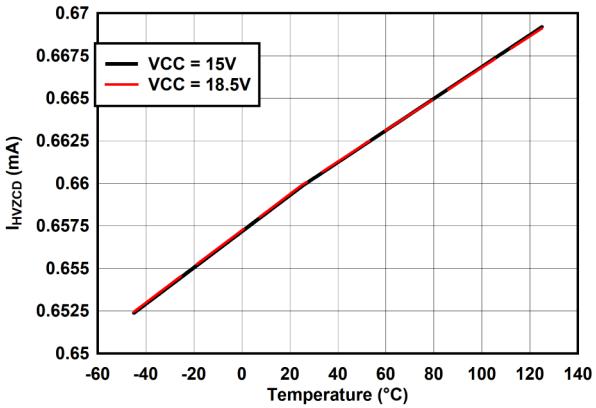

Figure 6-14. I_{HVZCD} vs Temperature

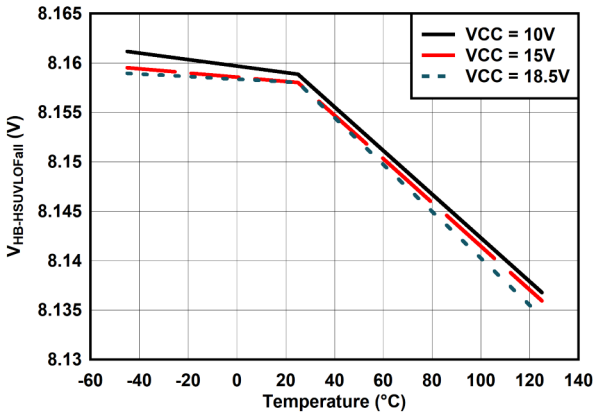

Figure 6-15. $V_{HB-HSUVLOFall}$ vs Temperature

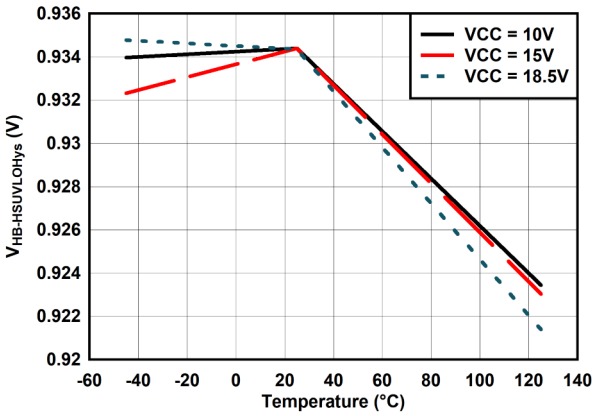

Figure 6-16. $I_{HB-HSUVLOHys}$ vs Temperature

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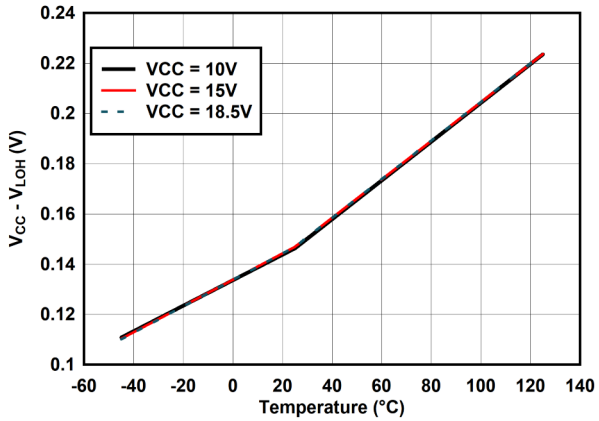

Figure 6-17. (V_{CC}- V_{LOH}) vs Temperature

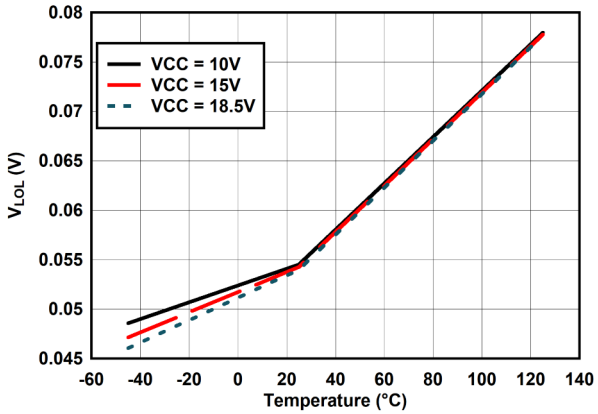

Figure 6-18. V_{LOL} vs Temperature

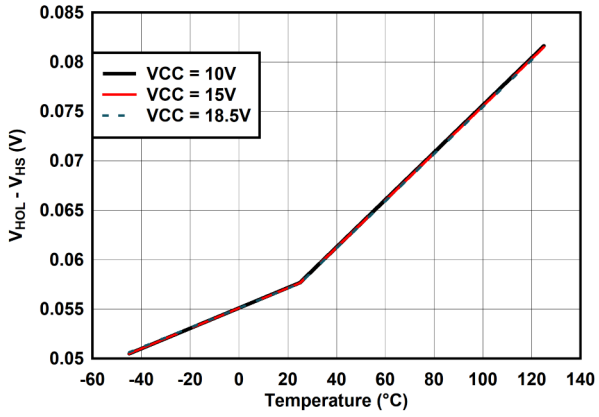

Figure 6-19. (V_{HOL}- V_{HS}) vs Temperature

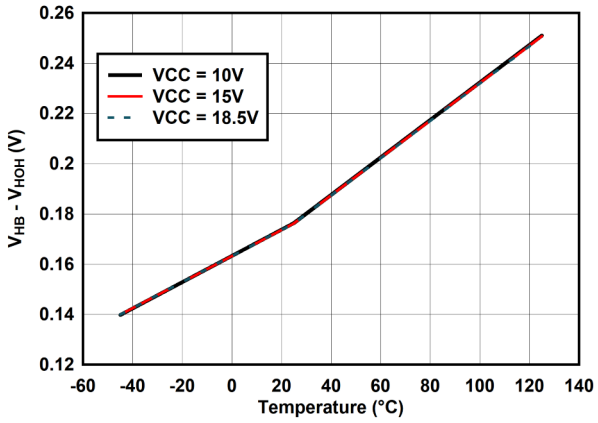

Figure 6-20. (V_{HB} - V_{HOH}) vs Temperature

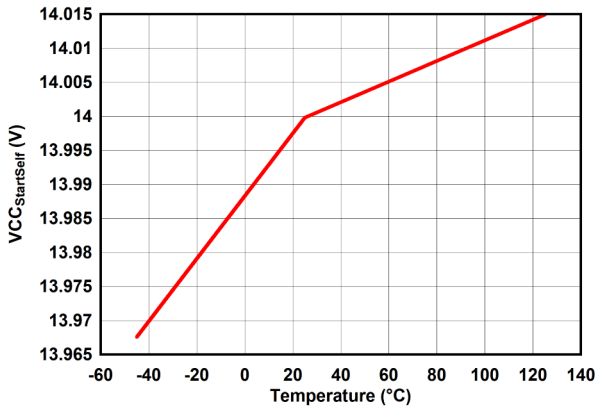

Figure 6-21. $VCC_{StartSelf}$ vs Temperature

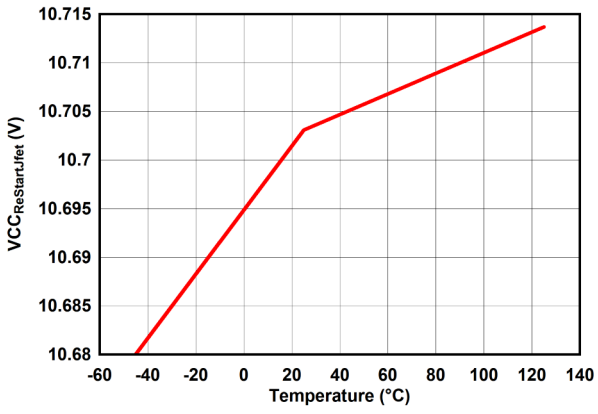

Figure 6-22. $VCC_{ReStartJfet}$ vs Temperature

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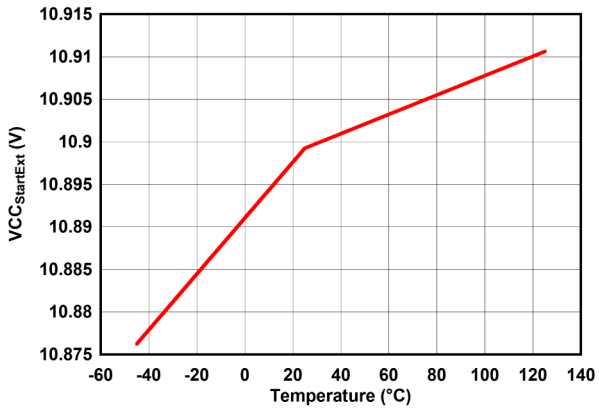

Figure 6-23. $VCC_{StartExt}$ vs Temperature

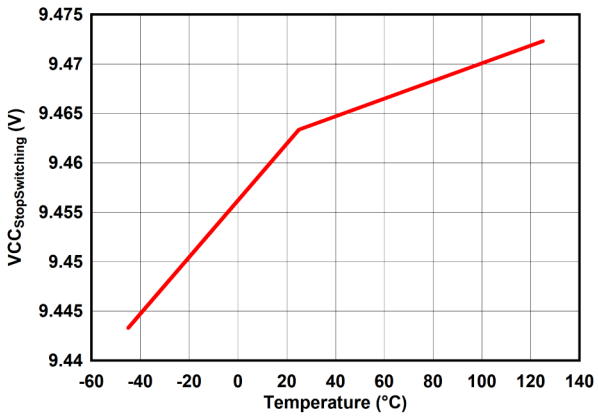

Figure 6-24. $VCC_{StopSwitching}$ vs Temperature

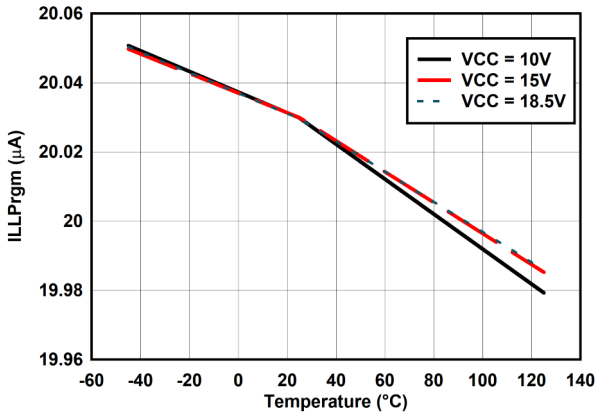

Figure 6-25. I_{LLPrgm} vs Temperature

7 Detailed Description

7.1 Overview

The UCC25660x family is a fully featured LLC resonant controller for isolated power supplies. It incorporates high level of integration and several design features to accommodate wide input/output voltage operation, high power density and increased reliability of the LLC power stage.

The device's novel control scheme Input Power Proportional Control (IPPC) offers excellent transient performance inherent in the current mode controls, while enabling a linear relationship between input power and control signal across wide input and output voltage variation. The IPPC control enables consistent light load, burst mode performance operation across a wide input/output voltage variation.

Some of the new features in UCC25660x family are specified below:

- IPPC Control enables better burst mode and dynamic response under wide input/output voltage operation.
- New operation modes to increase light load efficiency while reducing audible noise.
  - High-frequency (HF) pulse skip for improved light load efficiency.
  - Low-frequency (LF) burst mode for reduced stand by power consumption.
  - Programable light load / burst mode thresholds.
  - Adaptive burst mode threshold adjustment to accommodate input voltage change.
- Up to 750kHz full-load switching frequency enables high power density designs.
- Combined resonant current sensing with internal control voltage generation, improves control robustness.
- Input feed forward.
- Integrated protections include:
  - Fast 50ns cycle-by-cycle current limiting.
  - OCP fault to protect under short circuit conditions.
  - Over Power Protection (OPP) to limit peak input power.
  - ZCS (Zero Current Switching) avoidance scheme to eliminate capacitive region operation.
  - Adaptive soft start for reduced inrush current and eliminating reverse recovery at startup.
  - External OVP/OTP protection.
  - Input & bias supply (VCCP) UVLO.

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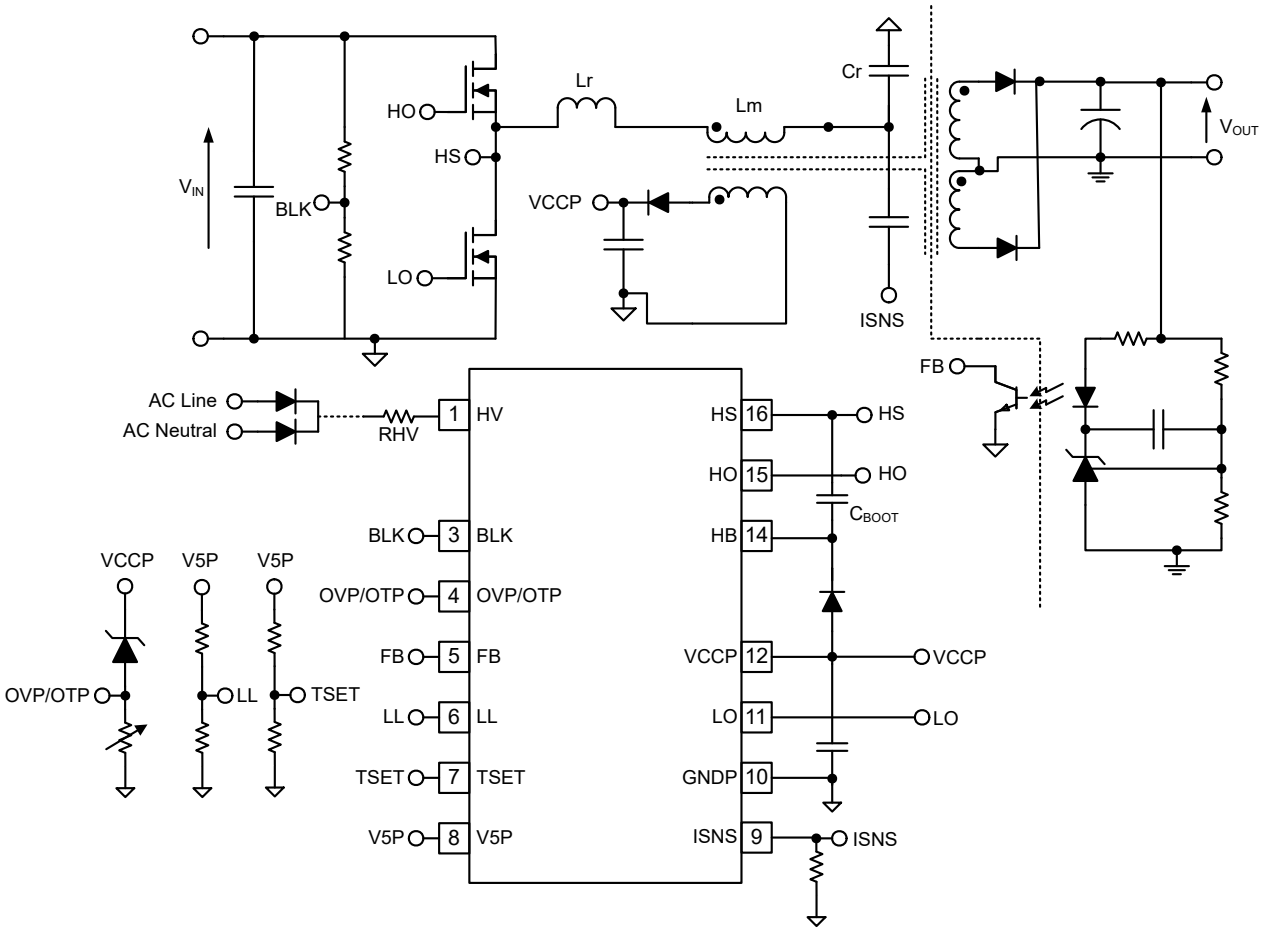
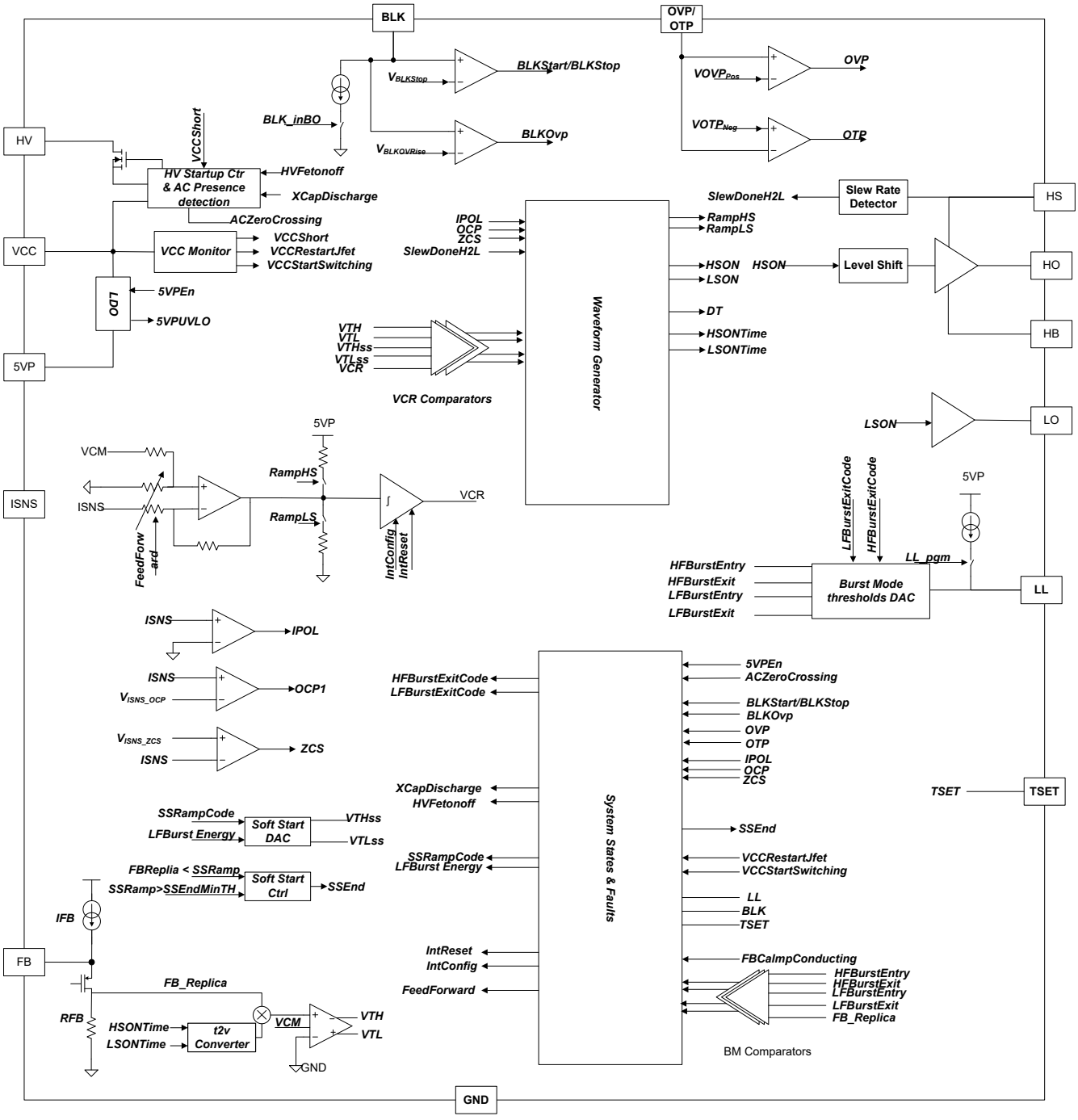


Figure 7-1. Simplified Application Schematic

7.2 Functional Block Diagram



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7.3 Feature Description

7.3.1 Input Power Proportional Control

The previous generation of TI LLC controllers use a version of Charge Control called Hysteretic Hybrid control (HHC). An improved version of the HHC, called Input Power Proportional Control (IPPC) is used in the UCC25660x family LLC controller. Compared to traditional Direct Frequency Control, where the control signal is proportional to the switching frequency, traditional charge control methods deliver faster transient response while simplifying compensator design as the power stage transfer function becomes a first order system. In traditional Charge Control, the control signal is determined by both input current and switching frequency. IPPC significantlly reduces the control signals dependency on switching frequency, thereby minimizing the impact of input and output voltage variations.

IPPC brings in the following advantages:

- Makes control signal proportional to input power.
- Consistent burst mode and over load performance in wide LLC (WLLC) operation application.
- Retains faster load transient performance and improves line transient performance.

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The UCC25660x family measures the resonant tank current on the ISNS pin through an external differentiator formed by capacitor C_{ISNS} and resistor R_{ISNS}. The voltage on the ISNS pin is integrated in the VCR synthesizer block to form an internal VCR signal *VCR_synth*.

The VCR Synthesizer block applies feed forward gain based on the BLK pin voltage, applies ramp compensation to generate the compensated internal VCR signal.

The compensated internal VCR signal is then compared with two sets of thresholds to control the high side switch turn-off (V_{TH}) and low side switch turn-off (V_{TL}). The thresholds V_{TH} and V_{TL} are generated from the internal control signal FBReplica and the high-side and low-side switch on-time from the previous half switching cycle. During the soft start, the V_{TH} and V_{TL} thresholds are generated based on the internal soft start ramp. This is used to minimize the resonant tank inrush current during startup.

In the waveform below, the high-side and low-side switches are controlled based on the internal VCR signal and comparator thresholds V_{TH} and V_{TL}. When the VCR is higher than V_{TH}, the high-side switch is turned off and when VCR is lower than V_{TL}, the low-side switch is turned off.

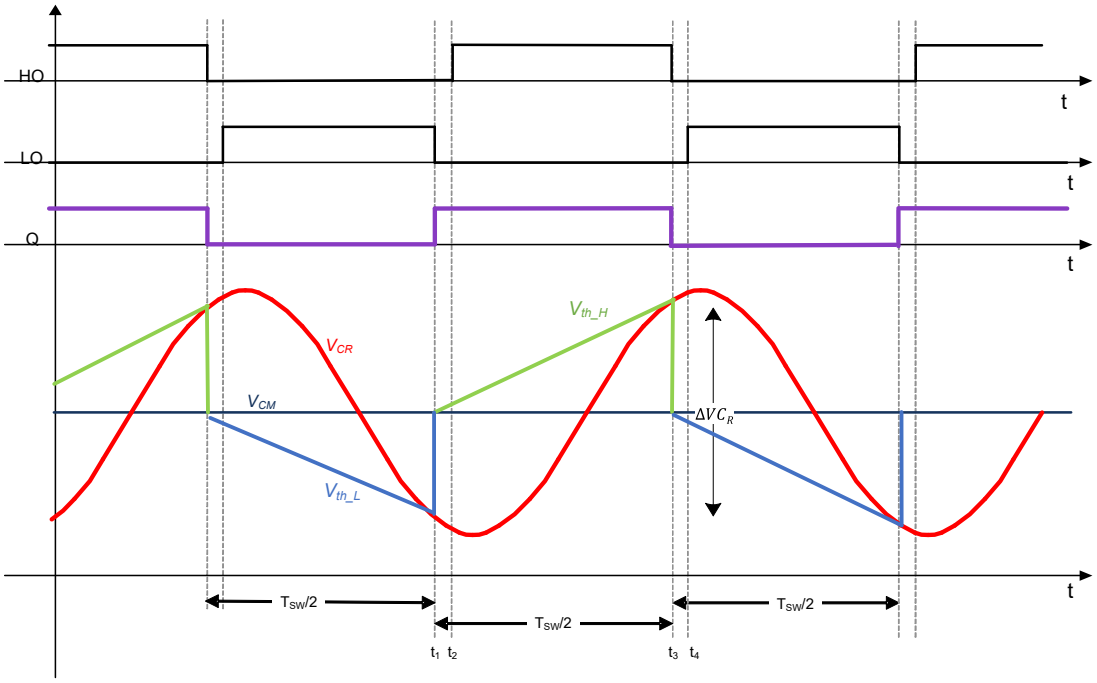

Figure 7-2. IPPC Basic waveforms

The comparator thresholds V_{TH} and V_{TL} can be calculated using the equations below.

$$V_{TH} = (V_{CM} + k*FBReplica*Tsw/2) \quad (1)$$

$$V_{TL} = (V_{CM} - k*FBReplica*Tsw/2) \quad (2)$$

$$V_{TH} - V_{TL} = \Delta V_{CR} = k*FBReplica*Tsw \quad (3)$$

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7.3.1.1 Voltage Feedforward

By implementing input voltage feed forward, the control signal is proportional to the input power P_{inavg}.

Rewriting the Equation 4 with input voltage feedforward applied.

$$FBReplica = \frac{2}{C_r} * K_1 * Pin_{avg} + K_2 * Iramp \quad (4)$$

The input voltage to the LLC power stage is periodically sensed on the BLK pin. A periodic average of this voltage is then used to adjust the feed forward gain to make the control signal proportional to input power. More details on this can be found in VCR Synthesizer.

7.3.2 VCR Synthesizer

The UCC25660x family implements a VCR Synthesizer which integrates the resonant tank current to form a internal representation of the resonant capacitor voltage. By implementing the VCR synthesizer internally, the UCC25660x family provides for an ability to support very high frequency startup with controlled inrush currents and feed forward gain stage. The internal VCR synthesizer also makes the controller less succeptible to external noise picked up on the ISNS pin, making the controller more robust.

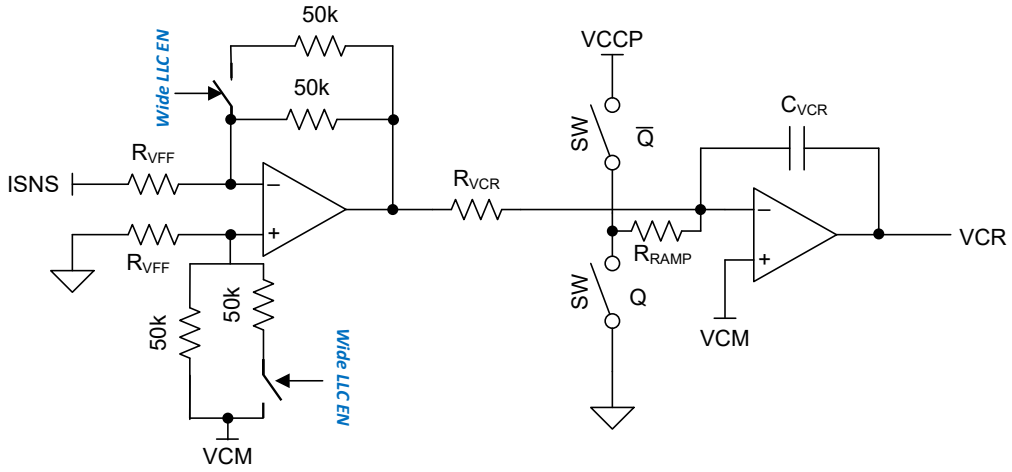

Figure 7-3. VCR Synthesizer Block Diagram

The first stage of the VCR synthesizer consists of a programable gain stage, used to implement the input voltage feed forward function. The second stage consist of a programable integrator with ramp compensation.

The UCC256604 has extended gain range enabled. This extended gain range helps to reduce the FBReplica variation when input voltage of the LLC changed over a wide range (3:1). This is achieved by reducing the gain of the programmable gain stage of the VCR synthesizer by turning on the *Wide LLC EN* bit.

To accommodate a wide frequency range of LLC power stages, the time constant of the integrator is externally configurable at startup to meet the needs of the design using the TSET pin. A voltage resistor divider between V5P and GNDP, connecting to TSET pin, configures the TSET settings. The UCC25660x family detected the divider ratio during startup. Based on the divider ratio, not only the time constant but the OCP threshold can be choosen. Once the time constant is chosen, the maximum dead-time is also configured. The column 2 in the tabled indicates the minimum frequency upto which the IPPC operation is maintained. Once the frequency falls below this, the controller can still maintian closed loop operation and works as a conventional current mode control.

In the table value TSET voltage values indicated are nominal values. Maximum and minimum range that can be used for each TSET setting is within +/- 48mV.

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Table 7-1. TSET Programming Options table

TSET Option #	TSET Voltage (V) for 3.5V OCP	TSET Voltage (V) for 4V OCP	Minimum Frequency for IPPC Operation (kHz)	Integrator Time Constant (ns)	Maximum dead-time (µs)
17	2.295	2.675	698.6	68	0.5
16	2.168	2.802	591.6	80	0.5
15	2.041	2.929	501	93	0.5
14	1.914	3.056	424.3	112	0.5
13	1.787	3.183	359.3	132	1
12	1.66	3.310	304.3	156	1
11	1.533	3.427	256.7	184	1
10	1.416	3.554	218.2	214	1
9	1.299	3.681	184.8	257	1
8	1.182	3.798	156.5	304	1
7	1.074	3.906	132.5	359	1
6	0.967	4.013	112.2	424	1
5	0.850	4.130	95	490	1
4	0.742	4.238	80.5	588	1
3	0.644	4.336	68.1	694	1
2	0.547	4.433	57.7	820	1
1	0.450	4.532	48.9	968	1
X	<0.392	>4.589	X	X	X

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7.3.3 Feedback Chain (Control Input)

Control of the output voltage is provided by a voltage regulator circuit located on the secondary side of the isolation barrier. The demand signal from the secondary-side regulator circuit is transferred across the isolation barrier using an optocoupler.

A constant current source I_{FB} is generated from VCCP voltage and connected to FB pin. A resistor RFB is also connected to this current source with a PMOS in series. During normal operation, the PMOS is always on, so that the FB pin voltage is equal to the Zener diode reference voltage plus the voltage drop on the PMOS source to gate.

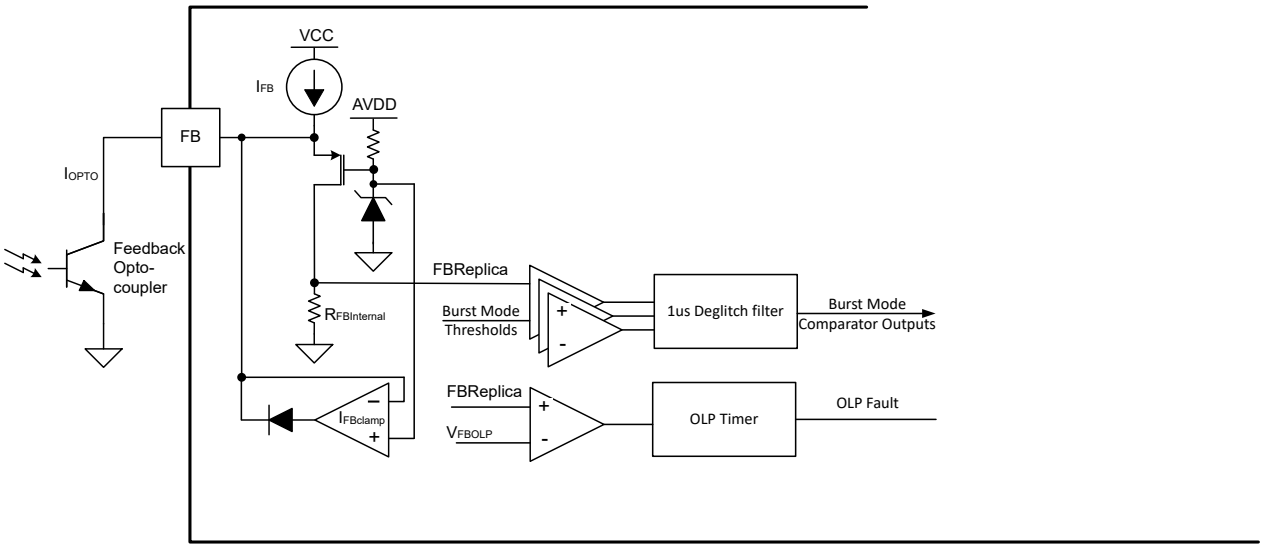

Figure 7-4. Feedback Chain Block Diagram

$$I_{R_{FBInternal}} = I_{FB} - I_{OPTO} \quad (5)$$

The control signal *FBReplica* is depicted using the equation below.

$$FBReplica = I_{R_{FBInternal}} \cdot R_{FBInternal} \quad (6)$$

From this equation, when I_{OPTO} increases, I_{RFB} decreases, decreasing the *FBReplica* . In this way, the control signal is inverted. When I_{OPTO} continues to increase and reaches the value of I_{FB}, the FB pin voltage starts to drop because there is not enough current flow through the PMOS. FB pin pulled low impacts the system transient response, due to the extra delay introduced by charging the parasitic capacitor of the optocoupler to pull up the FB pin voltage. A FB pin voltage clamp circuit is used to prevent this scenario. When FB pin voltage drops below the FB pin clamp voltage threshold, an extra current source is turned on to clamp the FB voltage. The clamp strength is $I_{FBClamp}$. The FB pin clamp circuit improves the system transient performance from light load to heavy load. The FB pin clamp operation is shown in the figure below.

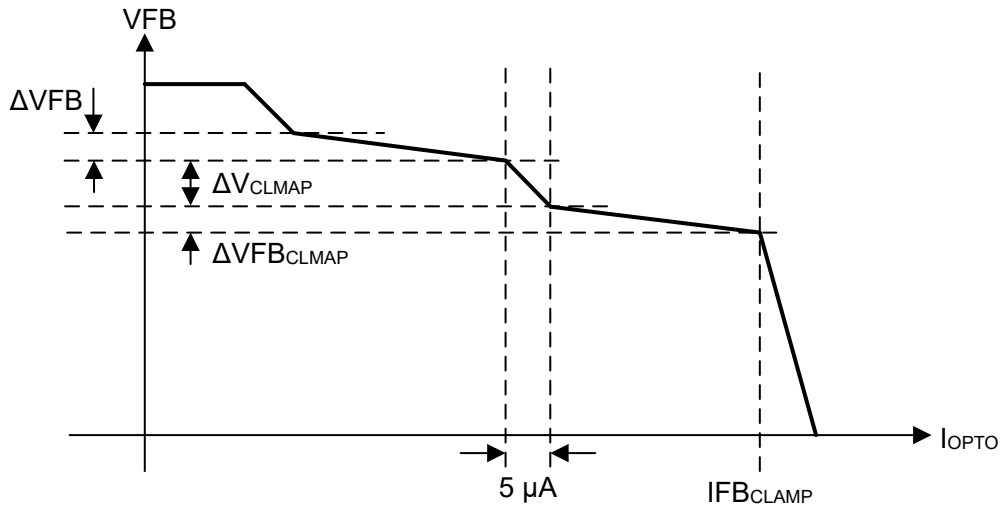

Figure 7-5. FB Pin Voltage vs FB Pin Current

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7.3.4 Adaptive Dead-Time

The UCC25660x family implements a high-speed low latency slew-rate detection block to optimize the dead time between high-side and low-side pulses. The adaptive dead-time block adjusts the dead time to prevent shoot through or excessive body diode conduction.

At the core of the adaptive dead time block is the slew rate detector block, capable of detecting slew rates upto 200V/ns, making UCC25660x family an excellent choice for use in high frequency resonant converters.

In burst mode, during a ZCS prevention operation or in power stages where the slew rate can be very slow, the resonant tank current polarity signal (Ipolarity comparator output) is used to augment the slew rate detector.

Taking advantage of the natural symmetric operation of LLC, only the dead time between high-side switch turn off and low-side switch turn on is determined by the slew rate detector. This dead time is copied and then applied to the dead time between low-side MOSFET turn off and high-side MOSFET turn on. There are a few exceptions where the dead time is not copied. The conditions are listed below.

- Missing Slew rate detector signal in the previous High to Low transition.
- ZCS detection in the previous cycle.

Under the above-mentioned conditions, the Ipolarity comparator based on the ISNS signal is used to adjust the dead time during low to high transitions.

7.3.5 Input Voltage Sensing

The input voltage sensing through BLK pin is used to implement multiple functions listed below:

- Input voltage Brown-in & Brown-output
- Input feedforward (explained in Input Power Proportional Control)
- Input voltage OVP.

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7.3.5.1 Brown in and Brown out Tresholds and Options

UCC25660x family provides programmable brown-in and brown-out threshold. When the voltage on the BLK pin falls below $V_{BLKStop}$, the controller enters brown out state and stops switching. In the brown-out state, an additional current sink is turned on to draw I_{BLKHys} form the BLK pin. By changing the equivalent resistance connected to the pin externally, the actual brown-in voltage can be programmed.

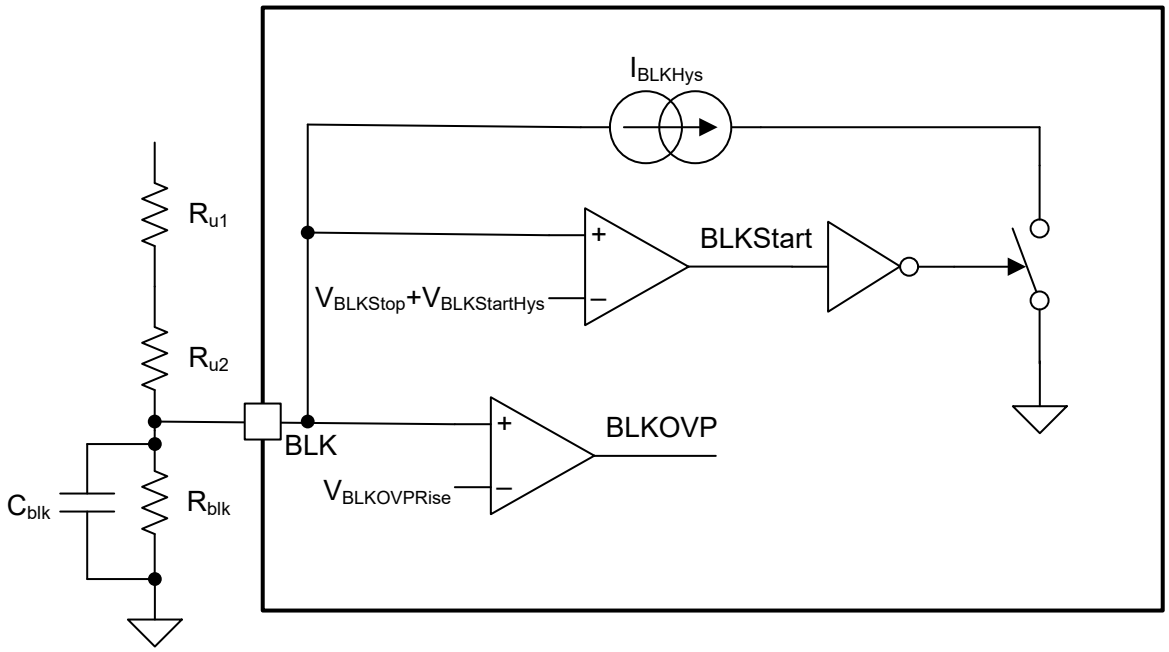

Figure 7-6. BLK Pin Input Voltage Sensing Architecture

When brown-out is detected, the controller stops switching. If BLK voltage rises above the brown-in voltage, the controller immediately begins soft start and does not wait for fault idle time.

In the variants that have the BLK OVP option enabled, if the BLK pin voltage rises above the OVP threshold, the controller stops switching and move to the fault state. After the fault idle time, the controller checks if the OVP condition is cleared. If the OVP condition is removed, the controller begins recovery and soft start. If the OVP condition is not cleared, the controller stays off and waits until the OVP condition is cleared.

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7.3.5.2 Output OVP and External OTP

UCC25660x family uses a multi-functional pin (OVP/OTP) that monitors for output overvoltage and external over-temperature conditions.

A Zener is connected between VCCP and the OVP/OTP pin. Under normal operating conditions, the Zener does not conduct and the OVP/OTP pin voltage is the result of the NTC resistance and I_{OTP} source current. If VCCP rises high enough to exceed the Zener breakdown voltage, the voltage on the OVP/OTP pin is pulled high because of the Zener current. If the voltage on OVP/OTP exceeds the $VOVP_{Pos}$ threshold for 40us the controller detects a fault and stops switching.

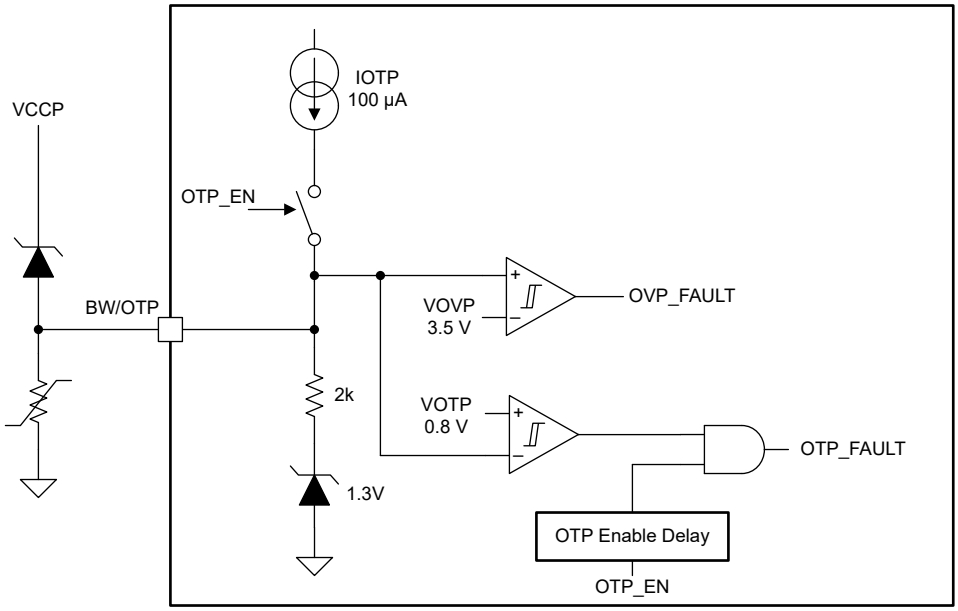

Figure 7-7. OVP/OTP Protection Architecture

A NTC is connected from OVP/OTP to GNDP. An internal current source, I_{OTP}, flows out of the OVP/OTP pin and into the NTC resistor. Based on the temperature of the NTC, the resulting voltage on the pin is compared to $VOTP_{Neg}$ to determine if an external over-temperature fault occurrs. Upon detection of external over-temperature protection, UCC25660x family moves to the fault state. After the 1-s wait period, UCC25660x family checks the OVP/OTP pin voltage. If the OVP/OTP pin voltage is higher than $VOVP_{Pos}$, the UCC25660x family attempts to restart, else it continues to wait in fault idle state. During burst mode, the over-temperature protection is disabled to minimize quiescent current. When transitioning from burst mode to normal switching, the OTP function is re-enabled.

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7.3.6 Resonant Tank Current Sensing

The ISNS pin senses the resonant tank current through a differentiator. Besides serving as over current protection pin, the ISNS pin is also an essencial part of the control functions.

The ISNS pin has the following functions.

1. Input to the integrator that develops the control voltage, used for IPPC control.
2. OCP (Cycle-by-Cycle) protection.
3. Resonant current polarity detection.
4. ZCS prevention and dead-time management.
5. Reverse recovery avoidance at startup.

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7.4 Protections

7.4.1 Zero Current Switching (ZCS) Protection

ZCS protection is a necessary function for LLC converters to avoid crossing over into the capacitive region of operation. In the capacitive region, the MOSFETs experience severe reverse recovery which can lead to damage to the LLC power stage. In addition, the gain vs frequency relationship inverts in the capacitive region and can cause the converter to completely lose regulation of the power stage.

The goal of the ZCS protection is to make sure that the MOSFET can be turned off before the current inverts thereby eliminating possibility of a hard reverse recovery of the MOSFET's body diode. This can increase the reliability of the power stage. The minimum turn off current is set at a threshold which can increase the chances of achieving ZVS or close to ZVS switching for switches under this condition.

Couple with dead time engine which looks at both the slew done signal and the IPOL signal, we can make sure that opposite MOSFET turns-on at the valley point of the Vds voltage, providing lower turn-on losses.

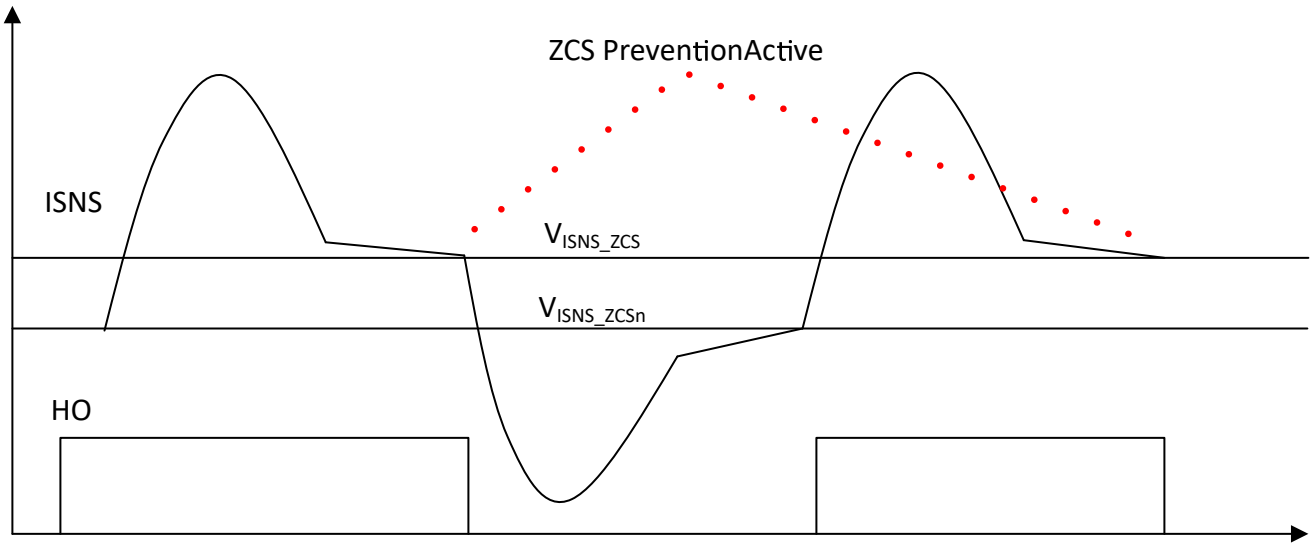

Figure 7-8. ZCS Protection

When operation nears the inductive/capacitive boundary, the resonant current decreases before the gate turn is turned off. If the ISNS waveform is less than the V_{ISNS_ZCS} threshold, the gate pulse is terminated early instead of waiting for the VCR waveform to cross the VTH or VTL boundary. This early termination scheme is capable of leaving enough resonant current at the gate turn-off edge to drive the ZVS transition during the dead-time.

The ISNS signal is fed to two ZCS comparators. As there is a dedicated comparator for when the HO is on and for when the LO is on, the other comparator output is ignored.

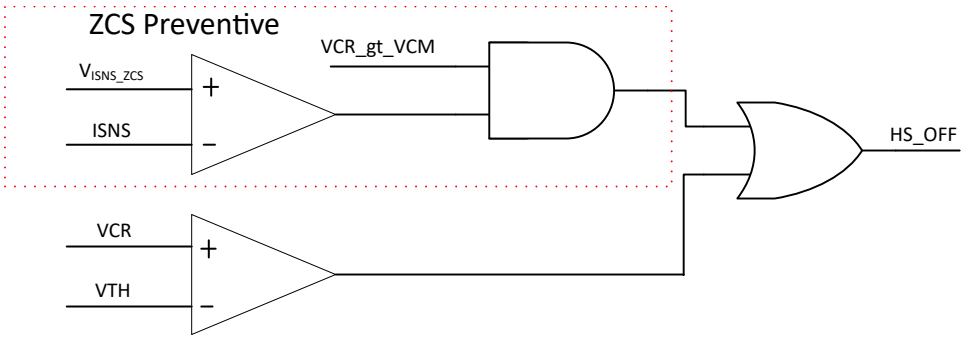

Figure 7-9. ZCS Prevention Scheme when the High-Sde MOSFET is On

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The shape of the resonant current well below the resonant frequency poses some challenge for detecting the correct falling edge of the resonant current waveform. The UCC25660x implements additional logic to make sure that the correct falling edge of the ISNS signal is detected to avoid false tripping.

To improve robustness against noise, the ISNS ZCS comparators are blanked at the rising edge of HO or LO gate. The same blanking time $t_{leb}$is used for both the VCR comparators and the ISNS ZCS comparators.

When a ZCS event is detected, internally the Soft Start ramp voltage is slowly reduced. When the internal soft start ramps down, the switching frequency is also forced to increase further, forcing the system out of Capacitive region.

In the event of a persistent ZCS condition, the controller ceases switching action and move to the fault state. A configurable time-out is used to declare a persistent ZCS fault condition.

7.4.2 Minimum Current Turn-off During Soft Start

During startup, for the first few switching cycles the MOSFET's on the primary side can experience body diode reverse recovery and hard switching. This is mainly due to the fact that at startup the resonant capacitor can have DC bias voltage which is off from the steady state operating voltage of Vin/2. This leads to a asymmetry in the resonant tank current at startup. In the first few cycles, this asymmetry can be high enough that the current at the point of switch turn-off is in the wrong polarity.

For example, please refer to the figure below.

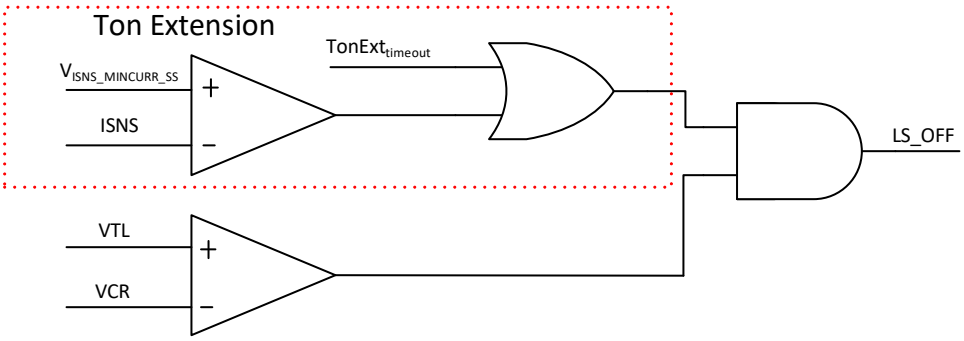

Figure 7-10. Ton Extension Scheme

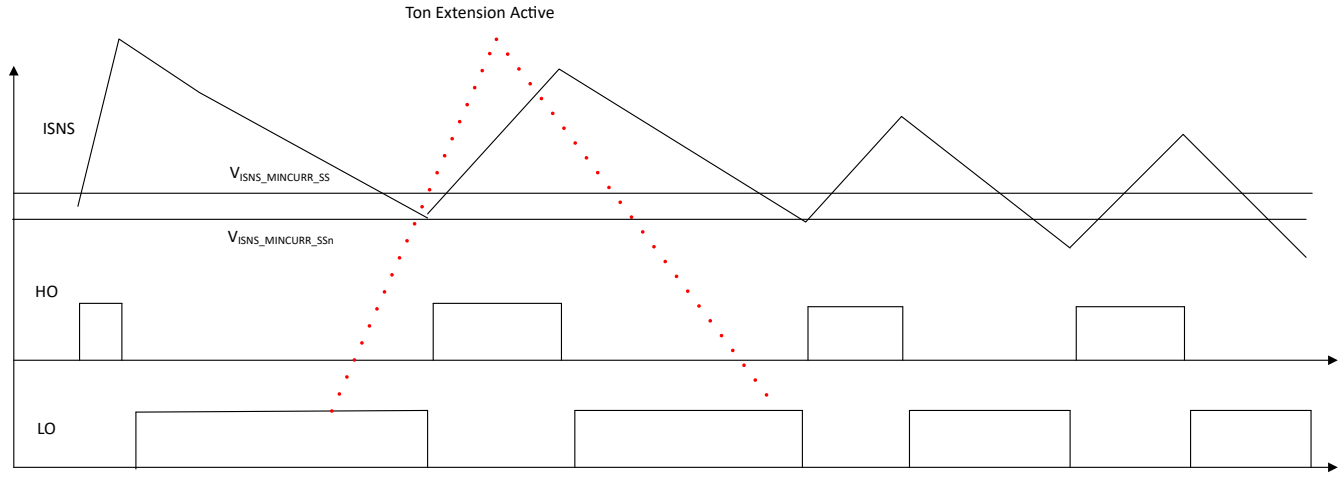

Figure 7-11. ZCS Prevention During Startup

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7.4.3 Cycle by Cycle Current Limit and Short Circuit Protection

The OCP and cycle-by-cycle current limiting feature in UCC25660X provides a fast (<50ns) response to short circuit.

The cycle-by-cycle protection helps to limit the peak stress in the power stage. When the ISNS voltage becomes greater than + V_{ISNS_OCP}, the current HO gate pulse is terminated. Correspondingly, during the half cycle where the LO pulse is high, if the ISNS voltage becomes less than V_{ISNS_OCPn} the current LO gate pulse is terminated.

If OCP is detected in 7 consecutive switching cycles, the device move to the fault state.

7.4.4 Overload (OLP) Protection

Using IPPC with feed forward enables us to get a close correlation between Pout Vs internal contrl signal FBReplica.

When the FBReplica goes above the V_{FBOLP} (I_{opto} goes to 0µA), the system starts to limit the input power and the OLP timer count increases. If the FBReplica stays above V_{FBOLP} for >(T_{OLP}), the OLP fault is detected and the system goes into fault restart sequence.

7.4.5 VCC OVP Protection

An internal current limited clamp on the VCC pin protects the VCC pin and clamps the gate drive output voltage when the voltage applied to the VCC pin exceeds the recommended max voltage. The clamp has maximum sink current $IVCC_{clamp}$. If the current going through the VCC shunt exceeds $IVCC_{clamp}$, this will result in in the further increase in the VCC pin voltage crossing VCC_{OVP}. If this occurs UCC25660X will immediately move to FAULT condition and retry after the 1s fault idle time.

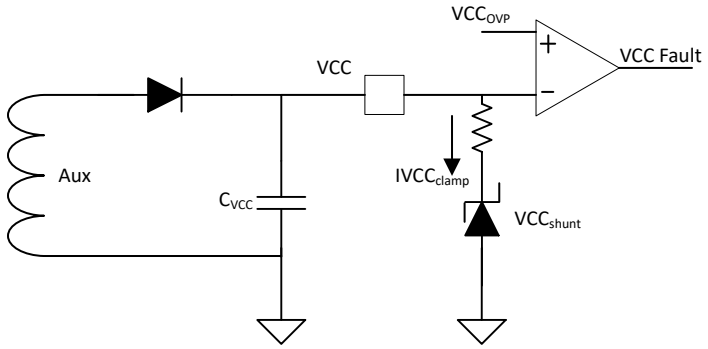

Figure 7-12. VCC Clamp

7.5 Device Functional Modes

7.5.1 Startup

7.5.1.1 With HV Startup

First time startup sequence

1. When AC is plugged in, voltage is applied on HV pin. If VCCP voltage is below VCC_{Short}, VCCP pin is charged with $I_{VCC_Charge_Low}$. If VCCP voltage is higher than VCC_{Short}, VCCP pin is charged with $I_{VCC_Charge_High}$.
2. When VCCP voltage is higher than VCC_{UVLOr}, an internal LDO regulates the V5P voltage untill the device initialization is complete.
3. V5P is established. LL pin & TSET pin are used for burst mode and internal VCR Synthesizer programming.
4. If the HV startup option is enabled, the TSET pin outputs high (means PFC OFF) to prevent PFC from turning on before VCCP is full established.
5. When VCCP is higher than $VCC_{StartSelf}$, HV charge current stops. LLC startup process begins. TSET voltage is kept lower than 1V, allowing PFC to startup.
6. If during stages 3 and 4, VCCP voltage drops below $VCC_{ReStartJfet}$, HV charge current enables again and VCCP gets charged with $I_{VCC_Charge_High}$
7. Once LLC finishes startup, HV charge current is disabled until VCCP drops below $VCC_{ReStartJfet}$.
8. During normal operation if the VCCP voltage falls below $VCC_{StopSwitching}$, a fault occurs and UCC25660x family shuts down. Normal restart sequence is then followed.

Restart sequence

1. After a fault is detected, UCC25660x family shuts down. For fault retry mode, after 1s idle time, UCC25660x family retries (TSET outputs high when VCCP is still higher than VCC_{UVLOf}).
2. if VCCP voltage is below VCC_{Short}, VCCP pin is charged with $I_{VCC_Charge_Low}$. If VCCP voltage is higher than VCC_{Short}, VCCP pin is charged with $I_{VCC_Charge_High}$. If VCCP pin voltage is higher than $VCC_{StartSelf}$, HV startup is not enabled (Phase I is skipped). V5P is established and LL pin is released for burst mode programming.

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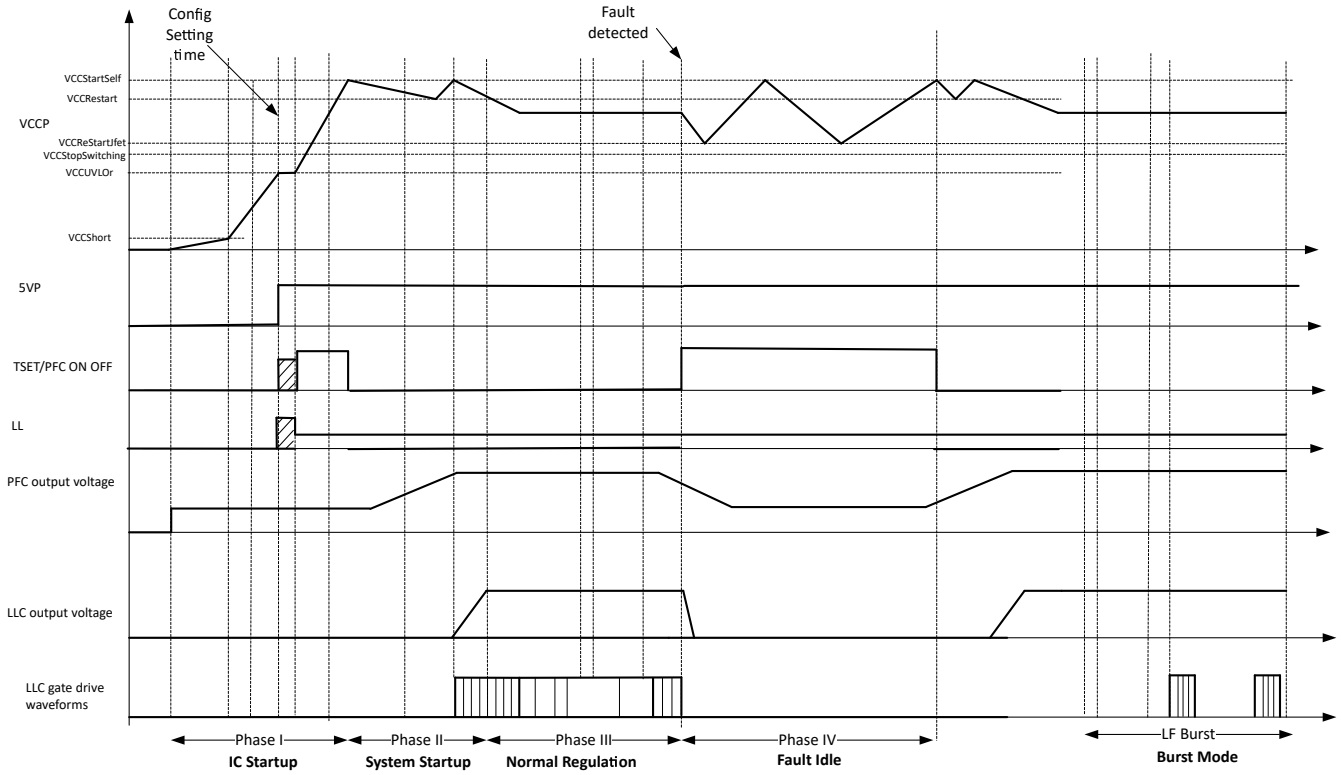

Figure 7-13. Startup Sequence for "HV Startup" Feature Enabled

7.5.1.2 Without HV Startup

When HV startup is disabled, PFC on/off signal is disabled as well. Therefore, the PFC on/off sequence during startup is disabled when HV startup is disabled. The startup sequence is as follows:

1. When VCCP voltage is higher than VCC_{UVLOr}, V5P is established
2. LL pin and TSET pin are used for burst mode and internal VCR integrator programming.
3. When VCC drops below VCC_{UVLOf}, V5P turns off and system shuts down.

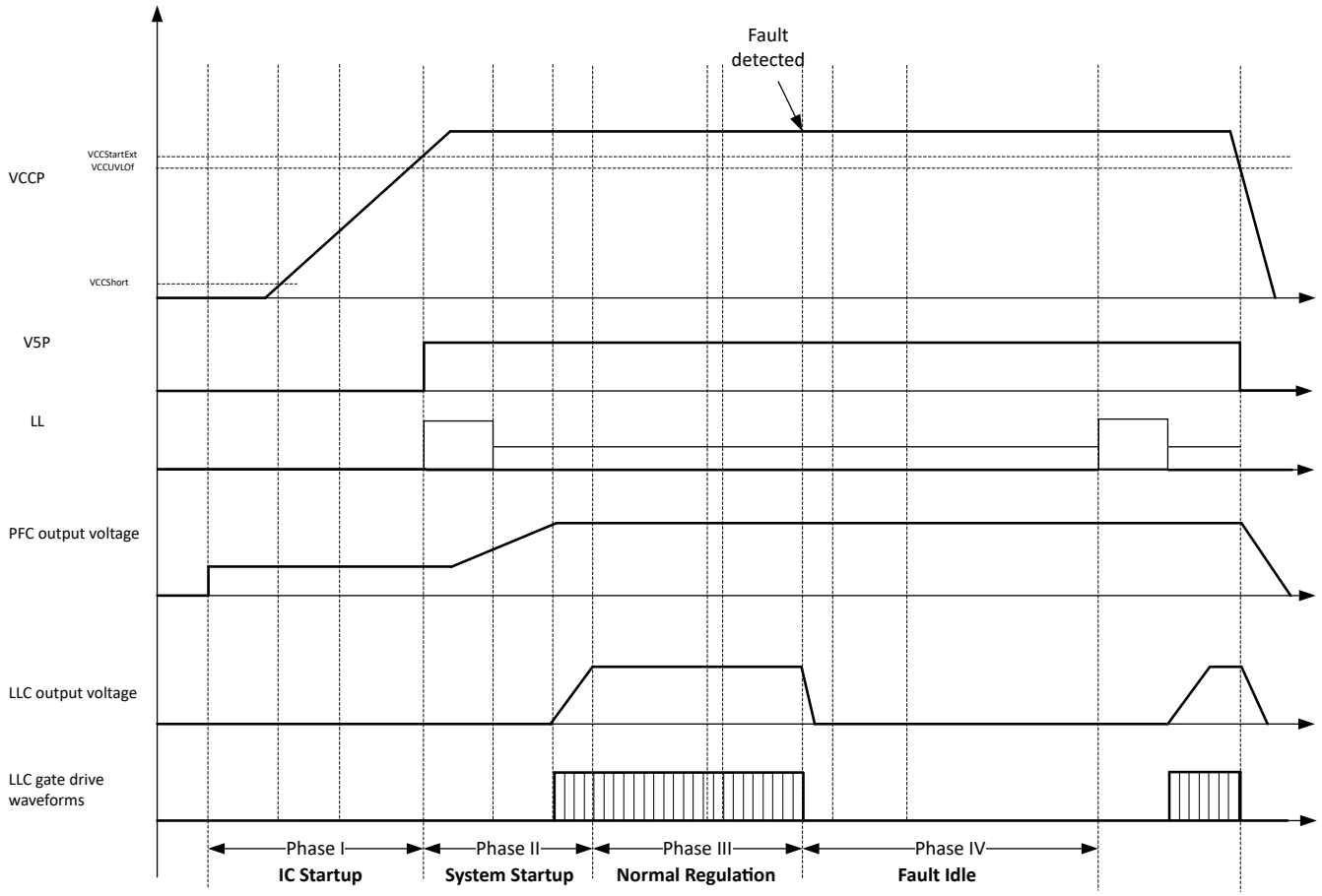

Figure 7-14. Startup Sequence for “HV Startup” Feature Disabled

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7.5.2 Soft Start Ramp

The Soft Start ramp is internally generated in the UCC25660x family. A fixed maximum Soft Start time of 25 ms is internally generated to help reduce inrush current at startup while allowing a fast output voltage ramping up.

7.5.2.1 Startup Transition to Regulation

In UCC25660x family, a new soft start is implemented to control the inrush current at startup.The new scheme helps avoiding any premature soft start termination and ensures smooth transition between soft start and closed loop regulation.

At startup, internal Soft start voltage (*SSRamp*) ramps up using a defined slope and the *FBReplica* is high as the output voltage is below the regulation voltage. A pick lower block looks at these two signals and uses the one that is lower of the two to control the turn-off of the power stage switches.

The soft start is exited only after the *SSRamp* is above a minimum threshold, avoiding any premature soft start exit. A figure showing this behaviour is shown below.

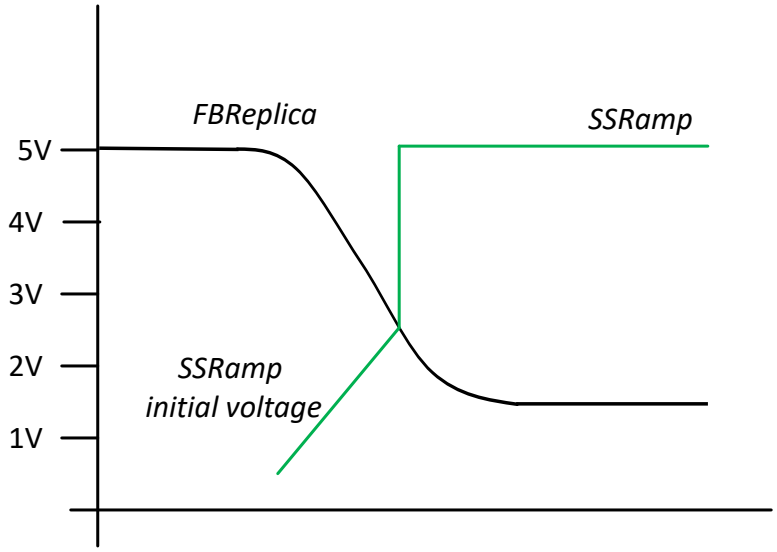

Figure 7-15. Soft Start operation

7.5.3 Light Load Management

7.5.3.1 Operating Modes (Burst Pattern)

UCC25660x family burst mode algorithm minimizes audible noise, while improving light load efficiency. This is accomplished by maintaining the burst packet frequency to either be above the audible range (>25kHz) or to maintain the burst packet frequency to be at the very low end of the audible region (<400Hz). UCC25660x family employs two burst mode patterns; high-frequency (HF) pulse skip and low-frequency (LF) burst.

HF burst packet includes a fixed number of LO and HO pulses. The purpose of HF burst is to maintain the burst frequency higher than the audible frequency range. In the below image, the low-side gate is enabled on the 2nd valley of the switch node to begin delivery of the next HF burst packet.

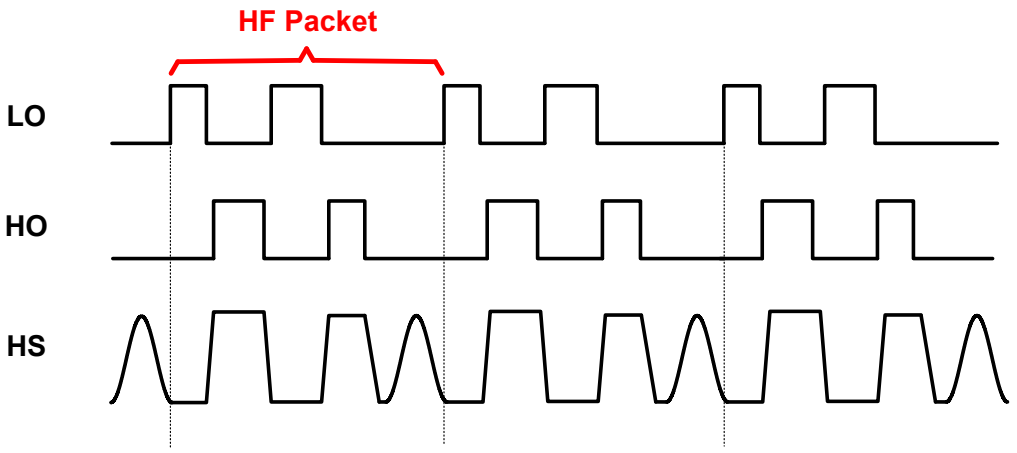

Figure 7-16. High Frequency Pulse Skip Packet

LF burst includes a number of HF burst packets and a LF burst off period.

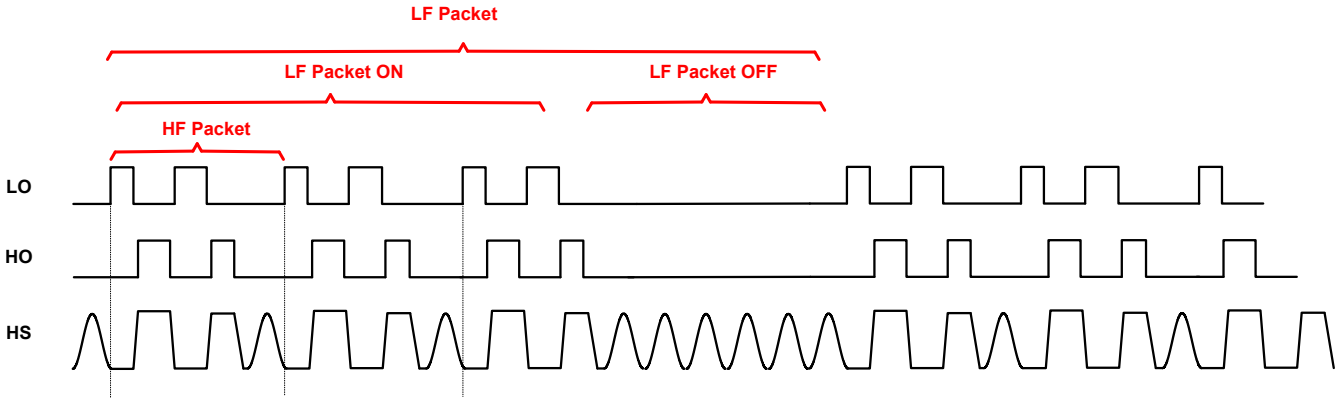

Figure 7-17. Low Frequency Burst Packet

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The number of HF burst packet is calculated to maintain the LF burst frequency within a frequency range. A set of target frequency range is internally provided, the default option is to regulate the LF burst around 200Hz.

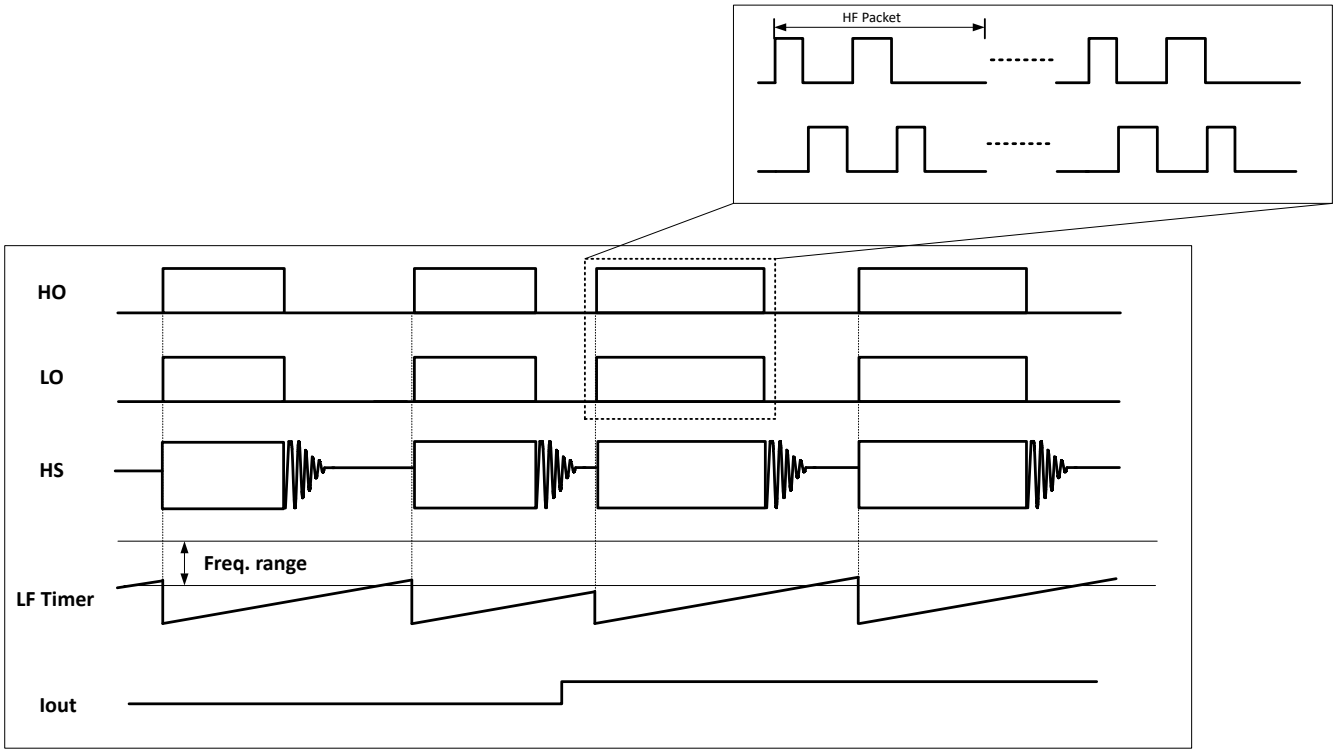

Figure 7-18. Packet Size Regulation Inside LF Burst

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7.5.3.2 Mode Transition Management

Using the LL pin, the user can configure the power level at which the UCC25660x family enters the HF pulse skip and LF Burst mode. The two thresholds that can be set are the *HFBurstEntry* and *LFBursttEntry*. More details on how this configuration is done is shown in Section 7.5.3.3.

Figure 7-19describes the entry and exit behavior of UCC25660X in burst mode.

- The *HFBurstEntry*, corresponds to the *FBReplica* voltage at desired power level where the system enters HF Pulse skip.
- The *LFBurstEntry* corresponds to a modified *FBReplica* voltage at which the system enters LF Burst.
- When *FBreplica* is higher than HFBurstEntry, UCC25660x family operates in normal switching.
- When *FBreplica* is less than *HFBurstEntry* but greater than *LFBurstEntry*, UCC25660x family operates in HF pulse skip mode. In the HF pulse skip mode, the energy in each packet is still controlled by the control signal *FBReplica*.
- When *FBreplica* is less than *LFBurstEntry*, UCC25660X operates in LF burst mode. In the LF Burst mode, the energy in each packet is fixed at *LFBurstEntry* threshold.
- While operating in LF Burst mode, a new LF Burst segment is started when the *FBReplica* rises above the *LFBurstEntry* threshold. The segment is terminated when the desired number of packets are delivered and the *FBReplica* is below the *PacketStop* threshold.
- The desired number of packets in a LF Burst segment is computed to regulate the LF Burst operating frequency within 200Hz to 400Hz.
- In case of a sudden load drop, the LF Burst segment is immedialtelly terminated to avoid output over voltage condition.

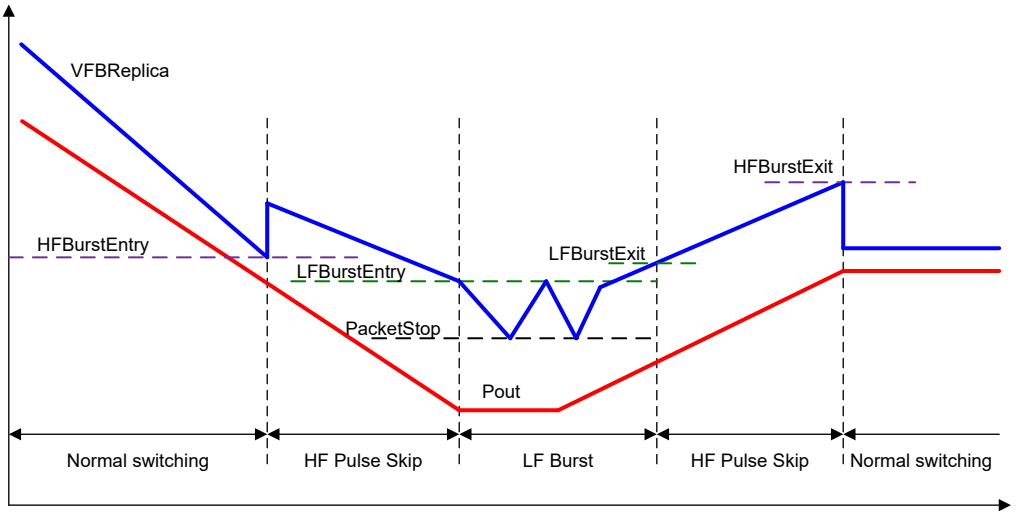

Figure 7-19. Burst Mode Determination from *FBReplica* Comparators

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7.5.3.3 Burst Mode Threshold Programming

Burst mode programming is set by external resistor divider connected to V5P. During the programming phase, a constant current I_{LLPrgm} is fed to the pin and the resulting voltage is measured via ADC (V_{LLA}) at time T_{LLPrgm}. After T_{Prgm}, I_{LLPrgm} is turned off and the voltage of the LL resistor divider is measured (V_{LLB}).

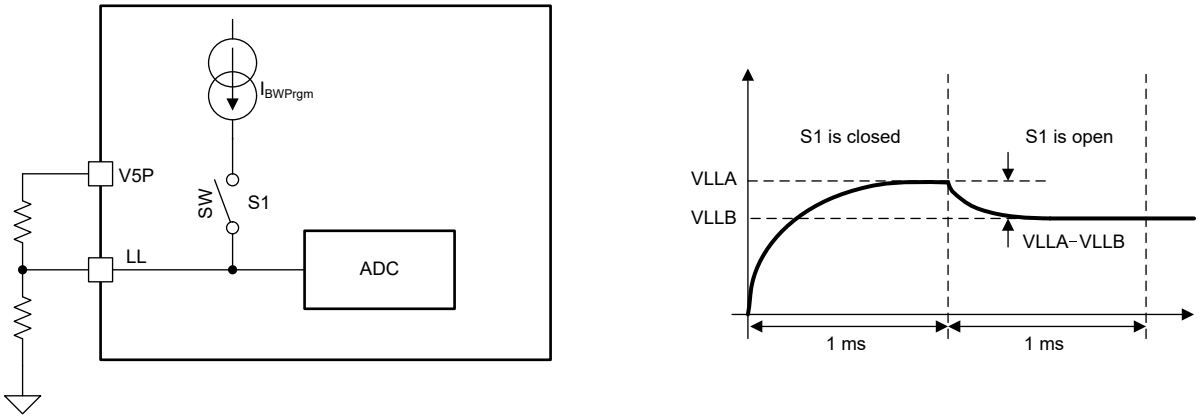

Figure 7-20. LL pin Programming

The voltage on the LL pin after switch S1 is off (V_{LLB}) is directly used to set the input power at which the system stops the LF Burst segment(*PacketStop*).

Based on the measured V_{LLB} voltage and the difference in voltage between V_{LLA} and V_{LLB}, the*FBReplica* voltage at which the controller enters HF Burst cant be determined. This can be calculated from the *PacketStop/ HFBurstEntry* ratio given in **TABLE** below. Apart from this, option to disable burst mode features itself is also provided.

The equation to claculate V_{LLA} - V_{LLB} is given below. where

$$V_{LLA} - V_{LLB} = (R_u||R_l)*I_{LLprgm} \quad (7)$$

$R_u||R_l = Rth$

The *FBReplica* at which the controllers starts the LF Burst segment is given below.

$$LFBurstEntry = PacketStop/0.6 \quad (8)$$

Table 7-2. Burst Mode Externally programable Settings

VLLA- VLLB (V)	PacketStop/HFBurstEntry ratio	Comment
>2.41	0.45	
2.185	NA	Burst disable
1.754	0.50	LF frequency range 200Hz to 400Hz
1.391	0.55	LF frequency range 200Hz to 400Hz
1.087	0.60	LF frequency range 200Hz to 400Hz
0.833	0.65	LF frequency range 200Hz to 400Hz
0.617	0.70	LF frequency range 200Hz to 400Hz
0.441	0.75	LF frequency range 200Hz to 400Hz
0.176	0.80	LF frequency range 200Hz to 400Hz

The ability to directly set the input power at which the system goes into various low power modes, dynamically disabling the burst mode enables an extra degree of freedom in the system design.

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7.5.3.4 PFC On/Off

PFC on/off logic uses the TSET pin. After the initial programming phase, TSET becomes a logic output pin expected to drive a small signal MOSFET (2N7002 for example). When UCC25660 enters LF Burst mode, the PFC on/off signal goes high. TSET pin voltage goes low when the controller exits LF Burst mode.

7.5.4 X-Capacitor Discharge

The HV pin is used for AC presence detection and X-Cap discharge.

7.5.4.1 Detecting Through HV Pin Only

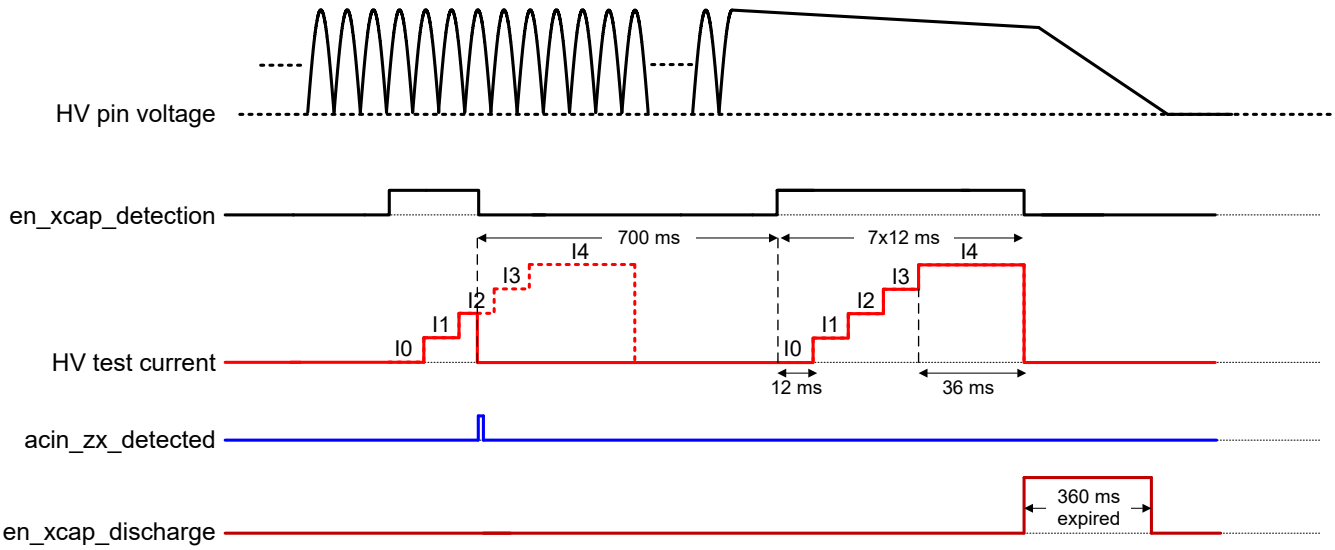

Figure 7-21. Zero Cross Detection Sequence HV Pin Only

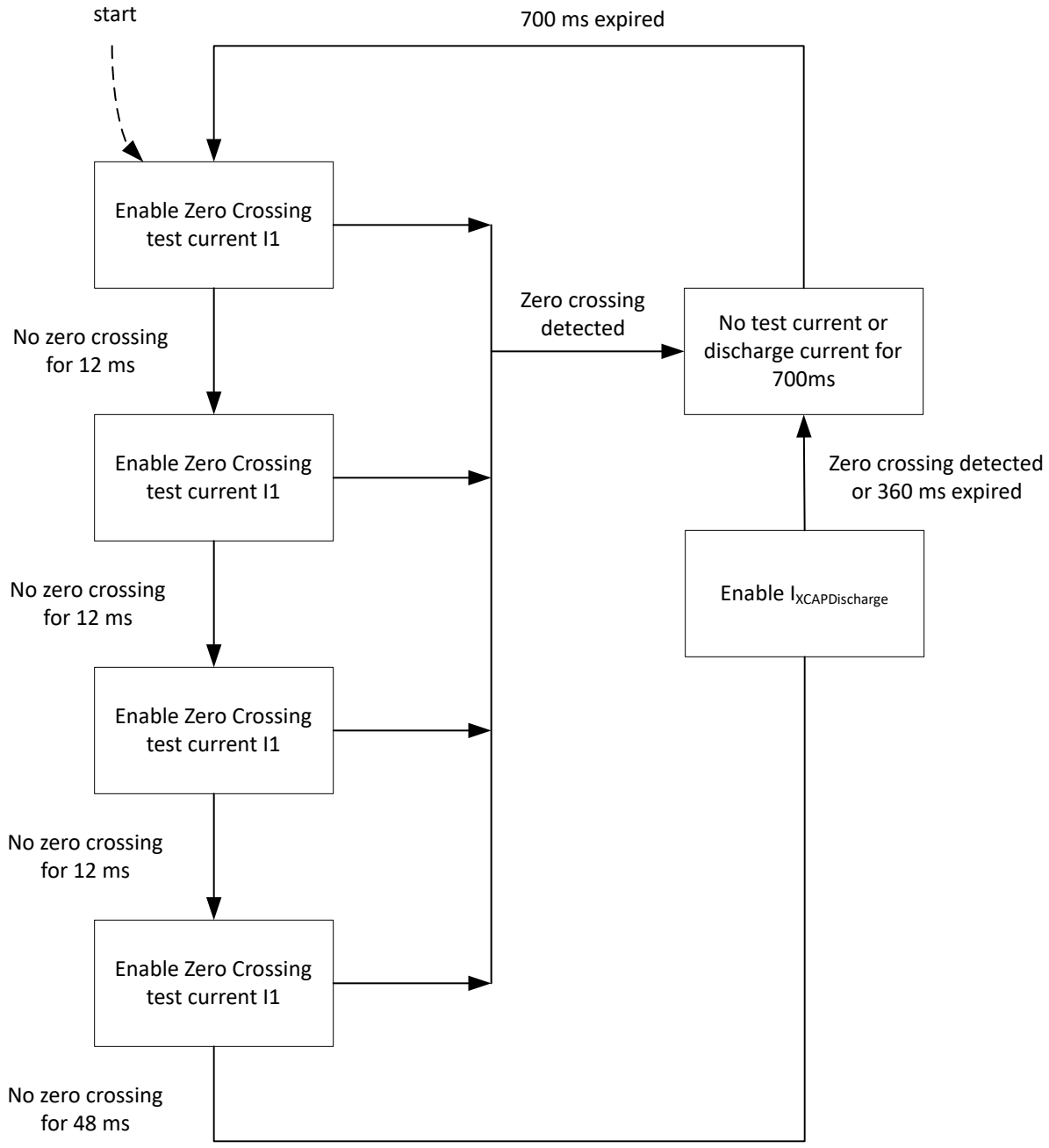

Figure 7-22. AC ZCD and X-Capacitor Discharge Flow Chart

1. Once every 700ms, the HV pin zero cross detection circuit gets engaged.
2. At first, HV pin test current is zero and the duration is 12ms. HV pin voltage is checked to see if the voltage is less than 9V threshold
3. If HV pin voltage does not falls below 9V, apply test current I1, and check again if HV pin voltage is less than 9V threshold
4. If HV pin voltage still not falls below 9V, continue to increase test current to I2 and then I3, I4
5. I4 test current's maximum on time is 36ms
6. If the HV pin voltage does not fall below 9V even after I4, the X-Cap discharge circuit is engaged for 360ms.
7. The minimal interval between two test current events is 700ms

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8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

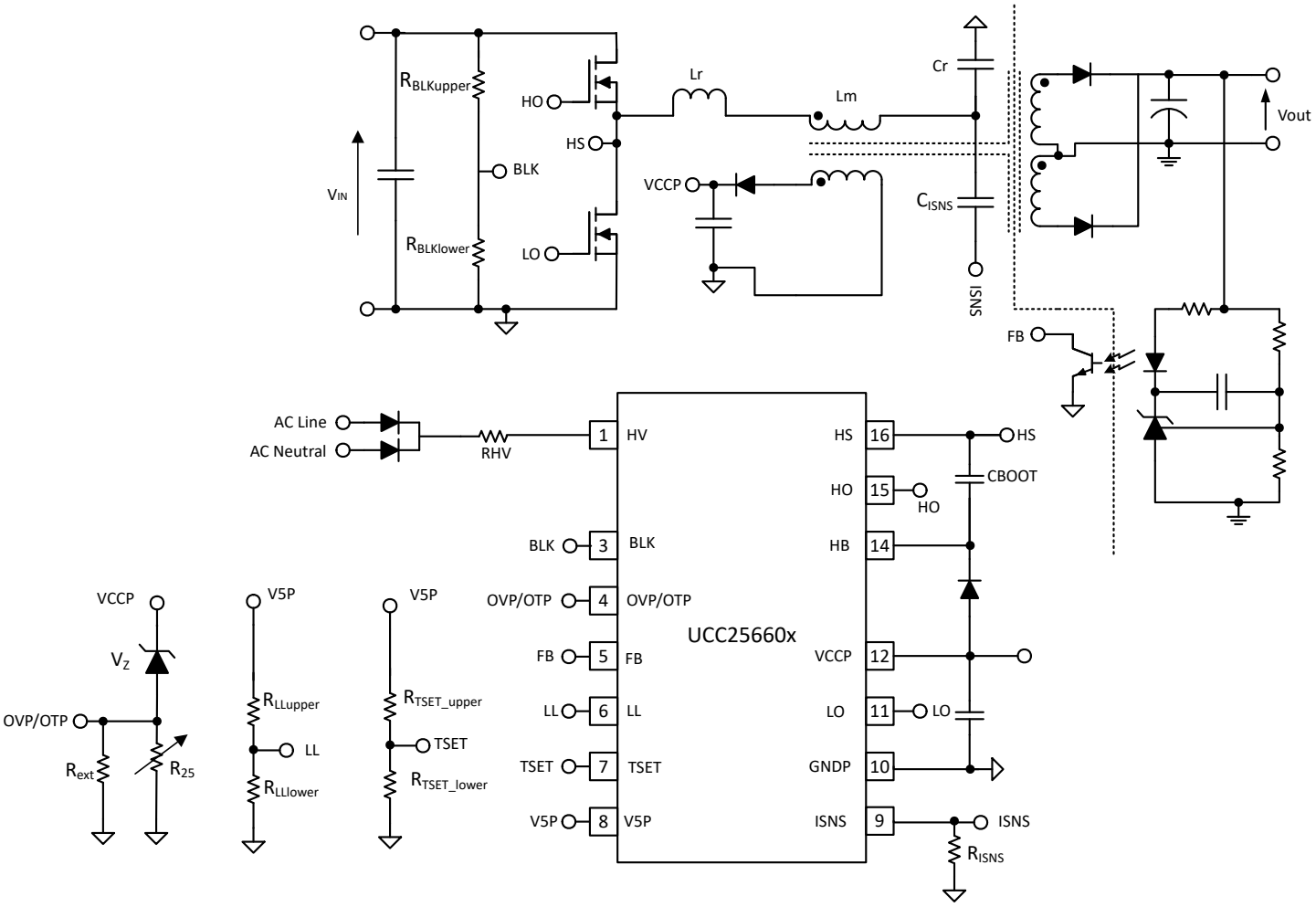
UC25660 can be used in a wide range of applications in which LLC topology is implemented. In order to make the part easier to use, TI has prepared a list of materials to demonstrate the features of the device:

- Full featured EVM hardware
- An excel design calculator
- Simulation models

In the following sections, a typical design example is presented.

8.2 Typical Application

Shown below is a typical half bridge LLC application using UC25660 as the controller.



8.2.1 Design Requirements

The design specifications are summarized in Table 8-1.

Table 8-1. System Design Specifications

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
INPUT CHARACTERISTICS					
DC Voltage range		365	390	410	VDC
AC Voltage range		85		264	VAC
AC Voltage frequency		47		63	Hz
Input DC UVLO On			365		VDC
Input DC UVLO Off			315		VDC
OUTPUT CHARACTERISTICS					
Output voltage, VOUT	No load to full load		12		VDC
Output load current, IOUT	360 VDC to 410 VDC			15	A
Output voltage ripple	390 VDC and full load = 10 A		120		mVpp
SYSTEMS CHARACTERISTICS					
Resonant Frequency			100		kHz
Peak efficiency	390 VDC		92		
Operating temperature	Natural convection		25		°C

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8.2.2 Detailed Design Procedure

8.2.2.1 LLC Power Stage Requirements

Start the design by deciding the LLC power stage component values. The LLC power stage design procedure outlined here follows the one given in the TI application note "Designing an LLC Resonant Half-Bridge Power Converters". The application note contains a full explanation of the origin of each of the equations used. The equations given below are based on the First Harmonic Approximation (FHA) method commonly used to analyze the LLC topology. This method gives a good starting point for any design, but a final design requires an iterative approach combining the FHA results, circuit simulation, and hardware testing. An alternative design approach is given in TI application note SLUA733, LLC Design for UCC29950.

8.2.2.2 LLC Gain Range

First, determine the transformer turns ratio by the nominal input and output voltages.

$$N_{PS} = \frac{V_{IN(nom)} / 2}{V_{OUT(nom)}} = \frac{390 / 2}{12} = 16.25 \Rightarrow 16.5 \tag{9}$$

Then determine the LLC gain range $M_{G(min)}$ and $M_{G(max)}$. Assume there is a 0.5V drop in the rectifier diodes (V_f) and an additional 0.5V due to other losses (V_{loss}).

$$M_{G(min)} = N_{PS} \frac{V_{OUT(min)} + V_f}{V_{IN(max)} / 2} = 16.5 \frac{12 + 0.5}{410 / 2} = 1.006 \tag{10}$$

$$M_{G(max)} = N_{PS} \frac{V_{OUT(max)} + V_f + V_{loss}}{V_{IN(min)} / 2} = 16.5 \frac{12 + 0.5 + 0.5}{365 / 2} = 1.175 \tag{11}$$

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8.2.2.3 Select L_n and Q_e

L_N is the ratio between the magnetizing inductance and the resonant inductance.

$$L_N = \frac{L_M}{L_R} \tag{12}$$

Q_E is the quality factor of the resonant tank.

$$Q_E = \frac{\sqrt{L_R / C_R}}{R_E} \tag{13}$$

In this equation, R_E is the equivalent load resistance.

Selecting L_N and Q_E values should result in an LLC gain curve, that intersects with $M_{G(min)}$ and $M_{G(max)}$ traces. The peak gain of the resulting curve should be larger than $M_{G(max)}$. Details of how to select L_N and Q_E are not discussed here. They are available in the Design calculator.

In this case, the selected L_N and Q_E values are:

$$L_N = 6 \tag{14}$$

$$Q_E = 0.3 \tag{15}$$

8.2.2.4 Determine Equivalent Load Resistance

Determine the equivalent load resistance by Equation 16.

$$R_E = \frac{8 \times N_{PS}^2}{\pi^2} \times \frac{V_{OUT(nom)}}{I_{OUT(nom)}} = \frac{8 \times 16.5^2}{\pi^2} \times \frac{12}{15} = 176.5\Omega \tag{16}$$

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8.2.2.5 Determine Component Parameters for LLC Resonant Circuit

Before determining the resonant tank component parameters, a nominal switching frequency (resonant frequency) should be selected. In this design, 100kHz is selected as the resonant frequency.

$$f_0 = 100\,kHz \tag{17}$$

The resonant tank parameters can be calculated as the following:

$$C_R = \frac{1}{2\pi \times Q_E \times f_0 \times R_E} = \frac{1}{2\pi \times 0.3 \times 100\,kHz \times 176.5\,\Omega} = 30.0\,nF \tag{18}$$

$$L_R = \frac{1}{(2\pi \times f_0)^2 C_R} = \frac{1}{(2\pi \times 100\,kHz)^2 \times 30.0\,nF} = 84.4\,\mu H \tag{19}$$

$$L_M = L_N \times L_R = 6 \times 84.4\,\mu H = 506.4\,\mu H \tag{20}$$

After the preliminary parameters are selected, find the closest actual component value that is available, re-check the gain curve with the selected parameters, and then run time domain simulation to verify the circuit operation.

The following resonant tank parameters are:

$$C_R = 30\,nF \tag{21}$$

$$L_R = 85\ \mu H \tag{22}$$

$$L_M = 510\,\mu H \tag{23}$$

Based on the final resonant tank parameters, the resonant frequency can be calculated:

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$$f_0 = \frac{1}{2\pi\sqrt{L_R C_R}} = \frac{1}{2\pi\sqrt{30\,nF \times 85\,\mu H}} = 99.7\,kHz \tag{24}$$

Based on the new LLC gain curve, the normalized switching frequency at maximum and minimum gain are given by:

$$f_{N(Mgmax)} = 0.7 \tag{25}$$

$$f_{N(Mgmin)} = 1.0 \tag{26}$$

The maximum and minimum switching frequencies are:

$$f_{SW(Mgmax)} = 69.8\,kHz \tag{27}$$

$$f_{SW(Mgmin)} = 99.7\,kHz \tag{28}$$

8.2.2.6 LLC Primary-Side Currents

The primary-side currents are calculated for component selection purposes. The currents are calculated based on a 110% overload condition.

The primary side RMS load current is given by:

$$I_{OE} = \frac{\pi}{2\sqrt{2}} \times \frac{I_o}{n} = \frac{\pi}{2\sqrt{2}} \times \frac{1.1 \times 15\,A}{16.5} = 1.111\,A \tag{29}$$

The RMS magnetizing current at minimum switching frequency is given by:

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$$I_M = \frac{2\sqrt{2}}{\pi} \times \frac{N_{PS} V_{OUT}}{\omega L_M} = \frac{2\sqrt{2}}{\pi} \times \frac{16.5 \times 12}{2\pi \times 64.8\,kHz \times 510\,\mu H} = 0.797\,A \quad (30)$$

The total current in resonant tank is given by:

$$I_R = \sqrt{I_M{}^2 + I_{OE}{}^2} = \sqrt{(1.111\,A)^2 + (0.797\,A)^2} = 1.367\,A \quad (31)$$

8.2.2.7 LLC Secondary-Side Currents

The total secondary side RMS load current is the current referred from the primary side current (I_{OE}) to the secondary side.

$$I_{OES} = N_{PS} \times I_{OE} = 16.5 \times 1.111\,A = 18.327\,A \quad (32)$$

In this design, the transformer's secondary side has a center-tapped configuration. The current of each secondary transformer winding is calculated by:

$$I_{WS} = \frac{\sqrt{2} \times I_{OES}}{2} = \frac{\sqrt{2} \times 18.327\,A}{2} = 12.959\,A \quad (33)$$

The corresponding half-wave average current is:

$$I_{SAV} = \frac{\sqrt{2} \times I_{OES}}{\pi} = \frac{\sqrt{2} \times 18.327\,A}{\pi} = 8.250\,A \quad (34)$$

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8.2.2.8 LLC Transformer

A bias winding is needed in order to utilize the HV self start up function. It is recommended to design the bias winding so that the VCC voltage is greater than 12V.

The transformer can be built or purchased according to these specifications:

- Turns ratio: Primary : Secondary : Bias = 33 : 2 : 2
- Primary terminal voltage: 450V_{pk}
- Primary magnetizing inductance: L_M = 510µH
- Primary side winding rated current: I_R = 1.367A
- Secondary terminal voltage: 36 V_{pk}
- Secondary winding rated current: I_{WS} = 12.959A
- Minimum switching frequency: 69.8kHz
- Maximum switching frequency: 99.7kHz
- Insulation between primary and secondary sides: IEC60950 reinforced insulation

The minimum operating frequency during normal operation is calculated above. Please note that for some applications that operate as a wide input LLC where the PFC may be shut off in standby mode, the operating frequency may be much lower during heavy load shutdown and the LLC can operate at just above the ZCS boundary which is a lower frequency. The magnetic components in the resonant circuit, the transformer and resonant inductor, should be rated to operate at this lower frequency.

8.2.2.9 LLC Resonant Inductor

The AC voltage across the resonant inductor is given by its impedance multiplied by the current:

$$V_{L_R} = \omega L_R I_R = 2\pi \times 69.8\text{kHz} \times 85\mu\text{H} \times 1.367\text{A} = 50.946V \tag{35}$$

The inductor can be built or purchased according to the following specifications:

- Inductance: L_R = 85µH
- Rated current: I_R = 1.367A
- Terminal AC voltage: 50.946V
- Frequency range: 69.8kHz to 99.7kHz

Please note some designs may utilize the leakage inductance of the transformer as the resonant inductance and do not require an external resonant inductor.

8.2.2.10 LLC Resonant Capacitor

This capacitor carries the full-primary current at the switching frequency. A low dissipation factor capacitor is needed to prevent overheating.

The AC voltage across the resonant capacitor is given by its impedance multiplied by the current.

$$V_{CR} = \frac{I_R}{\omega C_R} = \frac{1.367\text{A}}{2\pi \times 69.8\text{kHz} \times 30\text{nF}} = 104.0\,V \tag{36}$$

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$$V_{CR(rms)} = \sqrt{\left(\frac{V_{IN(max)}}{2}\right)^2 + V_{CR}^2} = \sqrt{\left(\frac{410}{2}\right)^2 + 104.0^2} = 229.9\,V \quad (37)$$

Peak voltage:

$$V_{CR(peak)} = \frac{V_{IN(max)}}{2} + \sqrt{2}V_{CR} = \frac{410}{2} + \sqrt{2} \times 104.0 = 352.0\,V \quad (38)$$

Valley voltage:

$$V_{CR(valley)} = \frac{V_{IN(max)}}{2} - \sqrt{2}V_{CR} = \frac{410}{2} - \sqrt{2} \times 104.0 = 58.0\,V \quad (39)$$

Rated current:

$$I_R = 1.367\,A \quad (40)$$

8.2.2.11 LLC Primary-Side MOSFETs

Each MOSFET sees the input voltage as its maximum applied voltage. Choose the MOSFET voltage rating to be 1.5 times of the maximum bulk voltage:

$$V_{QLLC(peak)} = 1.5 \times V_{IN(max)} = 615\,V \quad (41)$$

Choose the MOSFET current rating to be 1.1 times of the maximum primary side RMS current:

$$I_{QLLC} = 1.1 \times I_R = 1.504\,A \quad (42)$$

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8.2.2.12 Design Considerations for Adaptive Dead-Time

After the resonant tank is designed and the primary side MOSFET is selected, the ZVS operation of the converter needs to be double checked. ZVS can only be achieved when there is enough current left in the resonant inductor at the gate turn off edge to discharge the switch node. UC256604 implements adaptive dead-time based on the slewing of the switch node. The slew detection circuit has a detection range of 0.1V/ns to 200V/ns.

To check the ZVS operation, a series of time domain simulations are conducted, and the resonant current at the gate turn off edges are captured. An example plot is shown below:

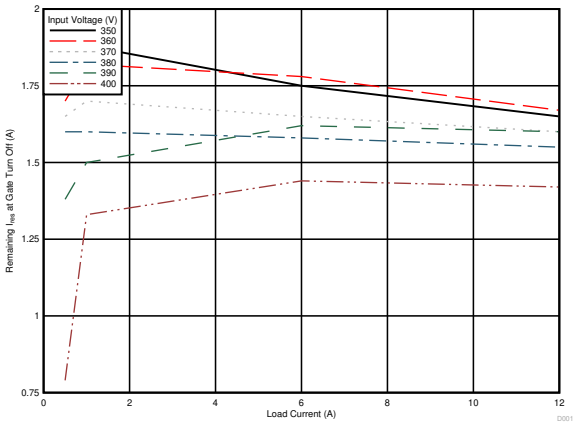

Figure 8-1. Adaptive Dead-Time

The figure above assumes the maximum switching frequency occurs at 5% load, and system starts to burst at 5% load.

From this plot, the minimum resonant current left in the tank is I_{min} = 0.8A in the interested operation range. In order to calculate the slew rate, the primary side switch node parasitic capacitance must be known. This value can be estimated from the MOSFET datasheet. In this case, $C_{switchnode}$ = 400pF. The minimum slew rate is given by:

$$\frac{I_{MIN}}{C_{switchnode}} = \frac{0.8\,A}{400\,pF} = 2V\,/\,ns \tag{43}$$

This is larger than 0.1V/ns minimum detectable slew rate.

8.2.2.13 LLC Rectifier Diodes

The voltage rating of the output diodes is given by:

$$V_{DB} = 1.2 \times \frac{V_{IN(max)}}{N_{PS}} = 1.2 \times \frac{410}{16.5} = 29.82V \tag{44}$$

The current rating of the output diodes is given by:

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$$I_{SAV} = \frac{\sqrt{2} \times I_{OES}}{\pi} = \frac{\sqrt{2} \times 18.329}{\pi} = 8.250\,A \tag{45}$$

8.2.2.14 LLC Output Capacitors

The LLC converter topology does not require an output filter although a small second stage filter inductor may be useful in reducing peak-to-peak output noise. Assuming that the output capacitors carry the rectifier's full wave output current then the capacitor ripple current rating is:

$$I_{RECT} = \frac{\pi}{2\sqrt{2}} I_{OUT} = \frac{\pi}{2\sqrt{2}} \times 15 = 16.66\,A \tag{46}$$

Use 20V rating for 12V output voltage:

$$V_{LLCcap} = 20\,V \tag{47}$$

The capacitor's RMS current rating is:

$$I_{C(out)} = \sqrt{\left(\frac{\pi}{2\sqrt{2}} I_{OUT}\right)^2 - I_{OUT}^2} = \sqrt{\left(\frac{\pi}{2\sqrt{2}} \times 15\right)^2 - 15^2} = 7.251A \tag{48}$$

Solid Aluminum capacitors with conductive polymer technology have high ripple-current ratings and are a good choice, especially if the design is required to operate at colder temperatures. The ripple-current rating for a single capacitor may not be sufficient so multiple capacitors are often connected in parallel.

The ripple voltage at the output of the LLC stage is a function of the amount of AC current that flows in the capacitors. To estimate this voltage, assume that all the current, including the DC current in the load, flows in the filter capacitors.

$$ESR_{max} = \frac{V_{OUT(pk-pk)}}{I_{RECT(pk)}} = \frac{0.12V}{2\frac{\pi}{4} \times 15\,A} = 5.1m\Omega \tag{49}$$

The capacitor specifications are:

- Voltage rating: 20V

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- Ripple current rating: 7.251A
- ESR: < 5.1mΩ

8.2.2.15 HV Pin Series Resistors

Multiple resistors are connected in series with HV pin to limit the power dissipation of the UC25660 device. The recommended series resistor with HV pin is 5kΩ.

8.2.2.16 BLK Pin Voltage Divider

BLK pin senses the LLC DC input voltage and determines when to turn on and off the LLC converter. Also, BLK pin voltage is used for feedforward compensation.

The desired power consumption of the BLK pin resistor divider is P_{BLKsns} = 15mW. The BLK sense resistor total value is given by:

$$R_{BLKsns} = R_{BLKupper} + R_{BLKlower} = \frac{V_{IN(nom)}^2}{P_{BLKsns}} = \frac{390^2}{0.015} = 10M\Omega \quad (50)$$

Choose LLC startup voltage as 365V. Then $V_{BLKStart}$ related to $V_{BLKStop}$, $V_{BLKStartHys}$, $I_{BLKSink}$ as below:

$$V_{BLKStart}\left(\frac{R_{BLKlower}}{R_{BLKupper} + R_{BLKlower}}\right) = V_{BLKStop} + V_{BLKStartHys} + I_{BLKsink}\left(\frac{R_{BLKupper}R_{BLKlower}}{R_{BLKupper} + R_{BLKlower}}\right) \quad (51)$$

For $V_{BLKStop}$= 1V, $V_{BLKStartHys}$= 0.1V, $I_{BLKSink}$= $5\mu A$, $R_{BLKupper}$ and $R_{BLKlower}$ are obtained as $10M\Omega$ and $35.4k\Omega$ respectively.

A standard value of 35.4kΩ is selected for $R_{BLKlower}$ and a standard value of 3x 3.3MΩ in series is selected for $R_{BLKupper}$.

The actual startup voltage is given by

$$V_{BLKStart}\left(\frac{R_{BLKupper} + R_{BLKlower}}{R_{BLKlower}}\right) = \begin{pmatrix} V_{BLKStop} + V_{BLKStartHys} + \\ I_{BLKSink}\left(\frac{R_{BLKupper}R_{BLKlower}}{R_{BLKupper} + R_{BLKlower}}\right) \end{pmatrix} \cdot \left(\frac{R_{BLKupper} + R_{BLKlower}}{R_{BLKlower}}\right) = 358V \quad (52)$$

The power consumption in BLK resistors are given by

$$P_{BLKsns} = \frac{V_{IN(nom)}^2}{(R_{BLKupper} + R_{BLKlower})} = \frac{390^2}{(10M\Omega + 35.4k\Omega)} = 15.3mW \quad (53)$$

The LLC turn off voltage is given by

$$V_{BLKStop}\left(\frac{R_{BLKupper} + R_{BLKlower}}{R_{BLKlower}}\right) = 280.6V \quad (54)$$

8.2.2.17 ISNS Pin Differentiator

The ISNS pin senses the resonant current through a Differentiator. The ISNS pin together with TSET, BLK pin resistors set the overload protection level. The typical threshold voltage of overload protection (V_{FBOPP}) is 4.75V. The ISNS pin also sets the over current protection level (OCP1). The threshold value of OCP1 is either 3.5V or 4V depending on the TSET pin resistors.

The peak ISNS pin voltage at full load

$$V_{ISNSpeak} = \sqrt{2}I_r = \sqrt{2} \times 1.367 = 1.933V \quad (55)$$

Select a current sense capacitor first, since there are less high voltage capacitor choices than resistors:

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$$C_{ISNS} = 150pF \tag{56}$$

For this design, TSET option #4 (Refer Section 8.2.2.18) is selected. This makes the over current protection threshold as

$$OCP1_Threshold = 3.5V \tag{57}$$

Then calculate the required ISNS resistor value:

$$R_{ISNS} < \frac{OCP1_Threshold \cdot C_r}{V_{ISNSpeak} \cdot C_{ISNS}} = \frac{3.5V \cdot 30nF}{1.933V \cdot 150pF} = 329\Omega \tag{58}$$

$R_{ISNS} = 205\Omega$ is selected.

The ISNS pin resistor can also be selected based on the $V_{FBreplica}$ voltage for a given output power. It's value should be chosen such that, at rated power, the FBReplica should be below V_{FBOPP} as shown in Figure 8-2.

8.2.2.18 TSET Pin

The TSET pin voltage is used to set the VCR integrator time constants and the minimum switching frequency. Depending on the selected option, OCP1 threshold, Timer gain (k_s), Integrator component values (R_{VCR}, R_{RAMP}, C_{VCR}), maximum dead time would be set.

For this design, TSET option #4 is selected. So, for option #4, TSET pin voltage needs to be between 0.742V to 0.850V as given in table TSET Programming Options table . A 1M ohm (R_{TSET_upper}) and a 191kΩ (R_{TSET_lower}) are used at the TSET pin. Then the TSET pin voltage will be

$$V_{TSET} = \frac{R_{TSET_lower} \cdot V5P}{R_{TSET_upper} + R_{TSET_lower}} = \frac{191k \cdot 5}{191k + 1M} = 0.8V \tag{59}$$

Then the Equation 4 will become

$$FBReplica = 0.0076P_{in} + 1.7364 \tag{60}$$

where previously chosen values of R_{ISNS}, C_{ISNS}, C_R, $R_{BLKupper}$, $R_{BLKlower}$, Integrator time constants values of TSET option #4 are used to obtain this relation.

Here for calculating P_{in}, 92% efficiency is considered in the following expression.

$$P_{in} = \frac{P_{out}}{\eta} \tag{61}$$

Figure 8-2 shows the FBReplica voltage with respect to the input power of the LLC.

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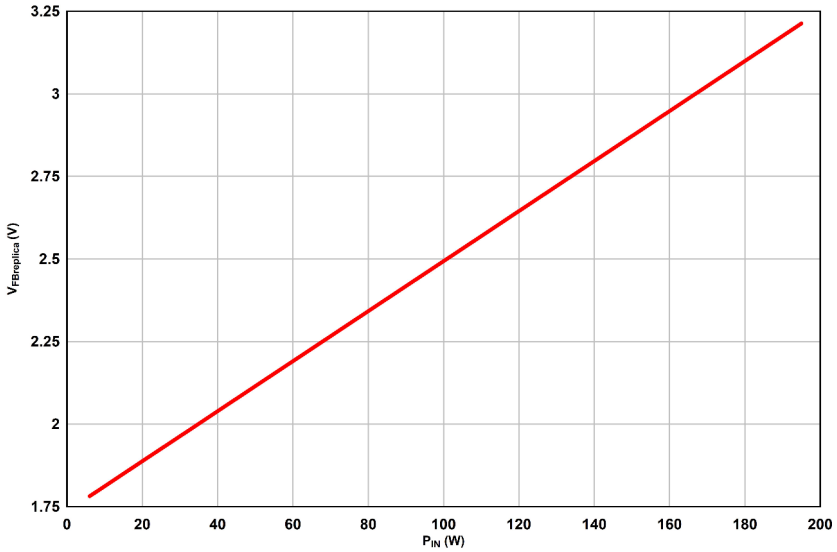

Figure 8-2. FBReplica vs P_{in}

The FBReplica voltage can be measured by inserting a 10-kΩ resistor between the feedback optocoupler emitter and ground. Assume the voltage measured on the 10-kΩ resistor is V_{10k}. Then FBReplica voltage can be calculated as:

$$FBReplica = \left(I_{FB} - \frac{V_{10k\Omega}}{10k\Omega}\right) \times R_{FBInternal} \quad (62)$$

8.2.2.19 OVP/OTP Pin

The OVP/OTP is used for protecting the power stage from over voltage. Also, the same pin is also used for over temperature protection using negative temperature coefficient (NTC) thermistor. As the bias winding voltage is the mirror image of the output voltage through the turns ratio of the transformer, pulling up this pin with a zener diode is a convenient approach to set the OVP on the primary side. In this design, the nominal output voltage is 12V. Both the bias winding and the secondary side winding has 2 turns. Assuming there is a 0.5V drop in the rectifier diodes (Vf) and a further 0.5V drop due to other losses (Vloss), the nominal voltage of the bias winding is given by:

$$V_{BiasWindingNom} = (12 + 0.5 + 0.5) \cdot \frac{N_{aux}}{N_2} = (12 + 0.5 + 0.5) \cdot \frac{2}{2} = 13V \quad (63)$$

The desired OVP threshold in this design is 140% of the nominal value. The OVP threshold level (V_{OVPpos}) in UC25660 device is 3.5V.

The required voltage rating of the Zener diode is then given by:

$$V_z = (1.4 \cdot V_{out} + V_{drop}) \cdot \frac{N_{aux}}{N_2} - V_{OVPpos} = (1.4 \cdot 12 + 0.5 + 0.5) \cdot \frac{2}{2} - 3.5 = 14.3V \quad (64)$$

Assume actual voltage rating of Zener used is 15V.

Then actual output voltage at which OVP will be triggered is

$$V_{out_ovp} = (V_z + V_{OVPpos}) \cdot \frac{N_2}{N_{aux}} - V_{drop} = (15 + 3.5) \cdot \frac{2}{2} - 1 = 17.5V = 146\% \cdot V_{out} \quad (65)$$

During normal operation, the voltage of the OVP/OTP pin should be within the working window of 0.8V to 3.5V. For over temperature protection, the OVP/OTP pin should be pulled down below OTP threshold of 0.8V.

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At room temperature, the OVP/OTP pin voltage is considered as 1.4V. So, at room temperature, the effective resistance value at this pin should be

$$R_{OVP/OTP_25} = \frac{1.4V}{I_{OVP_OTP}} = \frac{1.4V}{100 \cdot 10^{-6}A} = 14k\Omega \quad (66)$$

$$R_{OVP/OTP_25} = \frac{R_{ext} \cdot R_{NTC_25}}{R_{ext} + R_{NTC_25}} = 14k\Omega \quad (67)$$

where R_{ext} is external resistor that is in parallel with the thermistor. And R_{NTC_25} is resistance value of the thermistor at the room temperature.

For this design, over temperature protection is set at the 110^0C. So based on the availability and temperature coefficient of NTCs,

$$\frac{R_{NTC_110}}{R_{NTC_25}} = 0.035263 \quad (68)$$

(refer B57371V2474J060 Datasheet) is chosen. Here R_{NTC_110} is the resistance of the thermistor at the 110^0C.

For OTP trigger, the OVP/OTP pin voltage should be below 0.8V.

$$R_{OVP/OTP_110} = \frac{0.8V}{I_{OVP_OTP}} = \frac{0.8V}{100 \cdot 10^{-6}A} = 8k\Omega \quad (69)$$

$$R_{OVP/OTP_110} = \frac{R_{ext} \cdot R_{NTC_110}}{R_{ext} + R_{NTC_110}} = 8k\Omega \quad (70)$$

From equations,Equation 67, Equation 68, Equation 70, R_{NTC_25} and R_{ext} are obtained as 510kΩ and 14.4kΩ. So, finally R_{NTC_25}=470kΩ (Manfacturer part number: B57371V2474J060) and R_{ext}=15kΩ are chosen.

So, at room temperature, with new chosen resistors, the OVP/OTP voltage will be

$$R_{OVP/OTP_25} \cdot I_{OVP_OTP} = \left(\frac{15k \cdot 470k}{15k + 470k}\right) \cdot 100 \cdot 10^{-6} = 1.454V \quad (71)$$

At 110^0C, the OVP/OTP voltage will be

$$R_{OVP/OTP_110} \cdot I_{OVP_OTP} = \left(\frac{15k \cdot (470k \cdot 0.035263)}{15k + (470k \cdot 0.035263)}\right) \cdot 100 \cdot 10^{-6} = 0.78V \quad (72)$$

8.2.2.20 Burst Mode Programming

The LL pin voltage (VLLB) and the resistor divider that connected to the LL pin allow the designer to set the HFBurstEntry and LFBurstEntry thresholds as shown below.

$$VLLB = \frac{R_{LL_lower} \cdot V5P}{R_{LL_upper} + R_{LL_lower}} \quad (73)$$

$$VLLA = VLLB + \frac{R_{LL_lower} R_{LL_upper}}{R_{LL_upper} + R_{LL_lower}} \cdot I_{LLPrgm} \quad (74)$$

As shown in Table 7-2, (VLLA-VLLB) voltage determines the VLLB/HFBurstEntry ratio.

For this design, (VLLB/HFBurstEntry) = 0.55 is considered. So, Max voltage of (VLLA-VLLB) should be below 1.391V.

Then HFBurstEntry is related to LL pin voltage as below:

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$$HFBurstEntry = \frac{VLLB}{0.55} = 1.818 \cdot VLLB \quad (75)$$

The LFBurstEntry is always related to LL pin voltage as below:

$$LFBurstEntry = \frac{VLLB}{0.6} = 1.667 \cdot VLLB \quad (76)$$

For this design, VLLB= 1V and VLLA=(Max voltage of (VLLA-VLLB))-0.1V are considered. By substituting these values in Equation 73, Equation 74, $R_{LLupper}$, $R_{LLlower}$ can be obtained as 641k and 161k respectively.

Finally $R_{LLupper}$= 549kΩ and $R_{LLlower}$=140kΩ are chosen for this design.

Then final burst entries will be calculated as below.

$$VLLB = \frac{140k \cdot 5}{140k + 549k} = 1.016V \quad (77)$$

$$VLLA = 1.016V + \frac{140k \cdot 549k}{140k + 549k} \cdot 10\mu A = 2.131V \quad (78)$$

$$VLLA - VLLB = 1.116V \quad (79)$$

$$HFBurstEntry = 1.818 \cdot 1.016 = 1.847V \quad (80)$$

$$LFBurstEntry = 1.667 \cdot 1.016 = 1.693V \quad (81)$$

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8.2.2.21 Application Curves

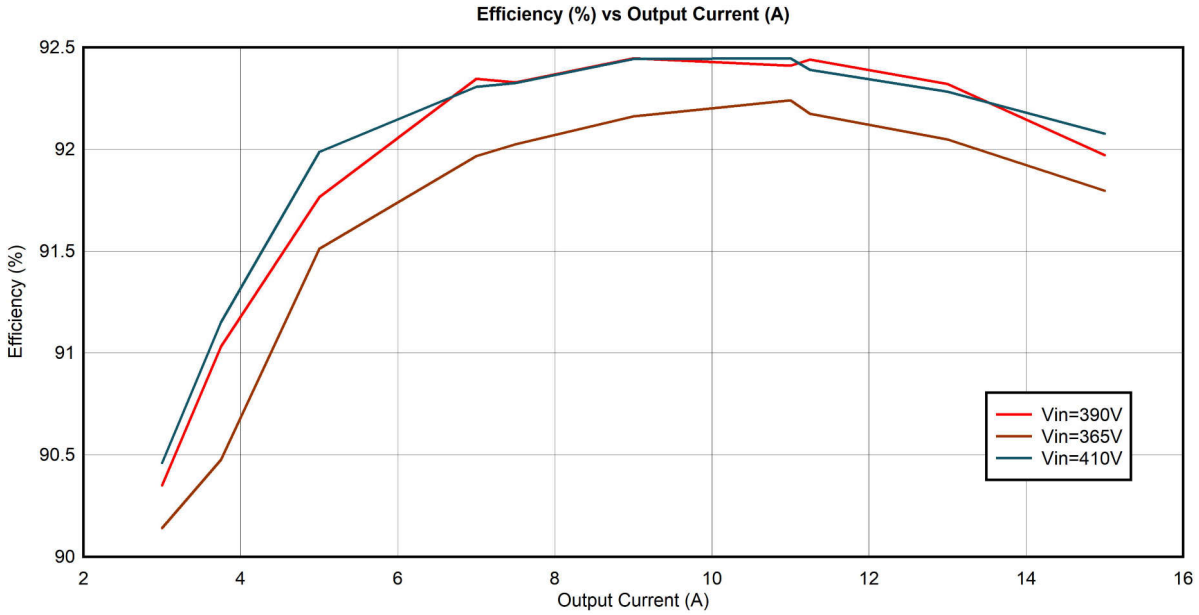

Figure 8-3. Efficiency

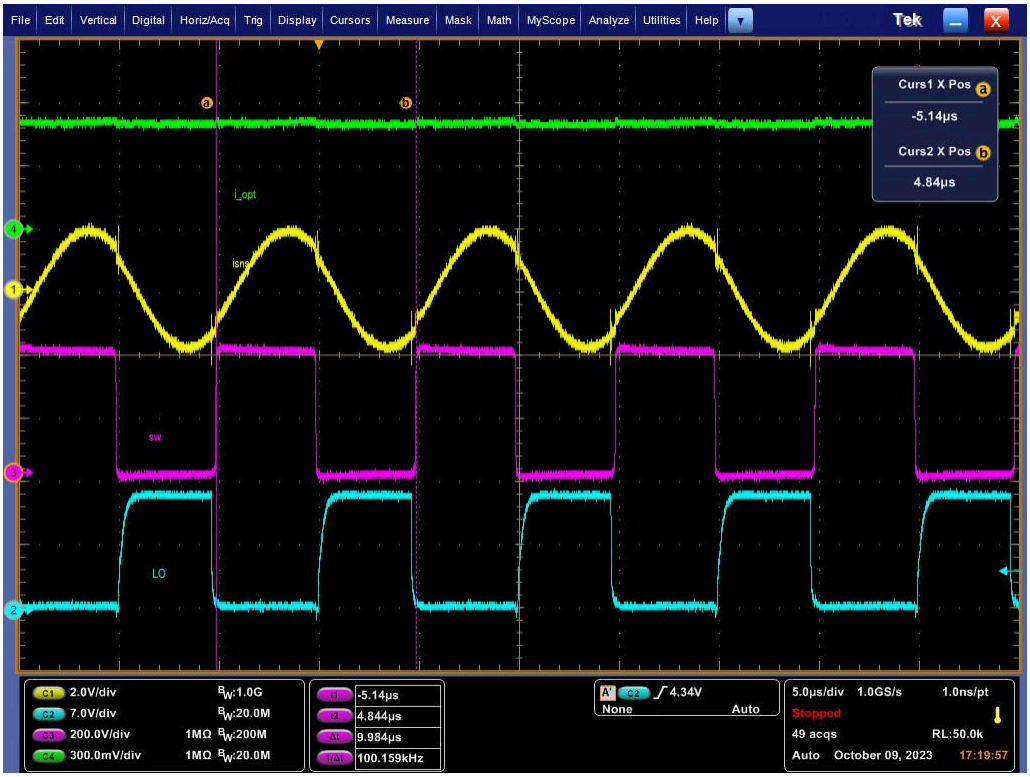

Figure 8-4. Steady State Waveforms (Ch1 = ISNS, Ch2 = LO, Ch3 =SW, Ch4 = opto coupler collector series resistance's voltage)

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8.3 Power Supply Recommendations

8.3.1 VCCP Pin Capacitor

The VCCP capacitor must be selected with a value high enough to guarantee that during the LF Burst operation, VCCP won't fall below the $VCC_{StopSwitching}$ level.

Choose at least 100µF capacitor or combination of capacitors.

8.3.2 Boot Capacitor

During LF burst off period, power consumed by the high-side gate driver from the HB pin must be drawn from C_{BOOT} and will cause its voltage to decay. At the start of the next burst period there must be sufficient voltage remaining on C_{BOOT} to power the high-side gate driver until the conduction period of LO allows it to be replenished from C_{VCCP}. The power consumed by the high-side driver during this burst off period will therefore have a direct impact on the size and cost of capacitors that must be connected to HB and VCCP.

Assume the system has a maximum burst off period of 150ms and the bootstrap diode has a forward voltage drop of 1V. Target a minimum bootstrap voltage of 8V to avoid UVLO fault. The maximum allowable voltage drop on the boot capacitor is:

$$V_{bootmaxdrop} = V_{VCCP} - V_{bootforwarddrop} - 8V = 12V - 1V - 8V = 3V \quad (82)$$

Boot capacitor can then be sized:

$$C_B = \frac{I_{BOOT_QUIESCENT}}{V_{bootmaxdrop}} = \frac{60\mu A \times 150ms}{3V} = 3uF \quad (83)$$

8.3.3 V5P Pin Capacitor

This pin should be externally connected to a decoupling capacitor to GND. Since the load on this pin is very small, a small decoupling capacitor of 1µF to 4.7µF would be sufficient.

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8.4 Layout

8.4.1 Layout Guidelines

- Put a 2.2µF ceramic capacitor on VCCP pin in addition to the energy storage electrolytic capacitor. The 2.2µF ceramic capacitor should be put as close as possible to the VCC pin.
- Minimum recommended boot capacitor, C_B, is 0.1µF. The minimum value of the boot capacitor needs to be determined by the minimum burst frequency. The boot capacitor should be large enough to hold the bootstrap voltage during the lowest burst frequency. Please refer to the boot leakage current in the electrical table.
- Signal ground and power ground should be single-point connected. Power ground is recommended to connect to the negative terminal of the LLC input bulk capacitor.
- The filtering capacitors for ISNS, BLK, LL, BW/OTP should be put as close as possible to the pins.
- FB trace should be as short as possible
- Use film capacitors or C0G, NP0 ceramic capacitors for the ISNS capacitor for low distortion
- Add necessary filtering capacitors on the VCCP pin to filter out the high spikes on the bias winding waveform.
- Keep necessary high voltage clearance and creepage.
- If 2kV HBM ESD rating is needed on HV pin, it is acceptable to place a 100pF capacitor from the HV pin to ground in order to pass up to 2kV HBM ESD.

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8.4.2 Layout Example

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8.4.2.1 Schematics

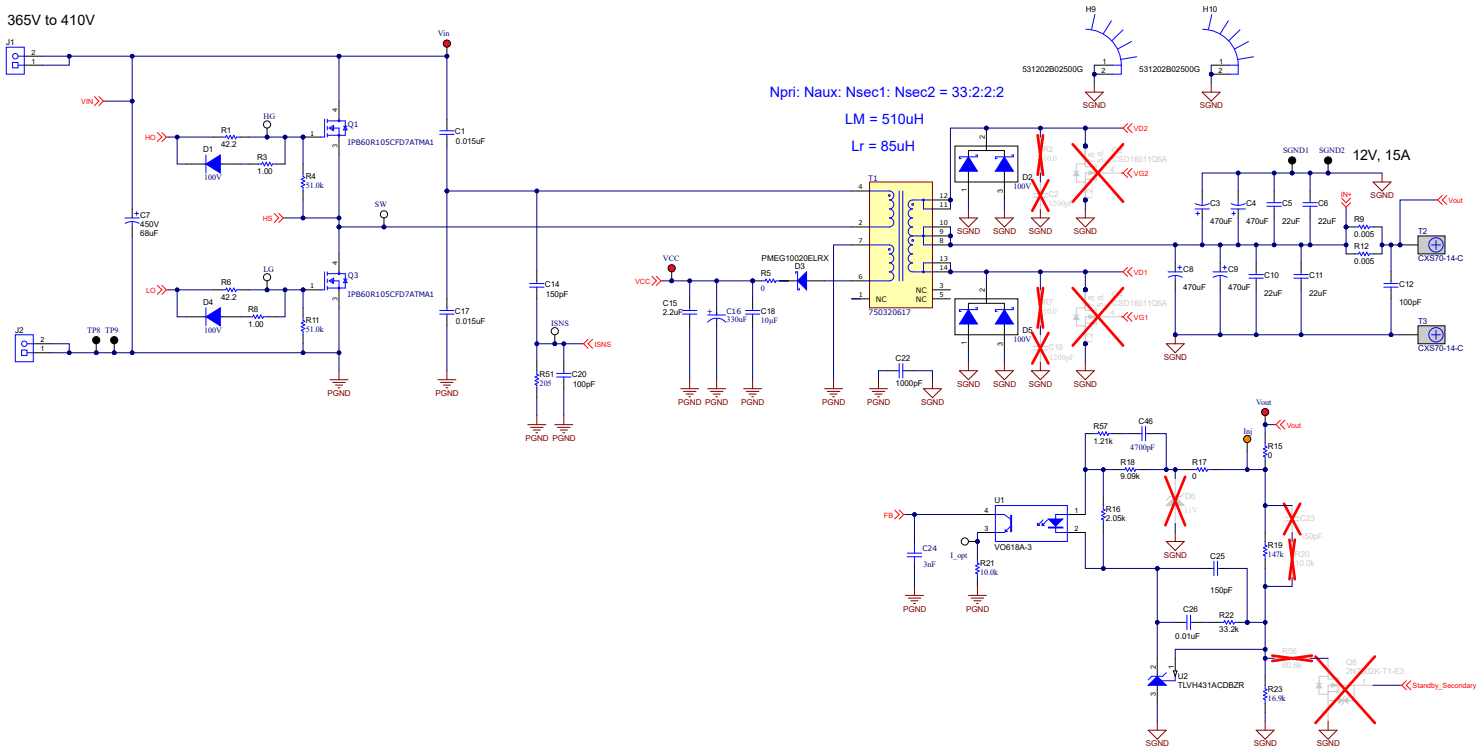

Figure 8-5. UCC25660EVM-064 Power Stage Schematic

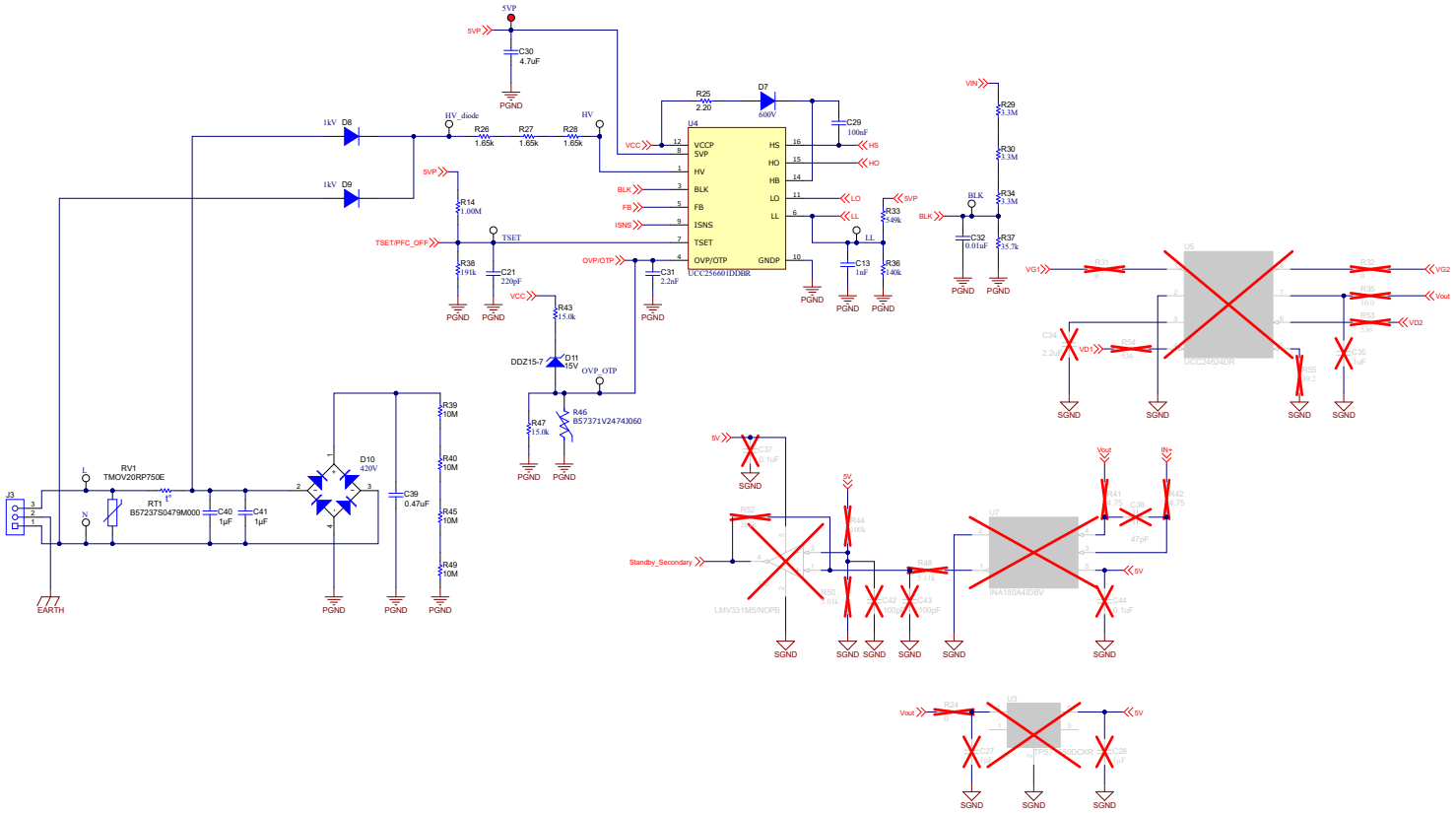

Figure 8-6. UCC25660EVM-064 Control Schematic

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8.4.2.2 Schematics

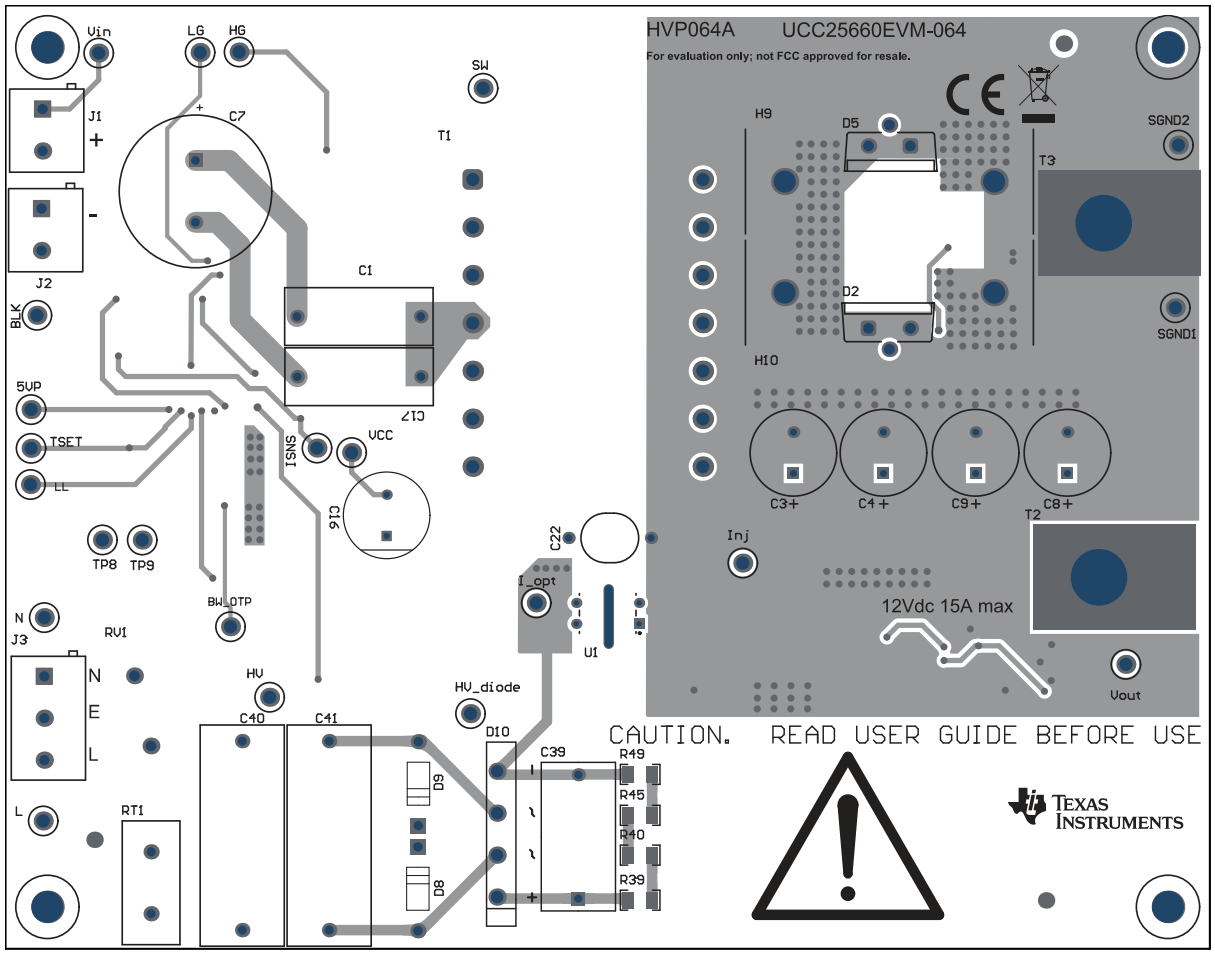

Figure 8-7. UCC25660EVM-064 (Top View)

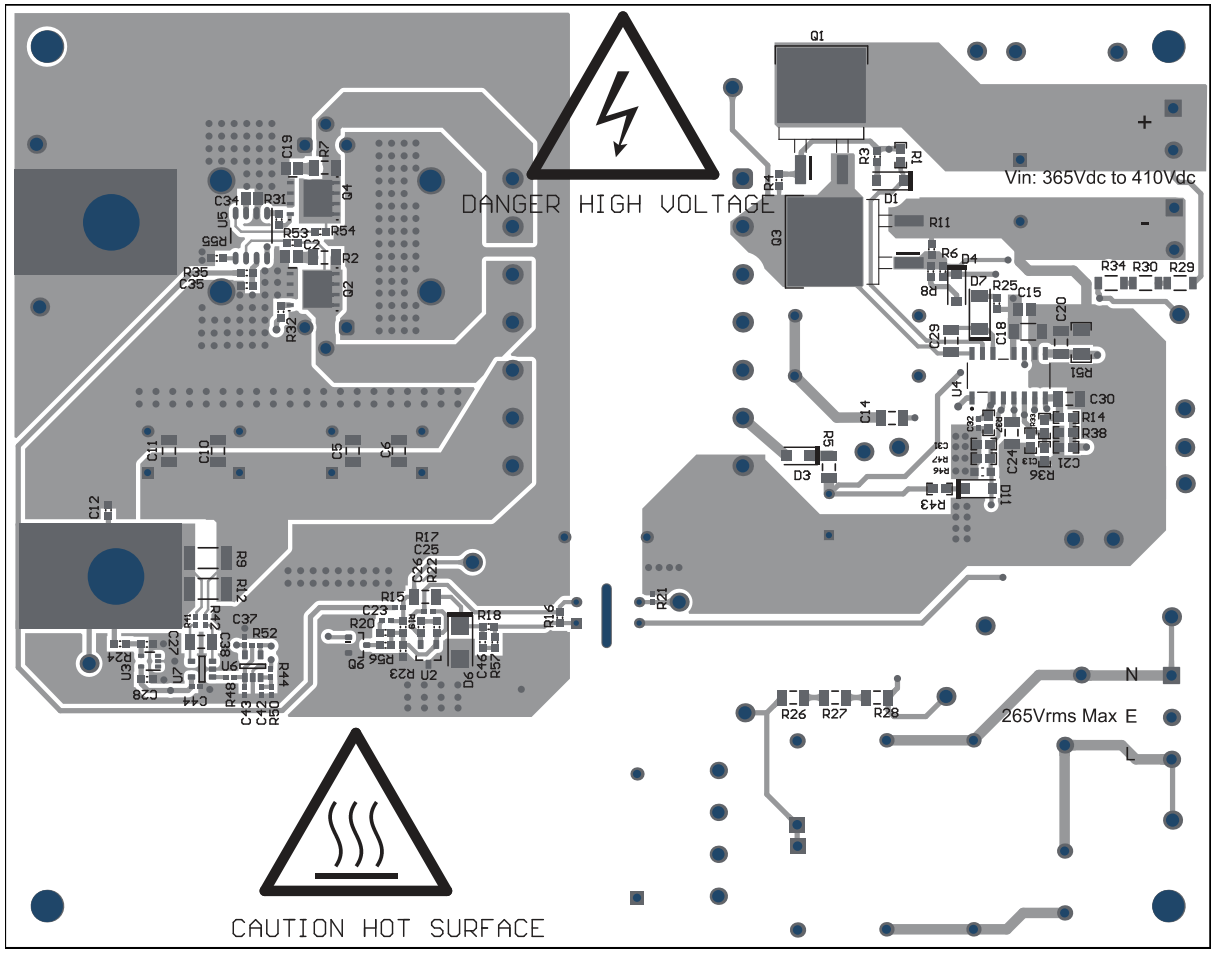

Figure 8-8. UCC25660EVM-064 (Bottom View)

9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (November 2023) to Revision B (July 2024)	Page
• Added UCC256602, UCC256603 and the UCC256604 oderable options	1
• Added UCC256601, UCC256602, UCC256603, an the UCC256604 orderable options to the Device Comparason Table	3
• Added UCC256601, UCC256602, UCC256603, an the UCC256604 orderable options to the specification tables	5

Changes from Revision * (October 2023) to Revision A (December 2023)	Page
• Changed Marketing status from Advance Information to Production Data	1

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10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
PUCC256601DDBR	Active	Preproduction	SOIC (DDB) | 14	2500 | LARGE T&R	-	Call TI	Call TI	-40 to 125	
PUCC256601DDBR.A	Active	Preproduction	SOIC (DDB) | 14	2500 | LARGE T&R	-	Call TI	Call TI	-40 to 125	
PUCC256601DDBR.B	Active	Preproduction	SOIC (DDB) | 14	2500 | LARGE T&R	-	Call TI	Call TI	-40 to 125	
PUCC256602DDBR	Active	Preproduction	SOIC (DDB) | 14	2500 | LARGE T&R	-	Call TI	Call TI	-40 to 125	
PUCC256602DDBR.A	Active	Preproduction	SOIC (DDB) | 14	2500 | LARGE T&R	-	Call TI	Call TI	-40 to 125	
PUCC256602DDBR.B	Active	Preproduction	SOIC (DDB) | 14	2500 | LARGE T&R	-	Call TI	Call TI	-40 to 125	
PUCC256603DDBR	Active	Preproduction	SOIC (DDB) | 14	2500 | LARGE T&R	-	Call TI	Call TI	-40 to 125	
PUCC256603DDBR.A	Active	Preproduction	SOIC (DDB) | 14	2500 | LARGE T&R	-	Call TI	Call TI	-40 to 125	
PUCC256603DDBR.B	Active	Preproduction	SOIC (DDB) | 14	2500 | LARGE T&R	-	Call TI	Call TI	-40 to 125	
PUCC256604DDBR	Active	Preproduction	SOIC (DDB) | 14	2500 | LARGE T&R	-	Call TI	Call TI	-40 to 125	
PUCC256604DDBR.A	Active	Preproduction	SOIC (DDB) | 14	2500 | LARGE T&R	-	Call TI	Call TI	-40 to 125	
PUCC256604DDBR.B	Active	Preproduction	SOIC (DDB) | 14	2500 | LARGE T&R	-	Call TI	Call TI	-40 to 125	
UCC256601DDBR	Active	Production	SOIC (DDB) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	UCC256601
UCC256601DDBR.A	Active	Production	SOIC (DDB) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	UCC256601
UCC256601DDBR.B	Active	Production	SOIC (DDB) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	UCC256601

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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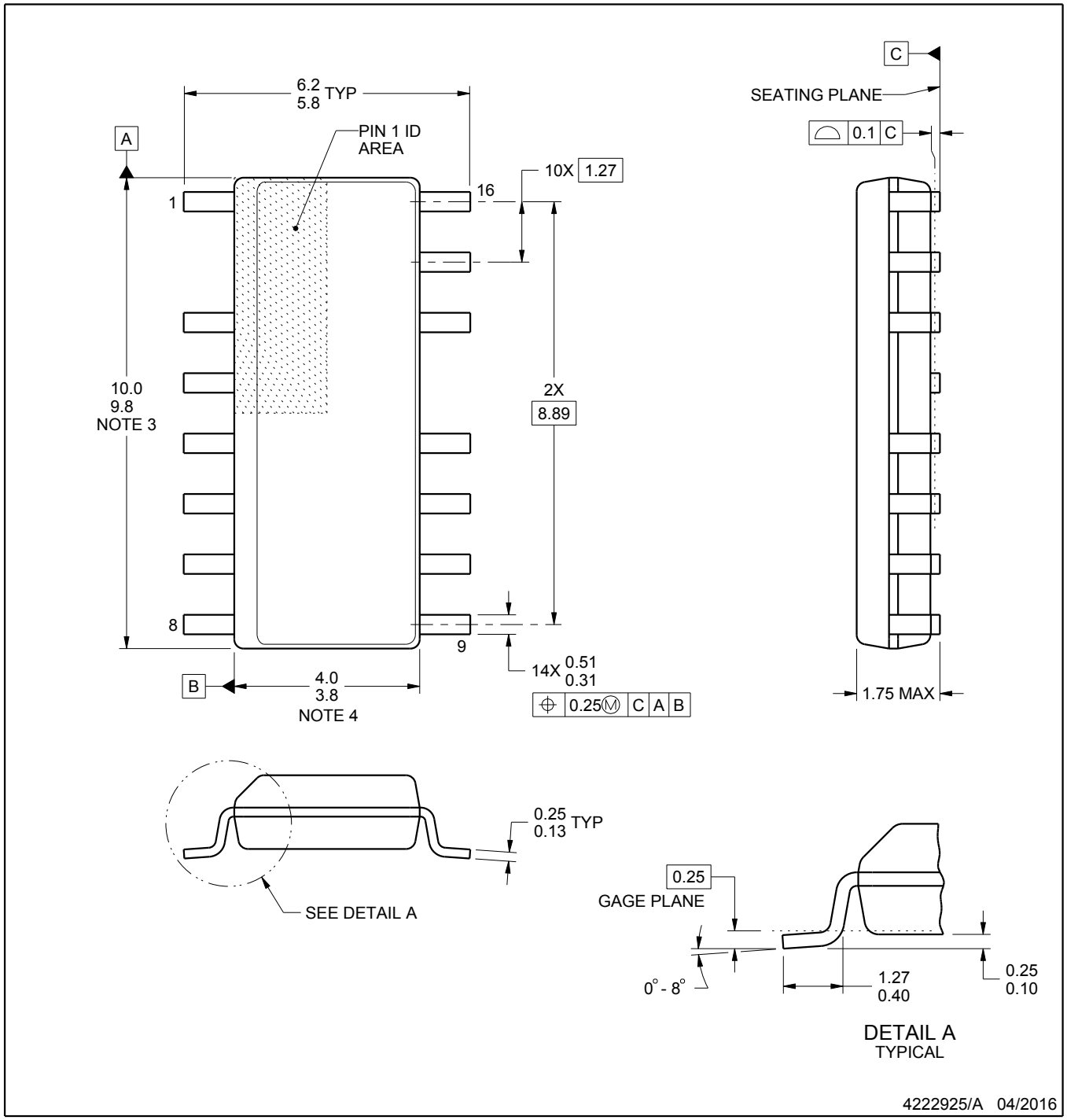
PACKAGE OUTLINE

DDB0014A

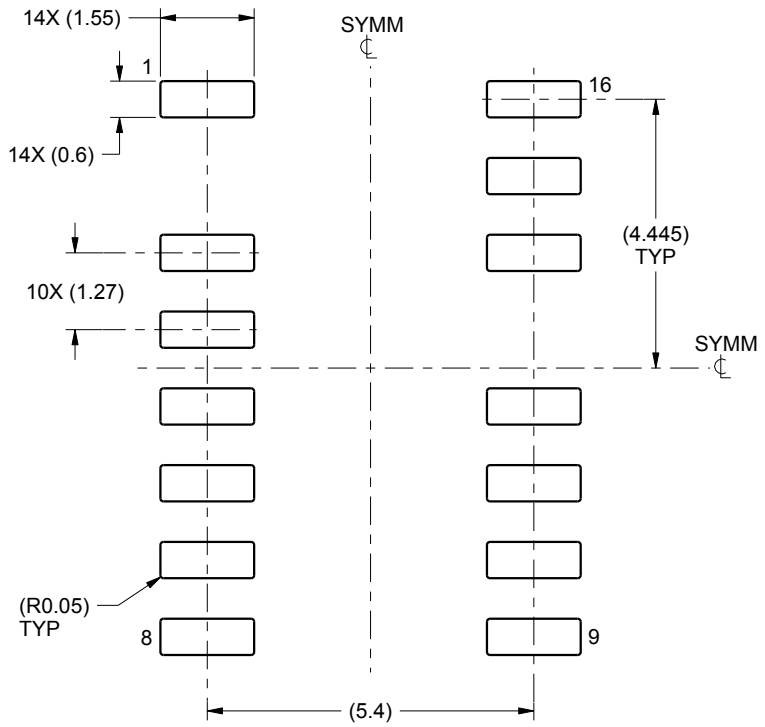
SOIC - 1.75 mm max height

SOIC

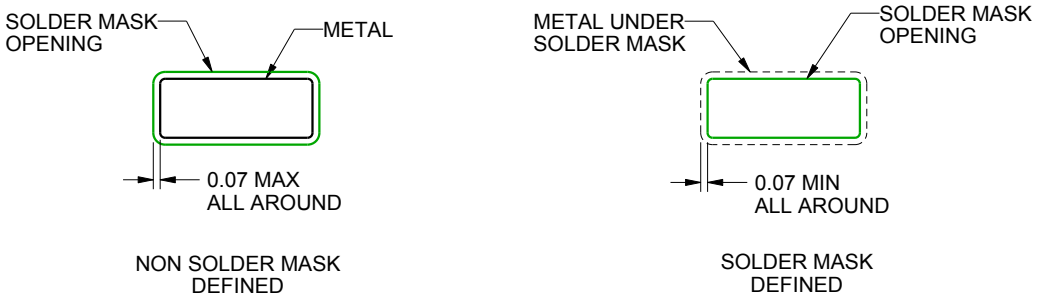


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-012, variation AC.



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS

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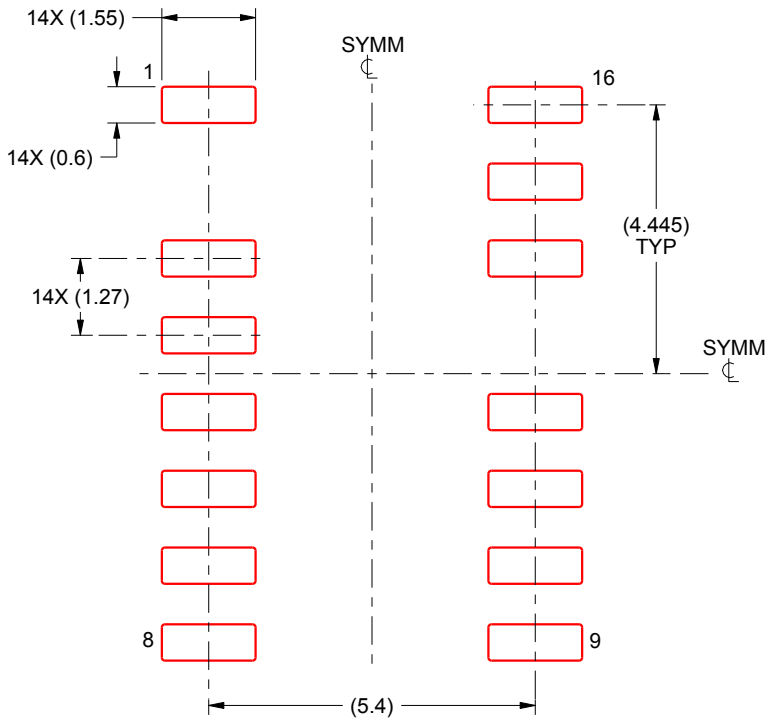
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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